VITESSE

VSC7984
Datasheet

12.5 Gbps Electroabsorption Modulator Driver

FEATURES

- 5 V or –5.2 V power supply operation
- Selectable data retiming
- AC-coupled inputs
- Internally-stabilized modulation and bias outputs
- Excellent output return loss
- 300 mV differential input sensitivity
- Programmable output data eye crossing point
- 2.5 V on-chip voltage reference
- On-chip temperature monitor
- Output Enable

APPLICATIONS

- SONET OC-192 and SDH STM-64 transmission systems up to 12.5 Gbps
- 10 Gigabit Ethernet (GbE) modules
- Very Short Reach (VSR) modules
- Fiber optic transponder and transceiver modules
- SONET/SDH test equipment

GENERAL DESCRIPTION

The VSC7984 is a 12.5 Gbps electroabsorption modulator (EAM) driver for SONET/SDH and 10 GbE applications. It provides selectable data retiming to improve jitter performance and controls for output bias voltage, modulation voltage, and duty cycle. Internal operational amplifiers and an on-chip voltage reference preclude the need for additional off-chip circuitry to stabilize modulation and offset voltages. A temperature-monitor output reflects the internal device temperature to simplify testing and to verify that the device is not being operated beyond its recommended maximum temperature.

The VSC7984 is available in a 24-pin, plastic quad flat no-lead (QFN) package. The device is also available in a lead(Pb)-free package, VSC7984XYF.

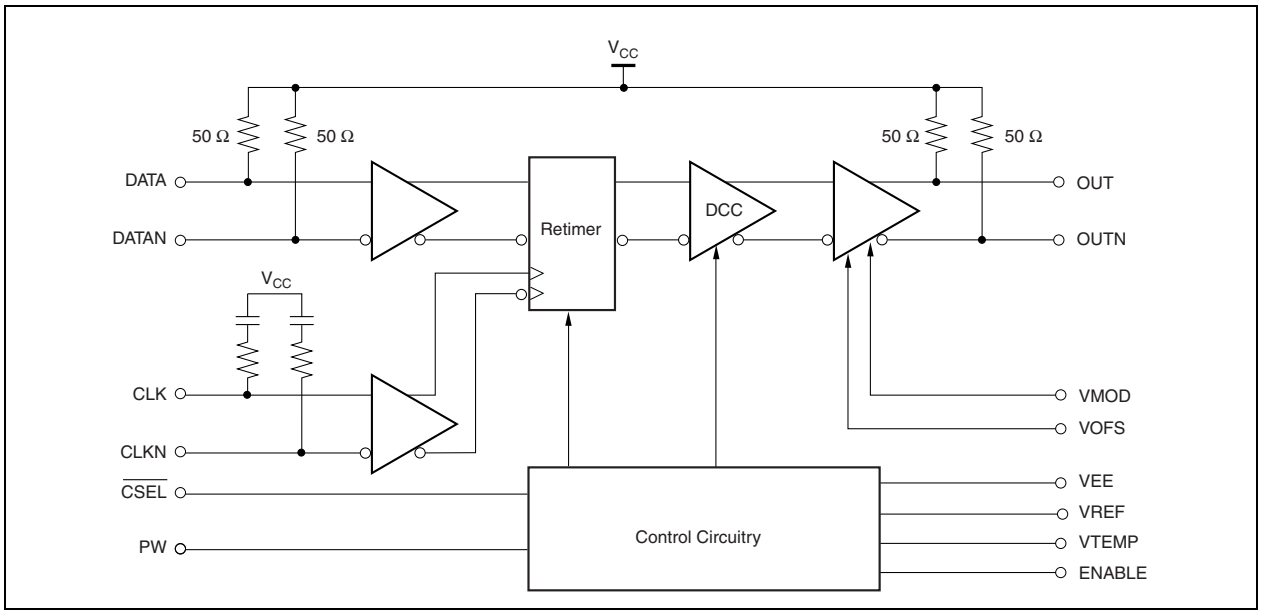

Figure 1. VSC7984 Block Diagram

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REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.1

Revision 4.1 of this datasheet was published on January 19, 2007. The following is a summary of the changes implemented in the datasheet:

- The VSC7984 device is now available in a lead(Pb)-free package.
- The package drawing was updated to display the correct number of pins. For more information, see Figure 11, page 14.

Revision 4.0

Revision 4.0 of this datasheet was published on November 17, 2004. This was the first production-level publication of the document.

FUNCTIONAL DESCRIPTION

The advantages of the VSC7984 device are its excellent output match, data retiming, internal stabilization of bias and modulation, and small package size. The VSC7984 provides up to 2.7 V of output modulation swing and up to 1.4 V of voltage offset (or bias). The output compliance (the lowest achievable peak level of output swing) is –3.5 V. Data retiming provides a means of reducing source jitter, as well as an Output Enable feature that disables modulation for low power modes. An on-chip reference provides a 2.5 V output relative to the most negative rail, which can be used to stabilize modulation and bias voltages over temperature and supply. An on-chip temperature monitor output is also provided for monitoring the internal thermal status.

The VSC7984 inputs are to be AC-coupled and the outputs DC-coupled. For assistance with other configurations, contact your local Vitesse sales representative.

ENABLE

When connected to the most negative rail or left floating, the ENABLE input shuts down the output modulation and bias voltages. Connect to the most positive rail for normal operation.

Voltage Reference

The voltage reference provides a 2.5 V output for stabilizing modulation and bias set points. The modulation and bias control voltages should be relative to the most negative rail. For –5.2 V applications, the control voltages must track power supply variations.

Temperature Monitor Output

The temperature monitor output (VTEMP) output provides a voltage proportional to the die temperature. This is useful for correlating die temperature in various environments. The temperature monitor may then be used to verify thermal designs in the user application.

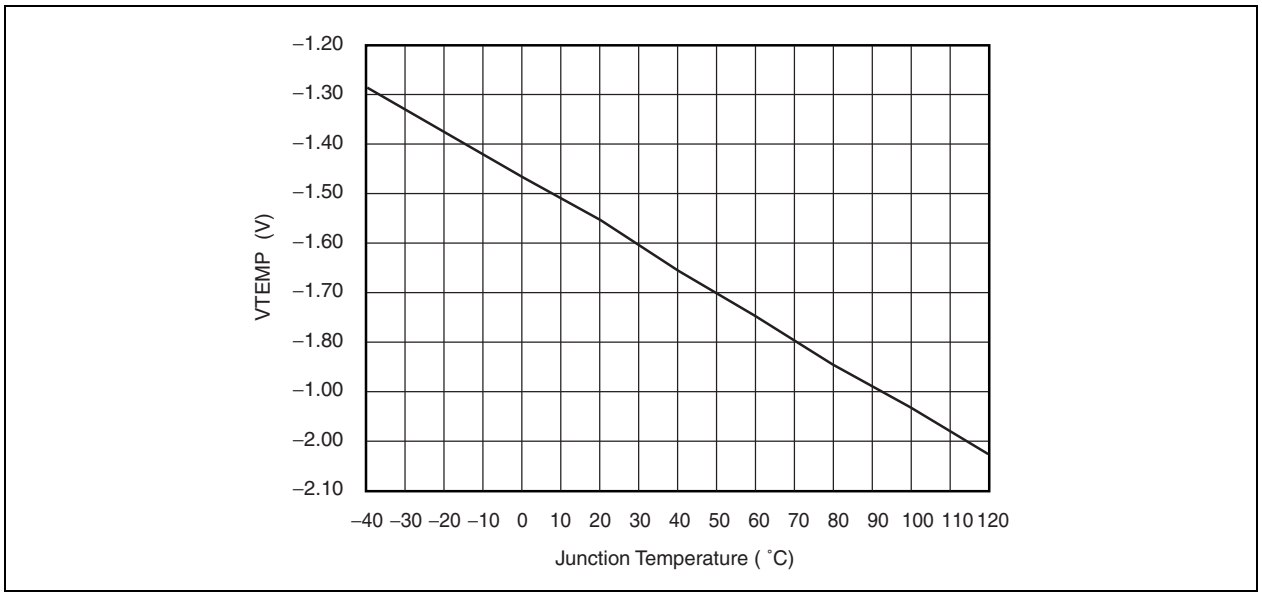


Figure 2. VTEMP vs. Junction Temperature

Power Consumption

The VSC7984 consumes 300 mA typical from a –5.2 V supply and 315 mA maximum with a 2.5 V output swing. The following equations provide the typical current consumption for a given modulation and offset setting:

$$P_D = 5.5\ V \times I_{EE} = 5.5\ V \times [165\ mA + (V_{OM}/25) + 35\ mA] \text{ for } V_{OM} < 1.4\ V \quad \textbf{(EQ 1)}$$

$$P_D = 5.5\ V \times I_{EE} = 5.5\ V \times [165\ mA + (V_{OM}/25) + (-0.024 \times (V_{OM}) + 0.07)] \text{ for } V_{OM} > 1.4\ V \quad \textbf{(EQ 2)}$$

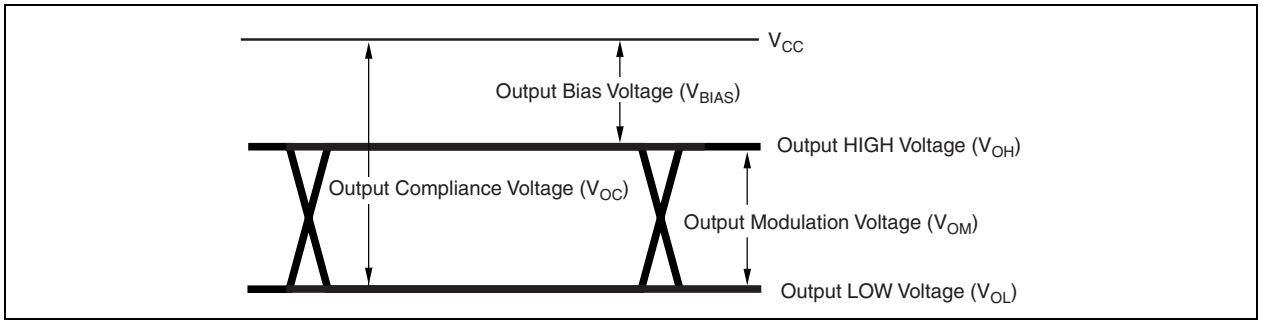


Figure 3. Output Voltage Range Specifications

Modulation, Bias, and Data Eye Crossing Point

Internal feedback stabilizes the VSC7984 modulation and offset voltages so no external operational amplifiers are required to stabilize modulation and bias currents. For optimal stability, it is recommended that a reference voltage relative to the most negative rail be used to set the VMOD and VOFS control voltages. The graphs in Figure 4, page 5, Figure 5, page 5, and Figure 6, page 6 depict bias voltage, modulation voltage, and data eye crossing point range versus their control voltage.

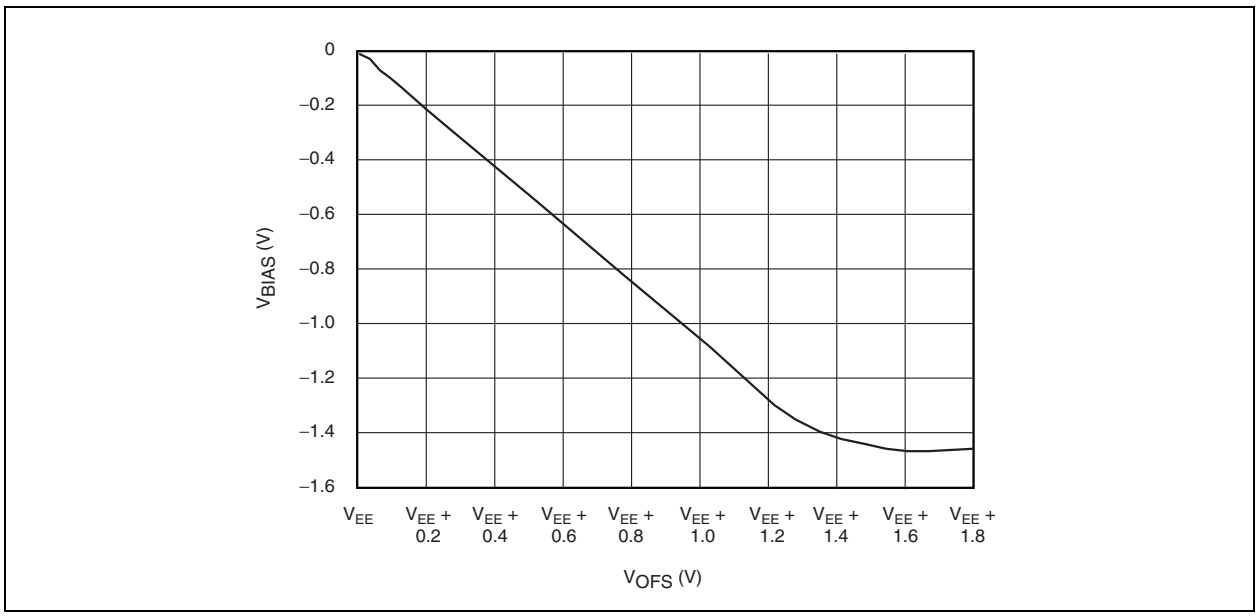


Figure 4. Output Bias Voltage vs. Output Offset Control Voltage

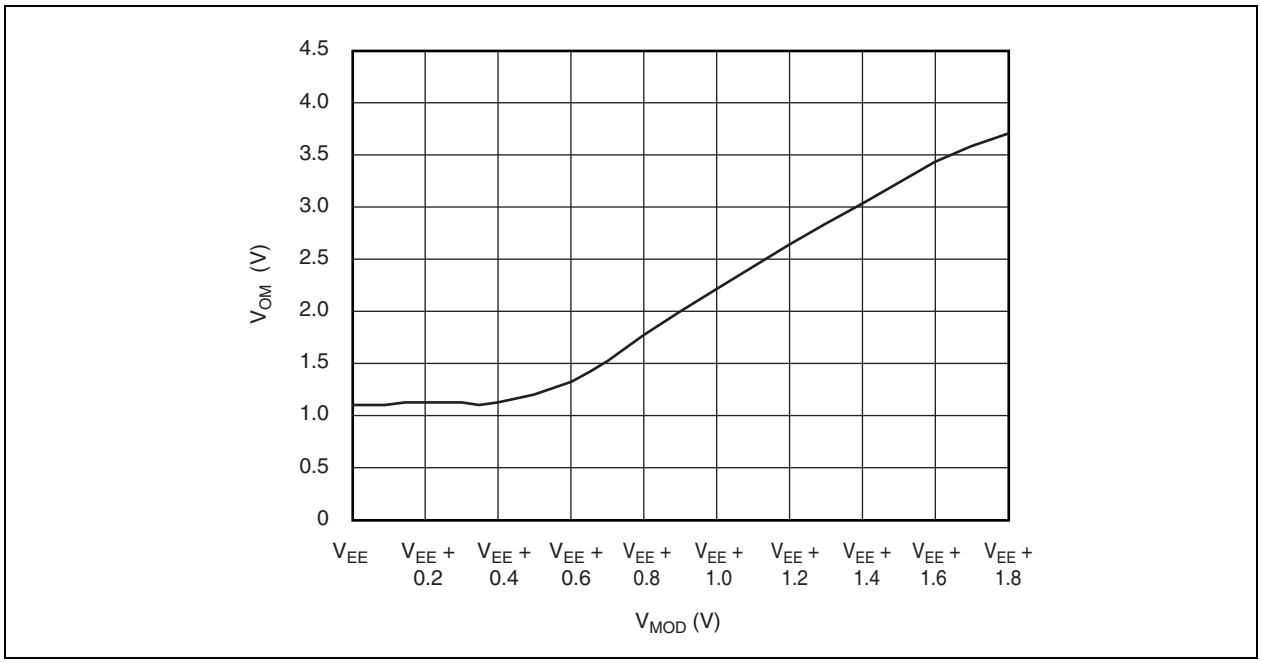


Figure 5. Output Modulation Voltage vs. Output Modulation Control Voltage

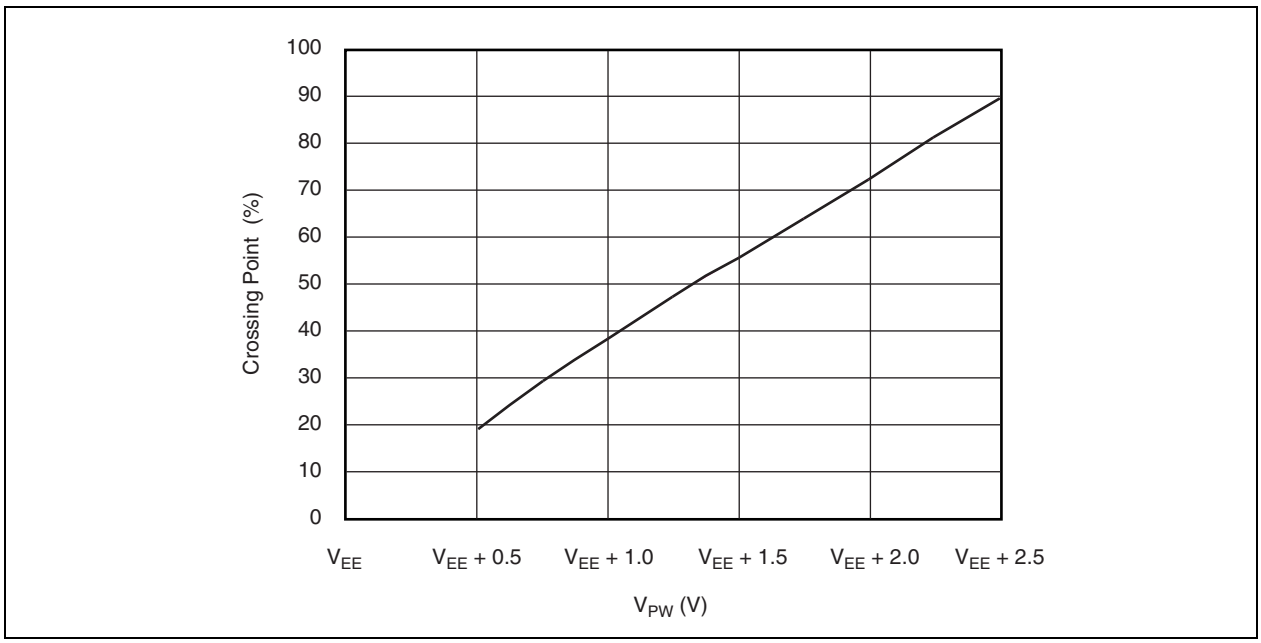


Figure 6. Data Eye Crossing vs. Pulse Width Control Voltage

ELECTRICAL SPECIFICATIONS

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC7984 device.

DC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 3, page 10. Data input pattern at PRBS 2^{31}–1 and 11.3 Gbps, unless otherwise noted.

Table 1. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
$V_{CC} - V_{EE}$	Power supply voltage	4.75	5.0	5.5	V	
I_{EE}	Power supply current (nominal bias and modulation current)		300	315	mA	V_{OM} = 2.5 V, V_{BIAS} = 1 V.
$P_{DNOMINAL}$	Power dissipation (nominal bias and modulation current)		1510	1735	mW	V_{OM} = 2.5 V, V_{BIAS} = 1 V.
I_Q	Quiescent power supply current		150	160	mA	ENABLE = LOW.
P_{DQ}	Quiescent power dissipation		780	880	mW	ENABLE = LOW.
V_{MOD}	Output modulation control voltage	V_{EE}		V_{EE} + 2.0	V	See Figure 5.
V_{OFS}	Output offset control voltage for output bias	V_{EE}		V_{EE} + 2.0	V	See Figure 4.
V_{BIAS_MAX}	Maximum output bias voltage		V_{CC} – 1.40	V_{CC} – 1.15	V	R_L = 50 Ω. See Figure 4.
V_{IH}	Input HIGH voltage (ENABLE)	V_{CC} – 3.0			V	
V_{IL}	Input LOW voltage (ENABLE)			V_{CC} – 4.0	V	
V_{REF}	Reference voltage output	V_{EE} + 2.4	V_{EE} + 2.5	V_{EE} + 2.7	V	C_{LOAD} < 100 pF.
I_{VREF}	Reference voltage current output			4	mA	Sourcing.
V_{TEMP}	Temperature monitor output voltage (±6 °C part-to-part variation)	V_{CC} – 1.58		V_{CC} – 1.51	V	T_J = 20 °C. See Figure 2.
		V_{CC} – 2.05		V_{CC} – 1.99	V	T_J = 120 °C. See Figure 2.

AC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 3, page 10. Data input pattern at PRBS 2^{31}–1 and 11.3 Gbps, unless otherwise noted.

Table 2. AC Characteristics

Symbol	Parameter	MinImum	Typical	Maximum	Unit	Condition
f_{DATA}	Data rate		11.3	12.5	Gbps	NRZ.
f_{CLK}	Clock rate	1	11.3	12.5	GHz	
V_{IN}	Single-ended data input voltage amplitude	0.3		1.0	V	AC-coupled, measured peak-to-peak. See Figure 9.
	Differential data input voltage amplitude	0.3		1.0	V	AC-coupled, measured peak-to-peak (150 mV per side). See Figure 9.
V_{CLK}	Single-ended clock input voltage amplitude	0.4		1.0	V	AC-coupled, measured peak-to-peak. See Figure 9.
	Differential clock input voltage amplitude	0.4		1.0	V	AC-coupled, measured peak-to-peak (200 mV per side). See Figure 9.
V_{OC}	Output compliance voltage			V_{CC} – 3.5	V	R_L = 50 Ω, V_{CC} – V_{EE} ≥ 4.9 V V_{OM} ≤ 2.7 V. See Figure 3.
				V_{CC} – 3.3	V	R_L = 50 Ω, V_{CC} – V_{EE} ≥ 4.75 V V_{OM} ≤ 2.7 V. See Figure 3.
V_{OM}	Output modulation voltage	1.4		2.7	V	R_L = 50 Ω.
I_{OM_DIS}	Disabled output current			5	mA	ENABLE = LOW.
t_R, t_F	Output rise time and fall time		25	35	ps	20% to 80%, R_L = 50 Ω.
DCC	Data eye crossing point range	25		85	%	See Figure 6 and Figure 7.
DCC_{STAB}	Data eye crossing point stability	–7		7	%	
V_{PW}	Pulse width control input[1]	V_{EE} + 0.5		V_{EE} + 2.5	V	For 50% crossing point at OUT, set V_{PW} = V_{EE} + 1.1 V. See Figure 6.
–OVS +OVS	Output undershoot /overshoot	–12		10	%	V_{OM} > 1.4 V.
$\overline{CSEL}$	Clock select		Floating		V	Unclocked mode.
		V_{EE}		V_{EE} + 0.3	V	Clocked mode.
t_S	Setup time	0	–11		ps	See Figure 8.
t_H	Hold time	30	25		ps	See Figure 8.
J_{TOT_rms}	Total jitter, rms		2.1	4	ps	Clocked mode.
			2.2	6	ps	Unclocked mode.
$J_{TOT\_p\text{-}p}$	Total jitter, peak-to-peak		12	16	ps	Clocked mode.
			14	18	ps	Unclocked mode.
S_{11}	Clock input return loss		–11		dB	1 GHz to 10 GHz.
			–9		dB	10 GHz to 15 GHz.
S_{11}	Data input return loss		–11		dB	50 MHz to 10 GHz.
			–10		dB	10 GHz to 15 GHz.
S_{22}	Data output return loss		–11			50 MHz to 7.5 GHz.
			–9			7.5 GHz to 10 GHz.

1. The VSC7984 is capable of moving the data eye crossing point to the very top and bottom of the eye diagram.

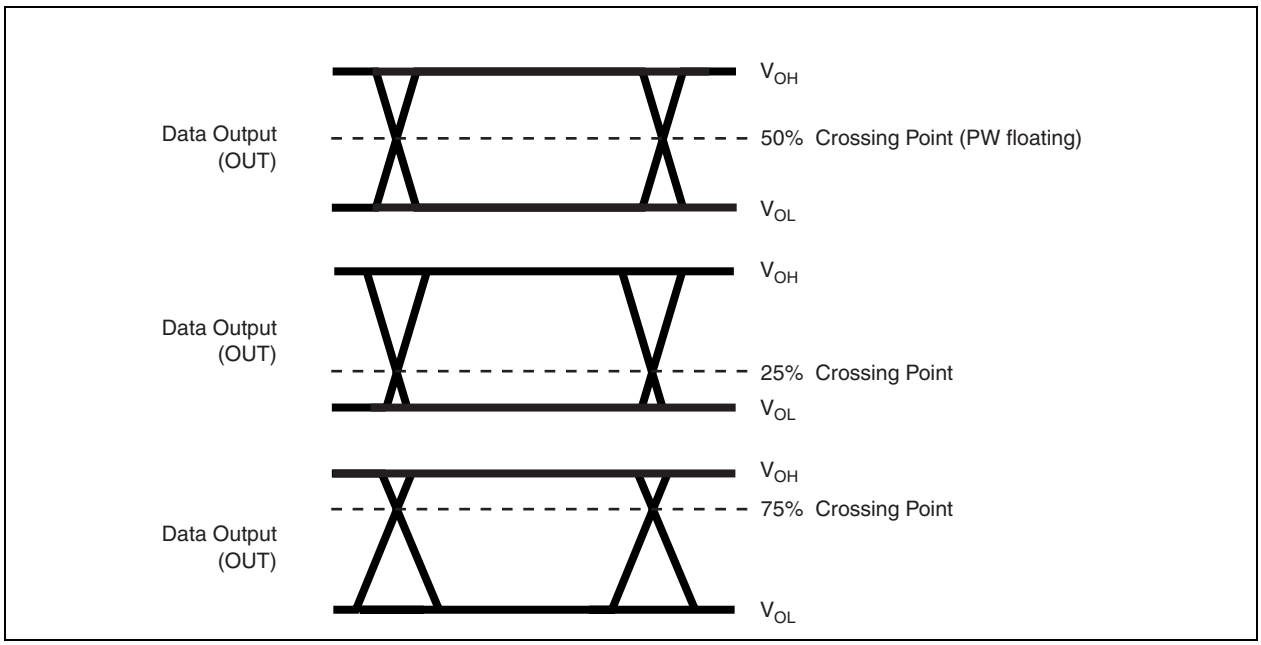


Figure 7. Data Eye Crossing Point Control Diagram

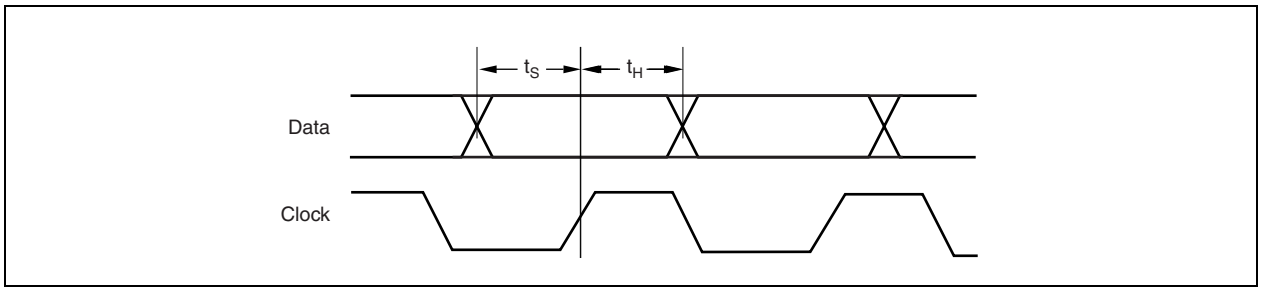


Figure 8. Setup and Hold Timing Diagram

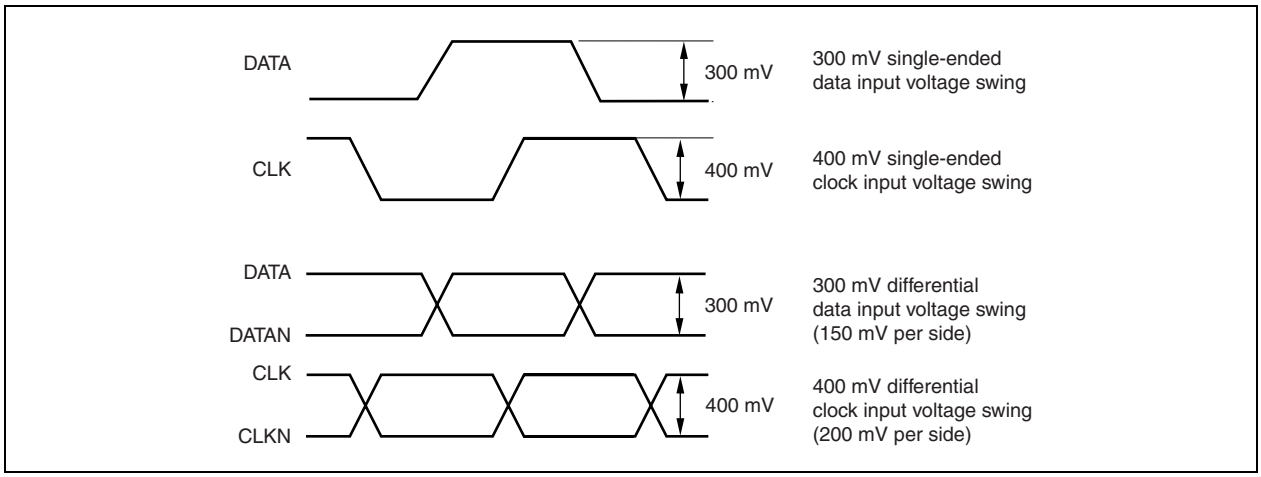


Figure 9. Input Voltage Swing Diagram

Operating Conditions

The following table shows the recommended operating conditions for the VSC7984 device.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{CC}	Power supply voltage for positive supply operation		5.0		V	V_{EE} = GND
V_{EE}	Power supply voltage for negative supply operation		–5.2		V	V_{CC} = GND
T	Operating temperature(1)	–20		95	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Stress Ratings

Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 4. Stress Ratings

Symbol	Parameter	Minimum	Maximum	Unit
$V_{CC} - V_{EE}$	Power supply voltage	0	6	V
I_{EE}	Supply current		500	mA
V_{IN}, V_{CLK}	Input voltage	$V_{CC} - 2$	$V_{CC} + 1$	V
V_{OUT}	Output voltage		$V_{CC} - 4$	V
V_{MOD}	Output voltage modulation control voltage	$V_{EE} - 0.5$	V_{CC}	V
V_{OFS}	Output voltage offset control voltage	$V_{EE} - 0.5$	V_{CC}	V
V_{PW}	Pulse width control voltage	V_{EE}	V_{CC}	V
T_S	Storage temperature	–55	140	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–250	250	V

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PIN DESCRIPTIONS

The VSC7984 device has 24-pins, which are described in this section.

Pin Diagram

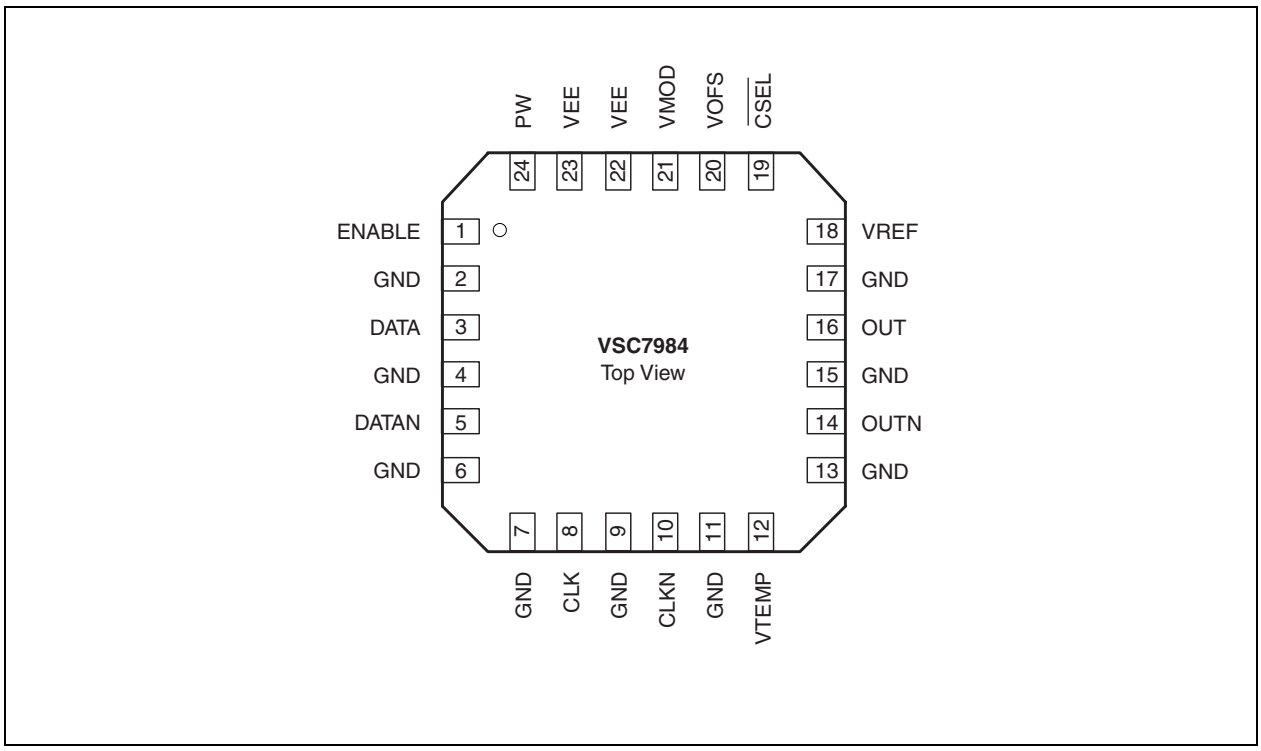


Figure 10. Pin Diagram

Pin Identifications

This section contains the pin descriptions for the VSC7984 device.

Table 5. Pin Identifications

Pin	Signal Name	I/O	Description
1	ENABLE	I	Enables output modulation and bias voltage.
2	GND	Power	Ground.
3	DATA	I	Data input, true.
4	GND	Power	Ground.
5	DATAN	I	Data input, complement.
6	GND	Power	Ground.
7	GND	Power	Ground.
8	CLK	I	Clock input, true.
9	GND	Power	Ground.
10	CLKN	I	Clock input, complement.
11	GND	Power	Ground.
12	VTEMP	O	Device temperature monitor output.
13	GND	Power	Ground.
14	OUTN	O	Data output, complement.
15	GND	Power	Ground.
16	OUT	O	Data output, true.
17	GND	Power	Ground.
18	VREF	O	Reference voltage.
19	$\overline{\text{CSEL}}$	I	Clock enable. For clock mode, connect to V_{EE}; leave floating for unclocked mode.
20	VOFS	I	Output bias control. See Figure 4, page 5.
21	VMOD	I	Output modulation control. See Figure 5, page 5.
22	VEE	Power	Negative power supply.
23	VEE	Power	Negative power supply.
24	PW	I	Pulse width control for data eye crossing point, true.

1. *A voltage HIGH on the data input (pin 3) corresponds to a voltage HIGH on the data output (pin 16).*

PACKAGE INFORMATION

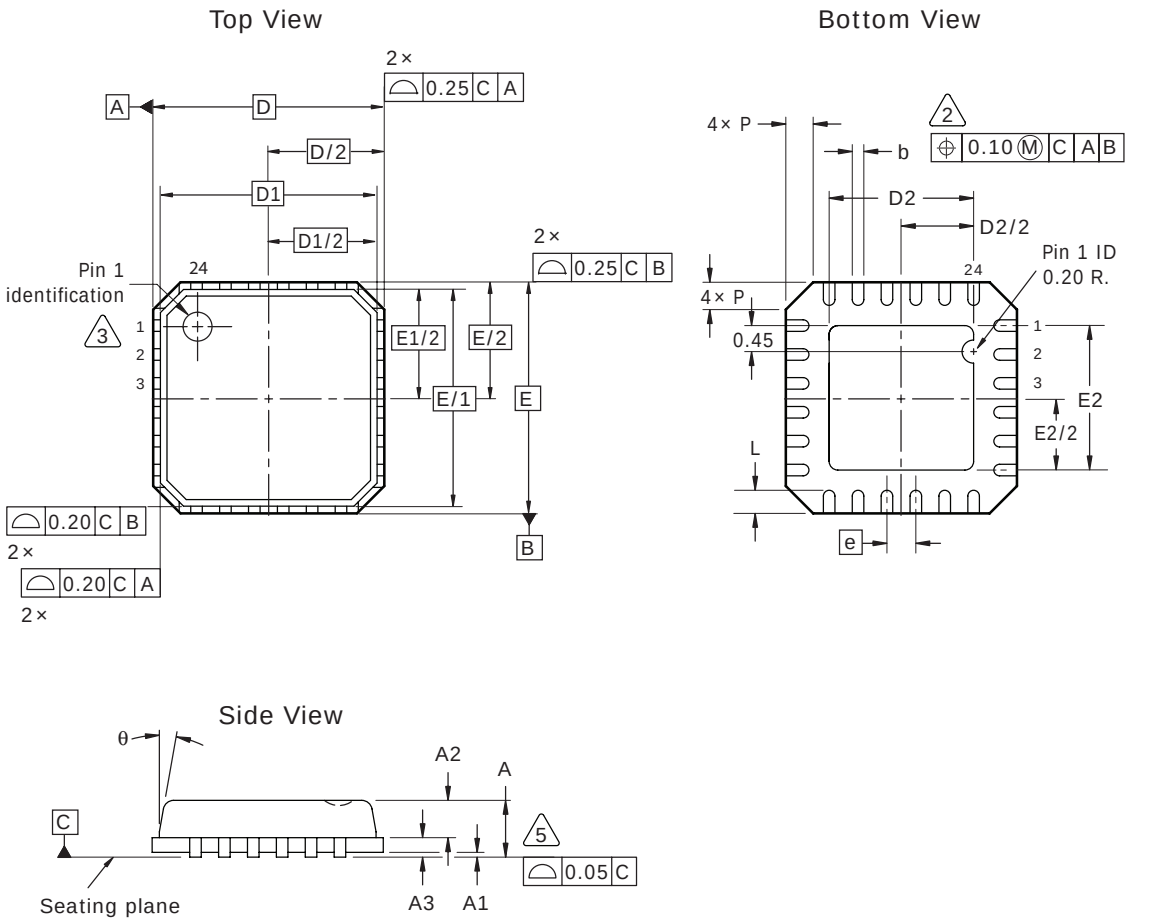
A significant advantage of the VSC7984 device is its small plastic package. VSC7984YF is a 24-pin, plastic quad flat no-lead (QFN) package with an exposed pad, 4 mm × 4 mm body size, 0.65 mm body thickness, 0.5 mm pin pitch, and 1 mm maximum height. The device is also available in a lead(Pb)-free package, VSC7984XYF.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The backside of the die is mounted directly to a heat spreader with conductive epoxy. The exposed heat spreader must be connected to the most negative power supply (typically –5 V) or must be left floating.

The primary heat path is through the exposed heat spreader on the bottom of the package. Some heat can be removed through the top of the package; however, it is recommended to thermally connect the exposed heat spreader to the PCB. Contact your local Vitesse sales representative for detailed information about the PCB design.

Package Drawing



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Dimension b applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.
3. Pin 1 is indicated on the top surface of the package by indentation mark or other feature. Exact size and shape is optional.
4. Maximum package warpage is 0.05 mm.
5. Applies only to the exposed pad and terminals; excludes the embedded part of exposed pad.

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A		0.85	1.00
A1	0.00	0.01	0.05
A2		0.65	0.80
A3		0.20 Ref	
D		4.00 BSC	
D1		3.75 BSC	
D2	2.35	2.50	2.65
E		4.00 BSC	
E1		3.75 BSC	
E2	2.35	2.50	2.65
θ			12°
P	0.24	0.42	0.60
e		0.50 BSC	
L	0.30	0.40	0.60
b	0.18	0.23	0.30

Figure 11. Package Drawing

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

The VSC7984 device is available in two package types. VSC7984YF is a 24-pin, plastic quad flat no-lead (QFN) package with an exposed pad, 4 mm × 4 mm body size, 0.65 mm body thickness, 0.5 mm pin pitch, and 1 mm maximum height. The device is also available in a lead(Pb)-free package, VSC7984XYF.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC7984 device.

VSC7984 12.5 Gbps Clocked Modulator Driver

Part Number	Description
VSC7984YF	24-pin, plastic QFN with an exposed pad, 4 mm × 4 mm body size, 0.65 mm body thickness, 0.5 mm pin pitch, and 1 mm maximum height
VSC7984XYF	Lead(Pb)-free, 24-pin, plastic QFN with an exposed pad, 4 mm × 4 mm body size, 0.65 mm body thickness, 0.5 mm pin pitch, and 1 mm maximum height

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