SY88953AL

3.3V 10.7Gbps CML Limiting Post Amplifier with TTL SD and /SD

General Description

The SY88953AL high-speed, limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88953AL quantizes these signals and outputs CML level waveforms.

The SY88953AL operates from a single +3.3V power supply over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, the SY88953AL can take signals with data rates up to 10.7Gbps and as small as 5mV$_{PP}$ and amplify them to drive devices with CML inputs.

The SY88953AL outputs TTL signal-detect (SD and /SD) signals. A programmable signal-detect level set pin (SD$_{LVL}$) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD$_{LVL}$ and deasserts low otherwise. /SD is the complementary output of SD. /SD can be fed back to the enable (/EN) input to maintain output stability under a loss-of-signal (LOS) condition. /EN deasserts the true output signal without removing the input signal. Typically 6dB SD hysteresis is provided to prevent chattering.

The SY88953AL also includes an input threshold adjustment to correct pulse-width distortion.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

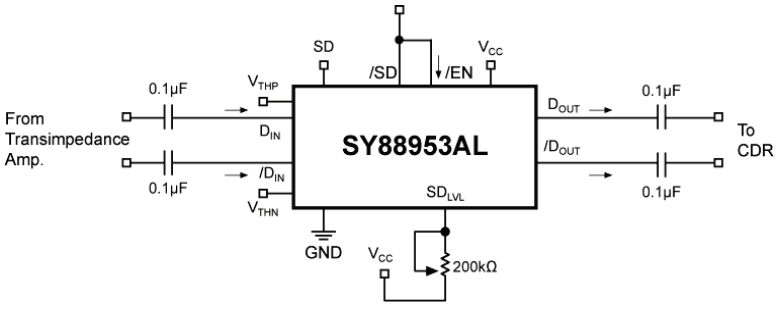
Features

- Single 3.3V power supply
- Up to 10.7Gbps operation
- 700mV$_{PP}$ output swing with 25ps edge rates (typically)
- 28dB voltage gain with 5mV$_{PP}$ input sensitivity
- On-chip 50Ω I/O termination
- Programmable signal detect (SD and /SD) with 6dB hysteresis
- Chatter-free OC-TTL SD and /SD outputs with internal 5kΩ pull-up resistors can feedback to TTL enable (/EN) input
- Available in a tiny 3mm x 3mm 16-pin QFN package or die
- Low power (62mA)

Applications

- OC-192 SDH/SONET
- 10G Ethernet/Fibre Channel receivers
- Up to 10.7Gbps proprietary link
- XFP transceivers
- Line driver/receiver

Typical Application



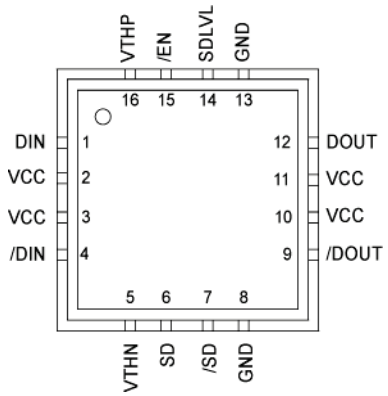
Ordering Information

Part Number	Package Marking	Operating Range	Package	Lead Finish
SY88953ALMG	953A with Pb-Free bar-line indicator	Industrial	16-Pin QFN	Pb-Free, NiPdAu
SY88953ALMGTR[1]	953A with Pb-Free bar-line indicator	Industrial	16-Pin QFN	Pb-Free, NiPdAu

Note:

1. Tape and reel.

Pin Configuration



16-Pin QFN

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	DIN	Data input	True data input with 50Ω resistor to V_{CC}.
2, 3, 10, 11	VCC	Power supply	Positive power supply.
4	/DIN	Data input	Complementary data input with 50Ω resistor to V_{CC}.
5	VTHN	Input	/DIN DC threshold adjustment pin.
6	SD	Open-collector TTL output with internal 5kΩ pull-up resistor	Signal detect asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
7	/SD	Open-collector TTL output with internal 5kΩ pull-up resistor	Inverted signal detect asserts low when the data input amplitude rises above the threshold set by SD_{LVL}.
8, 13, EP	GND	Ground	Device ground. Exposed pad must be soldered to PCB ground for proper electrical and thermal performance.
9	/DOUT	CML output	Complementary data output.
12	DOUT	CML output	True data output.
14	SDLVL	Input	Signal detect level set: A resistor from this pin to V_{CC} set the threshold for the data input amplitude at which SD asserts.
15	/EN	TTL input default is high	Enable: Deasserts true data output when high.
16	VTHP	Input	DIN DC threshold adjustment pin.

Absolute Maximum Ratings[2]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Data Input Voltage
(D_{IN}, /D_{IN}) ..... (V_{CC}–1.0V) to (V_{CC}+0.5V)
Data Output Voltage
(D_{OUT}, /D_{OUT}) ..... (V_{CC}–1.0V) to (V_{CC}+0.5V)
/EN Voltage ..... 0V to V_{CC}
SD, /SD Current 5mA
SDLVL Voltage ..... (V_{CC}–1.3V) to V_{CC}
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[3]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Junction Thermal Resistance[4]
QFN-16 (θ_{JA}) Still-Air ..... 59°C/W
QFN-16 (θ_{JB}) Still-Air ..... 32°C/W

DC Electrical Characteristics[5]

V_{CC} = 3.0V to 3.6V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V; T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current	No output load		62	85	mA
V_{SDLVL}	SDLVL voltage		V_{CC}–1.3		V_{CC}	V
V_{IH}	/EN input HIGH voltage		2.0			V
V_{IL}	/EN input LOW voltage				0.8	V
I_{IH}	/EN input HIGH current	V_{IN} = V_{CC}			20	µA
I_{IL}	/EN input LOW current	V_{IN} = 0.5V	–0.3			mA
V_{OH}	SD, /SD output HIGH level		2.4			V
V_{OL}	SD, /SD output LOW level	I_{OL} = +2mA			0.5	V
V_{OH}	Output HIGH voltage	50Ω to V_{CC} output load	V_{CC}–0.02	V_{CC}–0.005	V_{CC}	V
V_{OL}	Output LOW voltage	50Ω to V_{CC} output load	V_{CC}–0.40	V_{CC}–0.35	V_{CC}–0.24	V
V_{OFFSET}	Differential output offset				±80	mV
Z_O	Single-ended output impedance		45	50	55	Ω
Z_{IN}	Single-ended input impedance					

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.
4. Exposed pad must be soldered to PCB's ground plane.
5. Specification for packaged product only

AC Electrical Characteristics

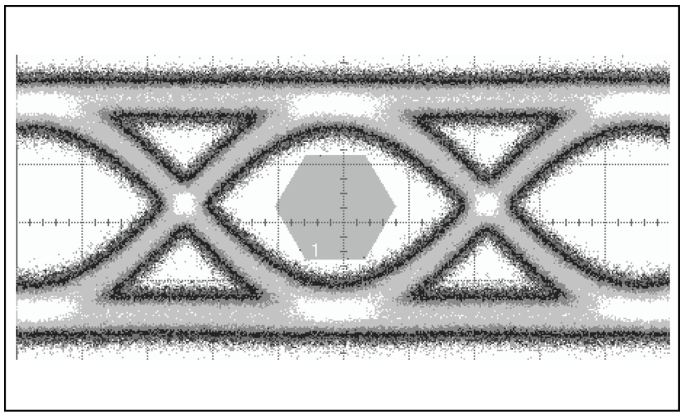
V_{CC} = 3.0V to 3.6V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V; T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
HYS	SD Hysteresis	Electrical signal	2	6	8	dB
PSRR	Power supply rejection ratio			35		dB
t_{OFF}	SD, /SD release time			0.1	0.5	µs
t_{ON}	SD, /SD assert time			0.2	0.5	µs
t_r/t_f	Output rise/fall time	$V_{ID} \geq 50mV_{PP}$		25	35	ps
V_{ID}	Differential input voltage swing		5		1800	mV_{PP}
V_{OD}	Differential output voltage swing		600	700	800	mV_{PP}
V_{SR}	SD sensitivity range		5		50	mV_{PP}
LOSAL	Low LOS assert level	RLOSLVL = 10kΩ, Note 6		11		mV_{PP}
LOSDL	Low LOS de-assert level	RLOSLVL = 10kΩ, Note 6		17		mV_{PP}
HSYL	Low LOS hysteresis	RLOSLVL = 10kΩ, Note 7		3.5		dB
LOSAM	Medium LOS assert level	RLOSLVL = 5kΩ, Note 6		17		mV_{PP}
LOSDM	Medium LOS de-assert level	RLOSLVL = 5kΩ, Note 6		26		mV_{PP}
HSYM	Medium LOS hysteresis	RLOSLVL = 5kΩ, Note 7		3.5		dB
LOSAH	High LOS assert level	RLOSLVL = 100Ω, Note 6		45		mV_{PP}
LOSDH	High LOS de-assert level	RLOSLVL = 100Ω, Note 6		68		mV_{PP}
HSYH	High LOS hysteresis	RLOSLVL = 100Ω, Note 7		3.5		dB
S_{21}	Single-ended small-signal gain		16	22		dB
$A_{OV(Diff)}$	Differential voltage gain		22	28		dB
B_{-3dB}	3dB Bandwidth			7.5		GHz

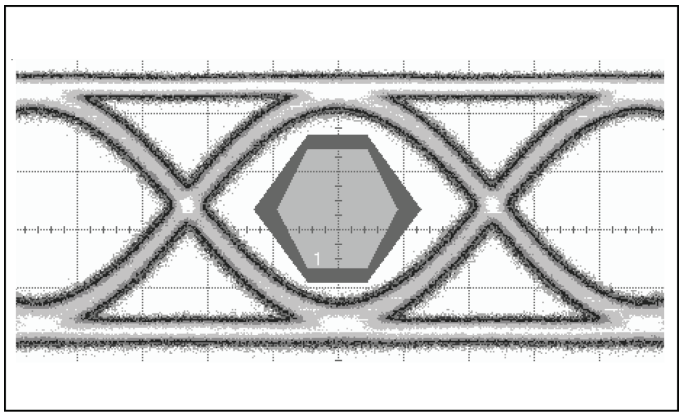
Notes:

6. See “Typical Operating Characteristics” for the graph that demonstrates how to choose a particular RLOSLVL for a particular LOS assert and its associated de-assert amplitude.
7. This specification defines electrical hysteresis as 20log(LOS de-assert/LOS assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending on the level of received power and ROSA characteristics.

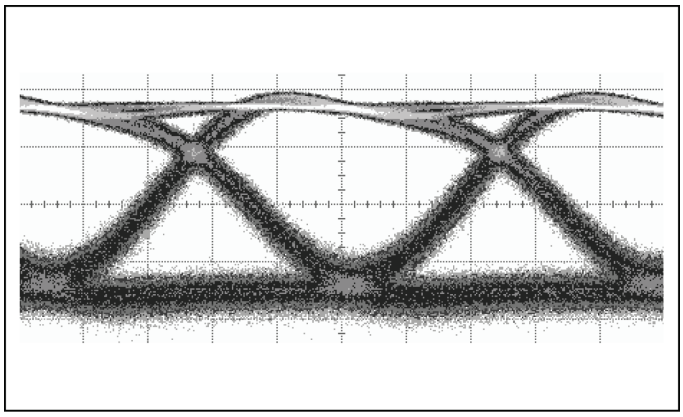
Typical Operating Characteristics



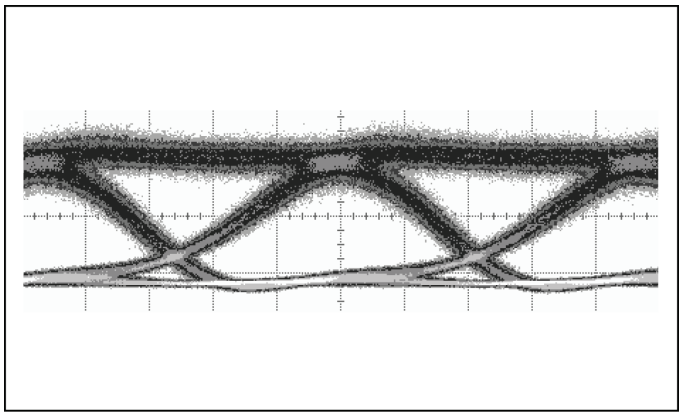
10.7Gbps, V_{IN} = 5mV_{PP}, V_{TH} Open (20ps/div)



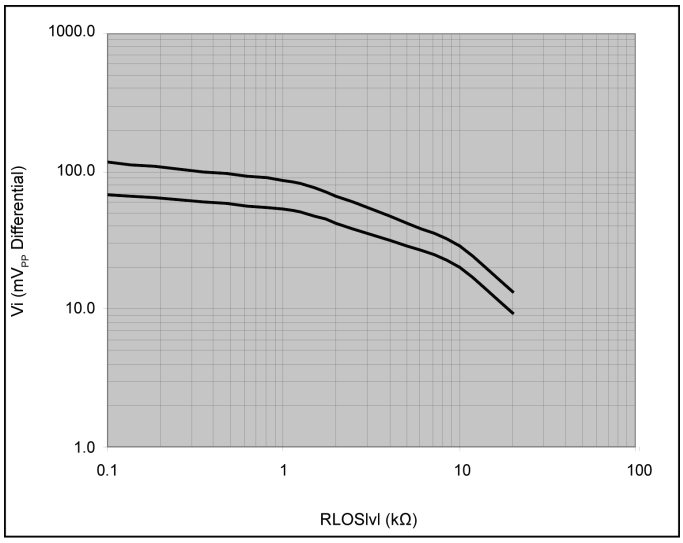
10.7Gbps, V_{IN} = 10mV_{PP}, V_{TH} Open (20ps/div)



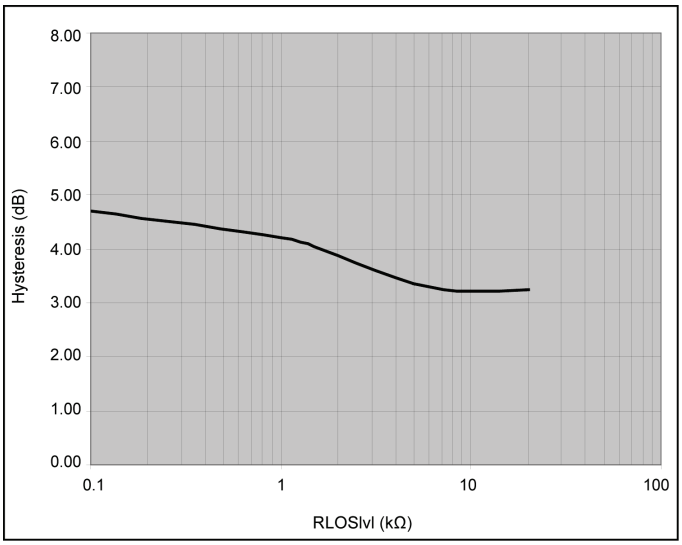
10.7Gbps, V_{IN} = 20mV_{PP}, V_{TH} = 1.0V (20ps/div)



10.7Gbps, V_{IN} = 20mV_{PP}, V_{TH} = 1.5V (20ps/div)

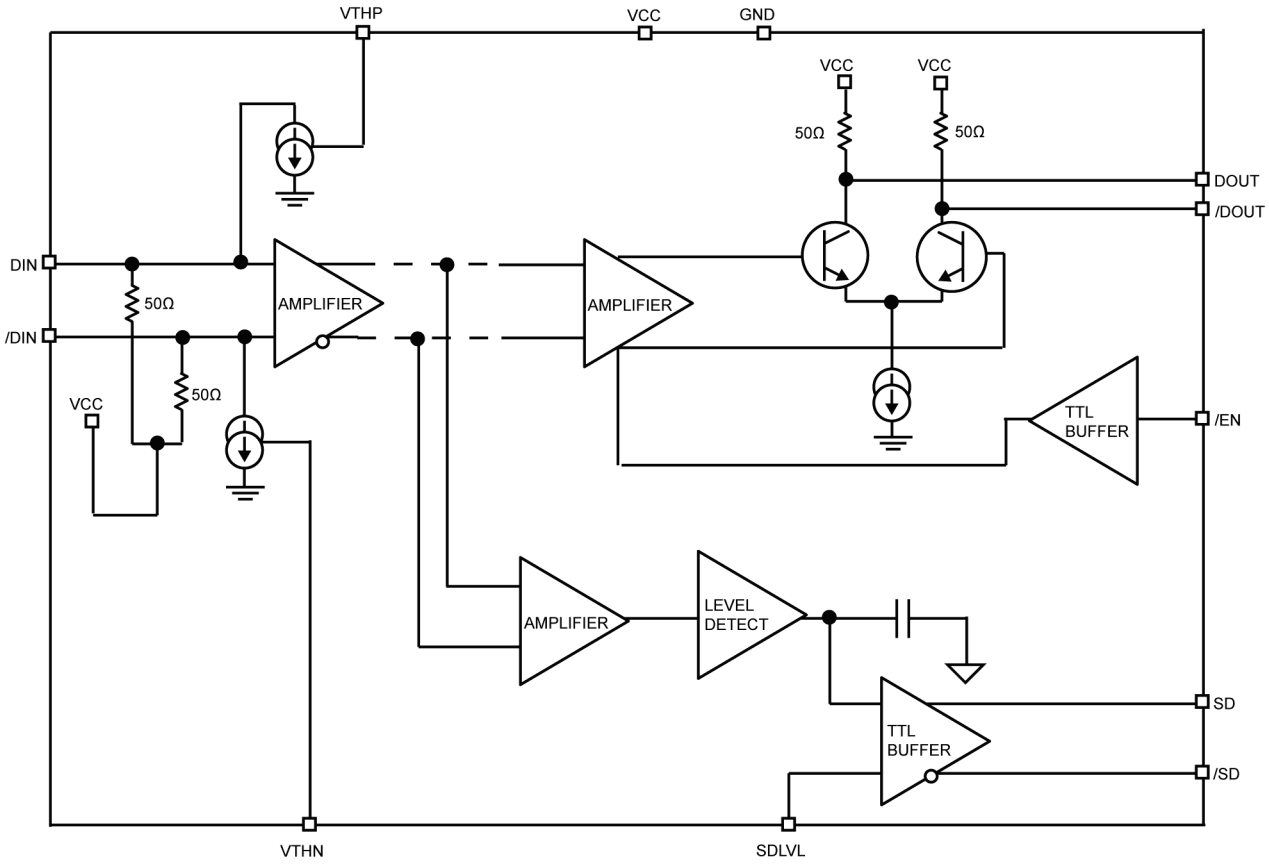


SY88953AL LOSA, LOSD vs. RLOSlvl



SY88953AL Hysteresis vs. RLOSlvl

Functional Diagram



Design Procedure

Layout and PCB Design

Because the SY88953AL is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from large swing outputs to the input via the power supply.

The SY88953AL's ground pins should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs that can degrade performance.

Functional Description

The SY88953AL high-speed limiting post amplifier operates from a single +3.3V power supply over temperatures from –40°C to +85°C. Signals with data rates up to 10.7Gbps and as small as $5mV_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88953AL generates SD and /SD outputs. SDLVL sets the sensitivity of the input amplitude detection. The SY88953AL also includes an input threshold adjustment to correct pulse width distortion.

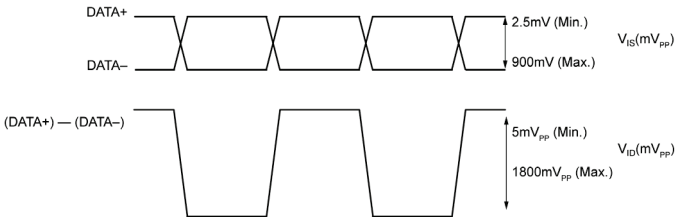


Figure 1. V_{IS} and V_{ID} Definitions

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88953AL's input stage. The high-sensitivity of the input amplifier allows signals as small as $5mV_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{PP}$. Input signals are linearly amplified with a typical differential voltage gain of 28dB. Because it is a limiting amplifier, the SY88953AL outputs typically $700mV_{PP}$ voltage-limited waveforms for input signals that are greater than $32mV_{PP}$. Applications requiring the SY88953AL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88953AL's input pins to ensure the best performance of the device.

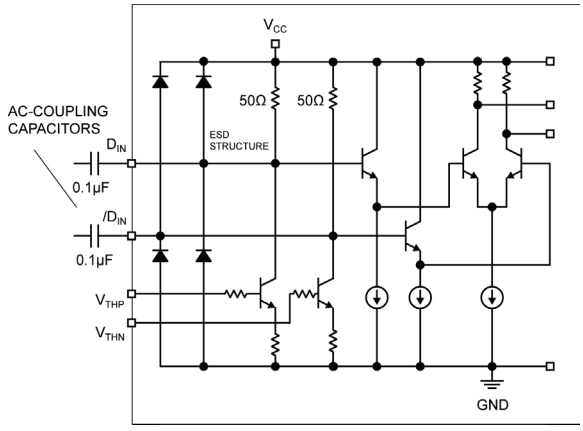


Figure 2. Input Structure

Threshold Adjustment

The SY88953AL's duty cycle can be controlled by forcing an offset at either input using V_{THP} or V_{THN}. Typically, only one of the inputs is required to be adjusted, depending on the required direction of the pulse width adjustment. The SY88953AL implements current source based offset control of the inputs. The Typical Operating Characteristics section shows the offset applied to the input for a given V_{TH} voltage. This feature is disabled by simply setting V_{TH} to GND.

Output Buffer

The SY88953AL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically $700mV_{PP}$ waveforms across 25Ω total loads. The output buffer thus switches typically 16mA tail-current.

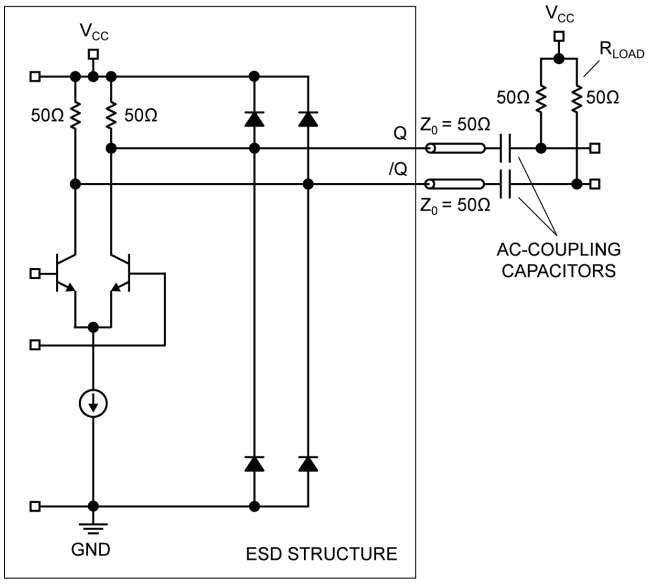


Figure 3. Output Structure

Signal-Detect

The SY88953AL generates chatter-free signal-detect (SD and /SD) open-collector TTL outputs with internal 5kΩ pull-up resistors as shown in Figure 4. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. /SD is the complementary output of SD. /SD asserts low if the input amplitude rises

above the threshold set by SD_{LVL} and deasserts high otherwise. /SD can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN deasserts the true output signal without removing the input signals. Typically 6dB SD hysteresis is provided to prevent chattering.

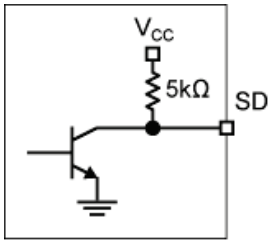


Figure 4. SD, /SD Output Structure

Signal-Detect Level Set

A programmable signal-detect level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} sets the voltage at SD_{LVL}. This voltages ranges from V_{CC} to V_{CC}–1.3V. The external resistor creates a voltage divider between V_{CC} and V_{CC}–1.3V as shown in Figure 5. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from SD_{LVL} to V_{CC}, the smaller the SD sensitivity. Hence, larger input amplitude is required to assert SD. The Typical Operating Characteristics section shows the relationship between the input amplitude detection sensitivity and the SD_{LVL} voltage.

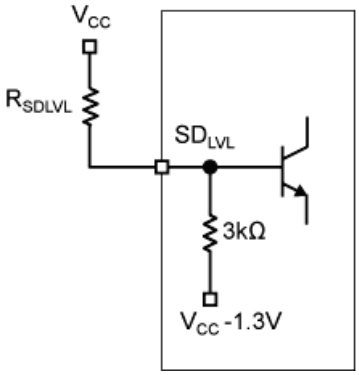
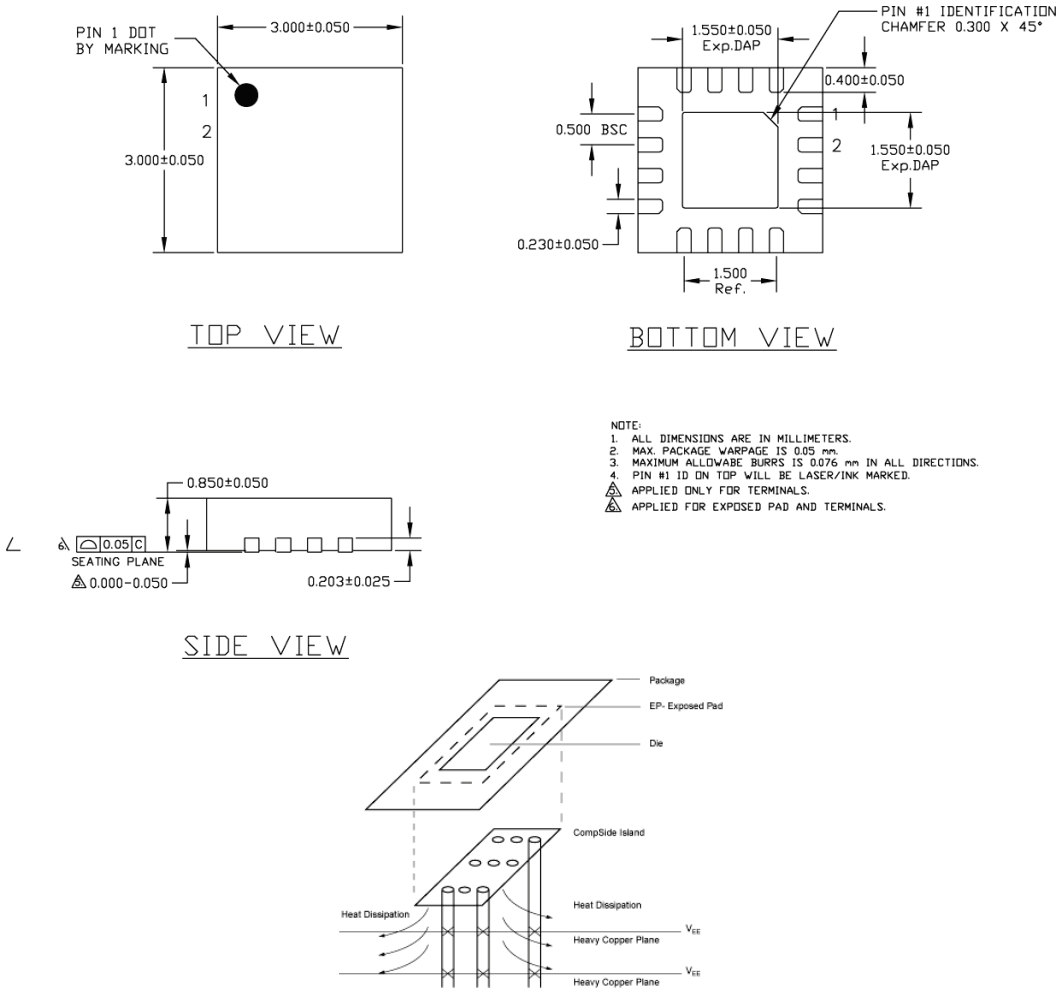


Figure 5. SD_{LVL} Setting Circuit

Hysteresis

The SY88953AL provides typically 6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88953AL provides typically 3dB SD optical hysteresis. As the SY88953AL is an electrical device, this datasheet refers to hysteresis in electrical terms. With 6dB SD hysteresis, a voltage factor of two is required to assert or de-assert SD.

Package Information[8]



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Note:

8. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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