MIC22700

1MHz, 7A Integrated Switch High-Efficiency Synchronous Buck Regulator

General Description

The Micrel MIC22700 is a high-efficiency, 7A, integrated switch, synchronous buck (step-down) regulator. The MIC22700 is optimized for highest efficiency, achieving more than 95% efficiency while still switching at 1MHz over a broad range. The device works with a small 1µH inductor and 100µF output capacitor. The ultra-high speed control loop keeps the output voltage within regulation even under extreme transient load swings commonly found in FPGAs and low-voltage ASICs. The output voltage can be adjusted down to 0.7V to address all low voltage power needs. The MIC22700 offers a full range of sequencing and tracking options. The Enable/Delay pin combined with the Power Good/POR pin allows multiple outputs to be sequenced in any way during turn-on and turn-off. The RC (Ramp Control™) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start up.

The MIC22700 is available in a 24-pin 4mm x 4mm MLF® with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

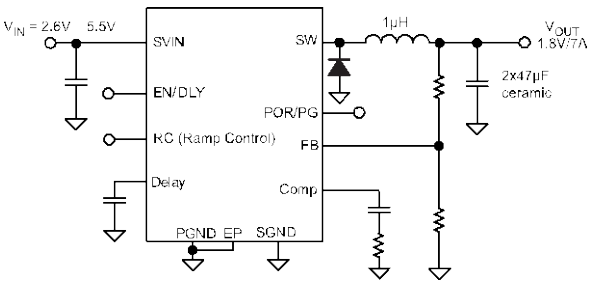
Features

- Input voltage range: 2.6V to 5.5V
- Output voltage adjustable down to 0.7V
- Output load current up to 7A
- Full sequencing and tracking capability
- Power-on-Reset/Power Good output
- Efficiency > 95% across a broad load range
- Ultra-fast transient response
  - Easy RC compensation
- 100% maximum duty cycle
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current-limit protection
- 24-pin 4mm x 4mm MLF®
- –40°C to +125°C junction temperature range

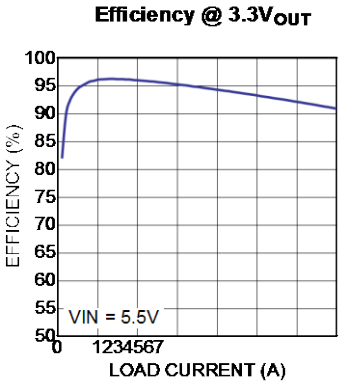
Applications

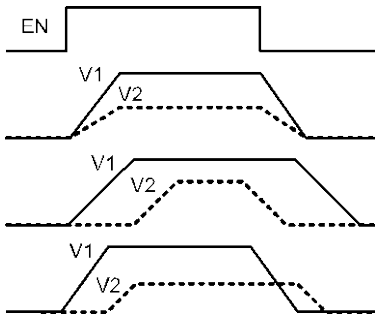
- High power density point-of-load conversion
- Servers and routers
- DVD recorders / Blu-Ray players
- Computing peripherals
- Base stations
- FPGAs, DSP and low voltage ASIC power

Typical Application



MIC22700 7A 1MHz Synchronous Output Converter





Sequencing & Tracking

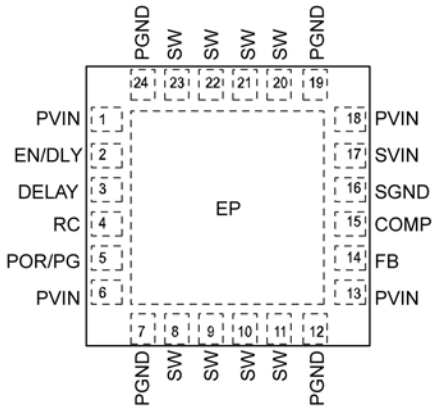
Ramp Control is a trademark of Micrel, Inc.
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

Ordering Information

Part Number	Voltage	Junction Temperature Range	Package	Lead Finish
MIC22700YML	Adjustable	–40° to +125°C	24-Pin 4mm x4mm MLF®	Pb-Free

Note: MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



24-Pin 4mm x 4mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Description
1, 6, 13, 18	PVIN	Power Supply Voltage (Input): Requires bypass capacitor to GND.
17	SVIN	Signal Power Supply Voltage (Input): Requires bypass capacitor-to-GND.
2	EN/DLY	Enable/Delay (Input): When this pin is pulled higher than the enable threshold, the part will start up. Below this voltage the device is in its low quiescent current mode. The pin has a 1µA current source charging it to VIN. By adding a capacitor to this pin a delay may easily be generated. The enable function will not operate with an input voltage lower than the min specified.
4	RC	Ramp Control: Capacitor to ground from this pin determines slew rate of output voltage during start-up. This can be used for tracking capability as well as soft start.
14	FB	Feedback: Input to the error amplifier, connect to the external resistor divider network to set the output voltage.
15	COMP	Compensation pin (Input): Place a RC to GND to compensate the device, see applications section.
5	POR/PG	Power On Reset (Output): Open-drain output device indicates when the output is out of regulation and is active after the delay set by the delay pin.
7, 12, 19, 24	PGND	Power Ground: Ground
16	SGND	Signal Ground: Ground
3	DELAY	Delay (Input): Capacitor to ground sets internal delay timer. Timer delays power-on reset (POR) output at turn-on and ramp down at turn-off.
8, 9, 10, 11, 20, 21, 22, 23	SW	Switch (Output): Internal power MOSFET output switches.
EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane for full output power to be realized.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... –0.3V to 6V
Output Switch Voltage (V_{SW}) ..... –0.3V to 6V
Output Switch Current (I_{SW}) ..... Internally Limited
Logic Input Voltage (V_{EN} V_{FLG}) ..... –0.3V to V_{IN}
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Rating[3] 2kV
Lead Temperature (Soldering 10s) ..... 260°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... 2.6V to 5.5V
Junction Temperature (T_J) ..... –40°C ≤ T_J ≤ +125°C
Thermal Resistance
4x4 MLF-24 (θ_{JC}) ..... 14°C/W
4x4 MLF-24 (θ_{JA}) ..... 40°C/W

Electrical Characteristics[4]

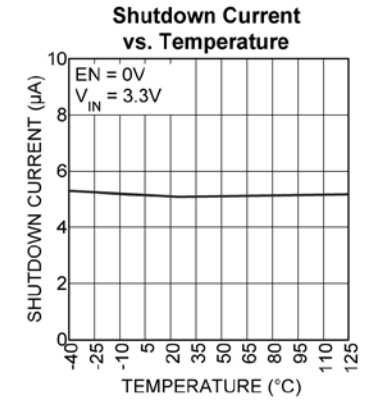
T_A = 25°C with V_{IN} = V_{EN} = 3.3V; V_{OUT} = 1.8V, unless otherwise specified. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

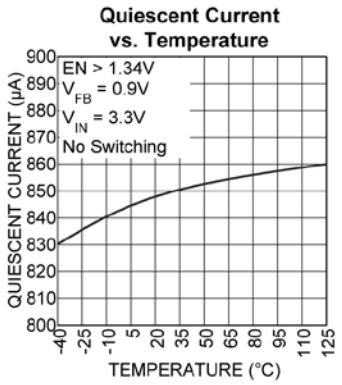
Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		**2.6**		**5.5**	V
Under-Voltage Lockout Threshold	(turn-on)	**2.4**	2.5	**2.6**	V
UVLO Hysteresis			280		mV
Quiescent Current, PWM Mode	V_{EN} =>1.34V; V_{FB} = 0.9V (not switching)		850	**1300**	µA
Shutdown Current	V_{EN} = 0V		5	**10**	µA
[Adjustable] Feedback Voltage	± 2% (over temperature)	**0.686**	0.7	**0.714**	V
FB Pin Input Current			1		nA
Current Limit	V_{FB} = 0.5	**7**	12.5	**16**	A
Output Voltage Line Regulation	V_{OUT} 1.8V; V_{IN} = 2.6 to 5.5V, I_{LOAD}= 100mA		0.2		%
Output Voltage Load Regulation	100mA < I_{LOAD} < 7A, V_{IN} = 3.3V		0.2		%
Maximum Duty Cycle	V_{FB} ≤ 0.5V	100			%
Switch ON-Resistance PFET Switch ON-Resistance NFET	I_{SW} = 1000mA; V_{FB}=0.5V I_{SW} = 1000mA; V_{FB}=0.9V		0.03 0.025		Ω Ω
Oscillator Frequency		0.8	1	1.2	MHz
EN/DLY Threshold Voltage		**1.14**	1.24	**1.34**	V
EN/DLY Source Current	V_{IN} = 2.6 to V_{IN} = 5.5V	**0.7**	1	**1.3**	µA
RC Pin I_{RAMP}	Ramp Control Current	**0.7**	1	**1.3**	µA
Power On Reset $I_{PG(LEAK)}$	V_{PORH} = 5.5V; POR = High			1 **2**	µA µA
Power On Reset $V_{PG(LO)}$	Output Logic-Low Voltage (undervoltage condition), I_{POR} = 5mA		130		mV
Power On Reset V_{PG}	Threshold, % of V_{OUT} below nominal	**7.5**	10	**12.5**	%
	Hysteresis		2		%
Over-Temperature Shutdown			160		°C
Over-Temperature Shutdown Hysteresis			20		°C

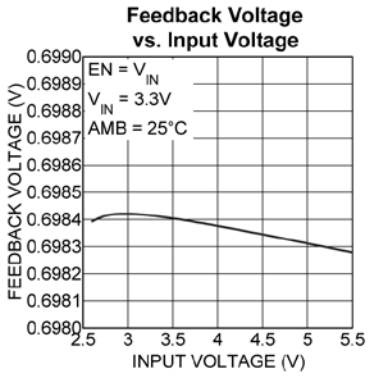
Notes:

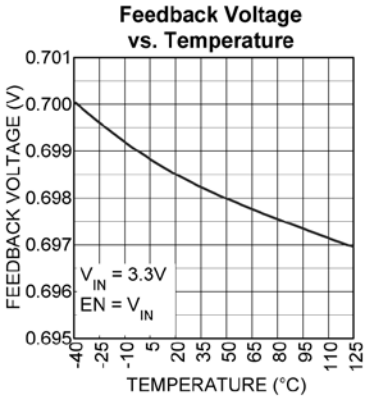
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Specification for packaged product only.

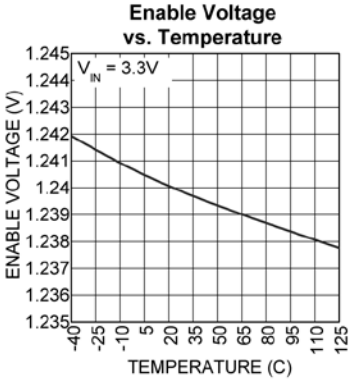
Typical Characteristics

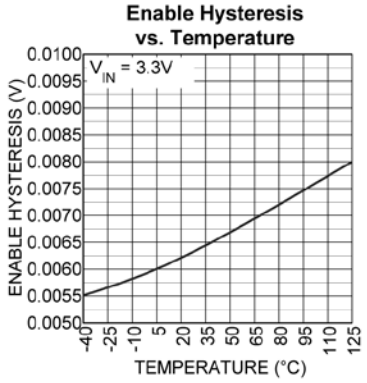


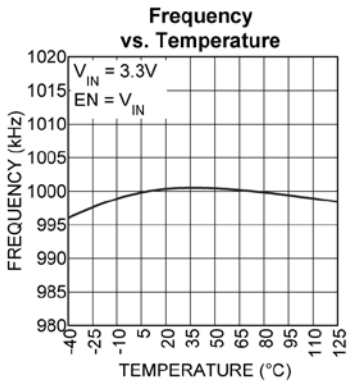


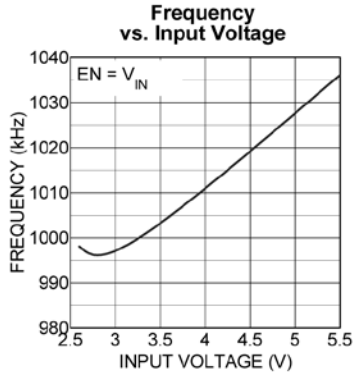


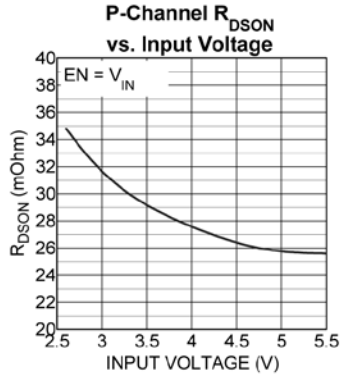


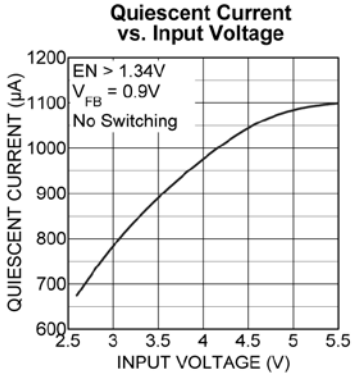


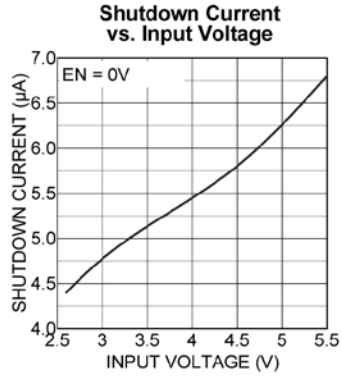






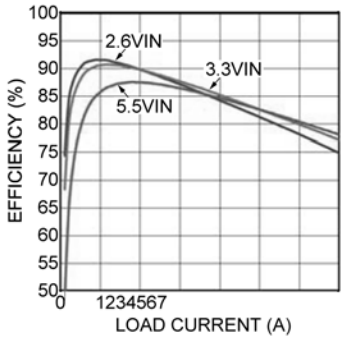




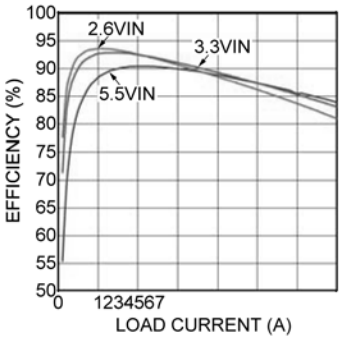


Typical Characteristics (continued)

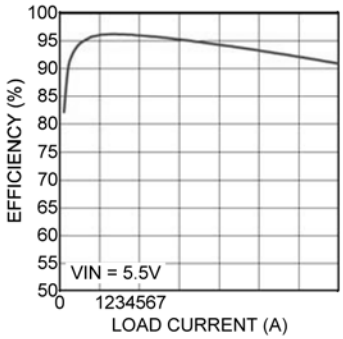
Efficiency @ 1.2V$_{OUT}$



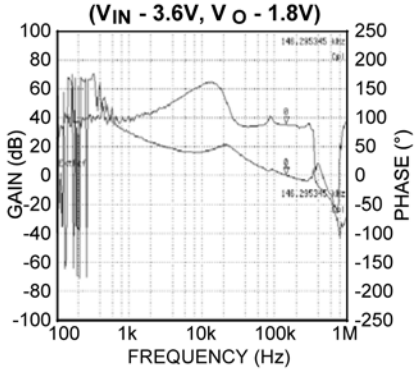
Efficiency @ 1.8V$_{OUT}$



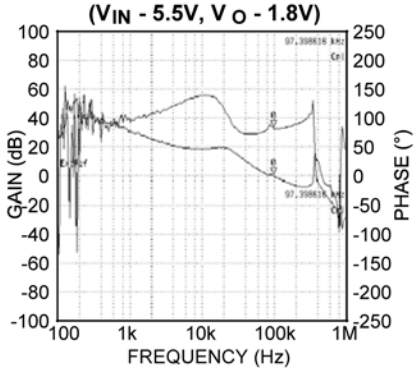
Efficiency @ 3.3V$_{OUT}$



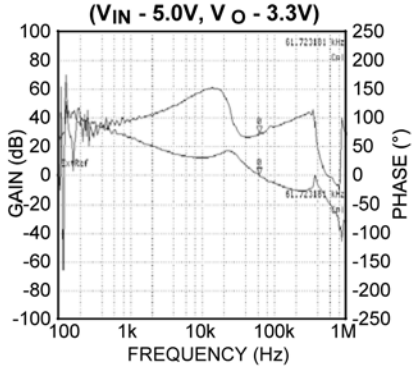
Bode Plot
(V$_{IN}$ - 3.6V, V$_O$ - 1.8V)



Bode Plot
(V$_{IN}$ - 5.5V, V$_O$ - 1.8V)

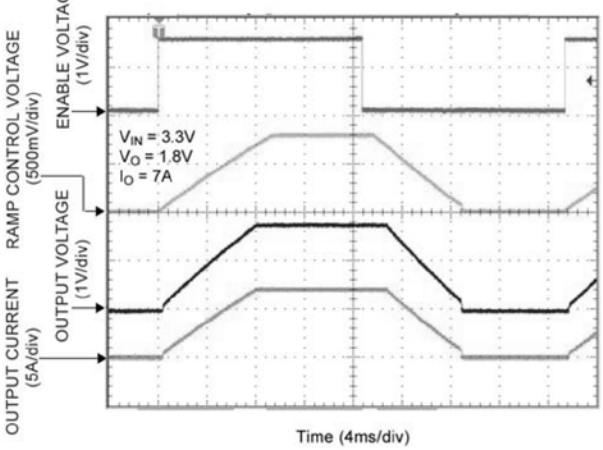


Bode Plot
(V$_{IN}$ - 5.0V, V$_O$ - 3.3V)

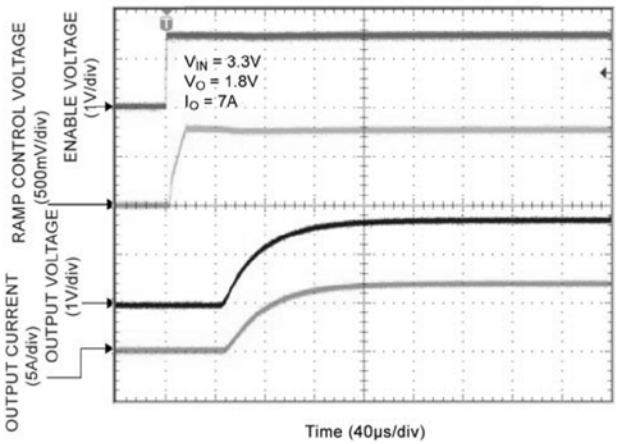


Functional Characteristics

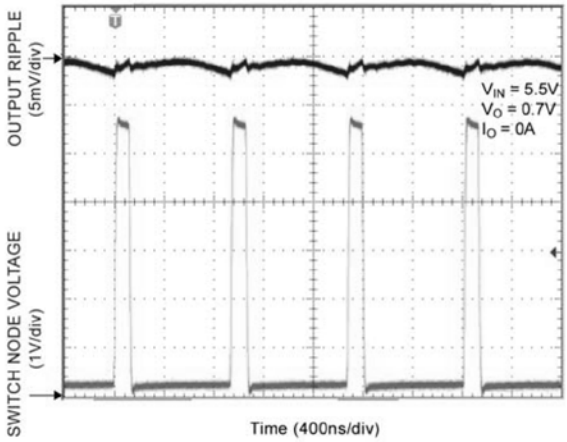
Start-Up/Shutdown (C_{RC} = 10nF)



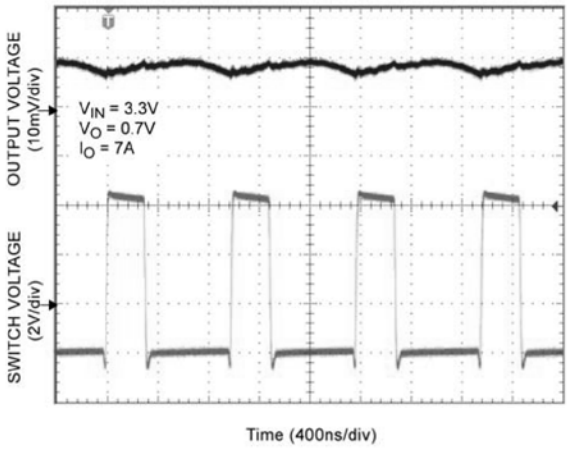
Start-Up (C_{RC} = 0nF)



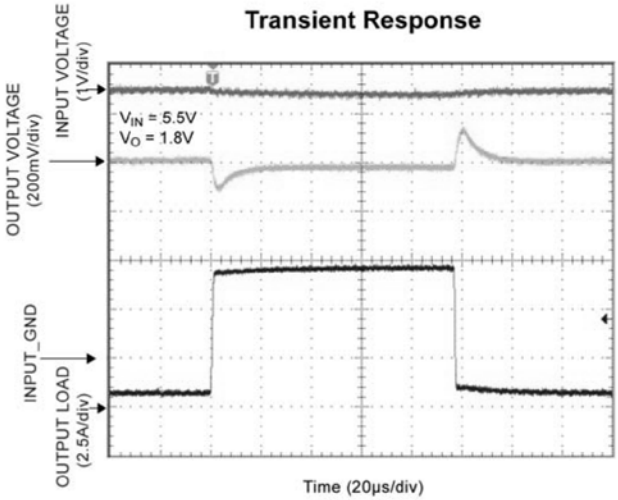
High DC Operation



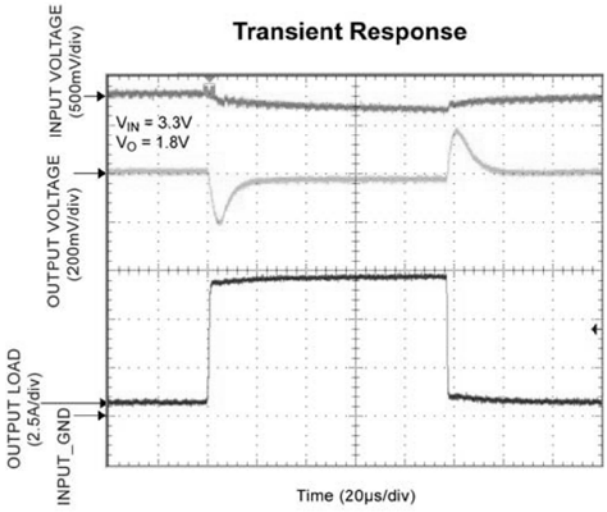
Switching Waveforms



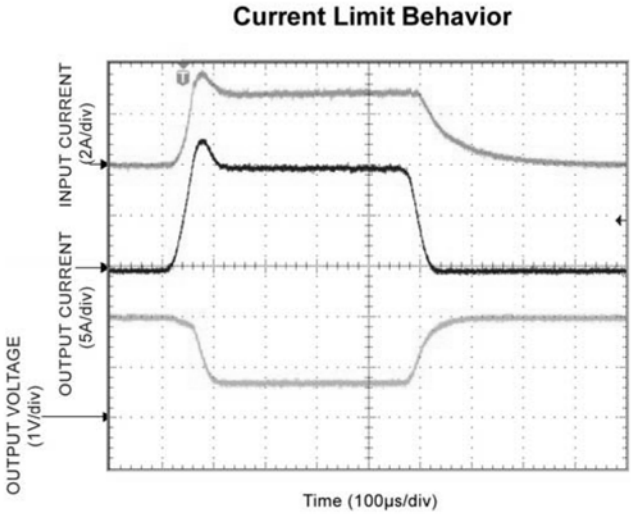
Transient Response

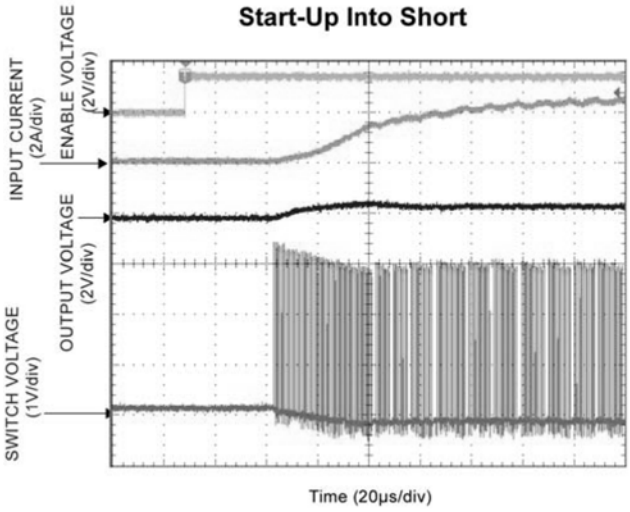


Transient Response



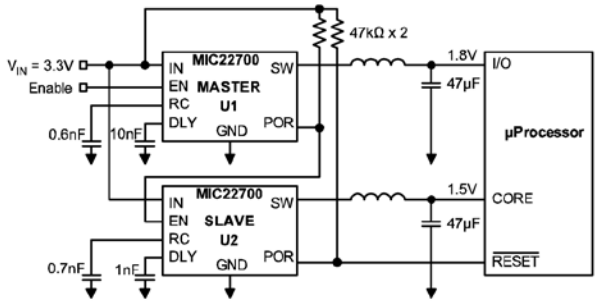
Functional Characteristics (continued)

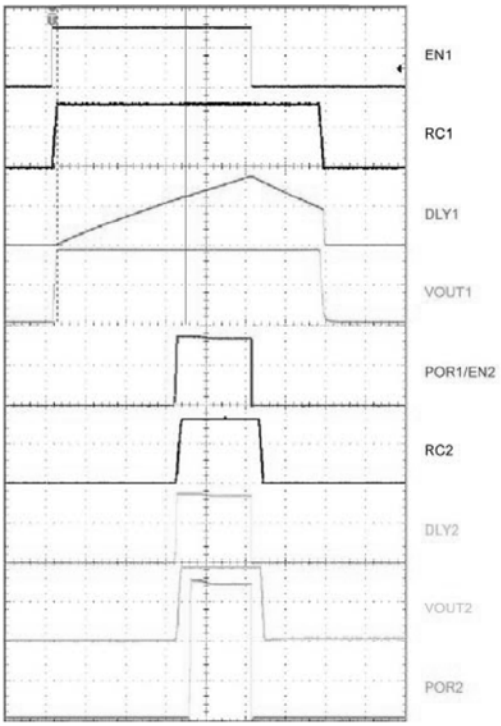




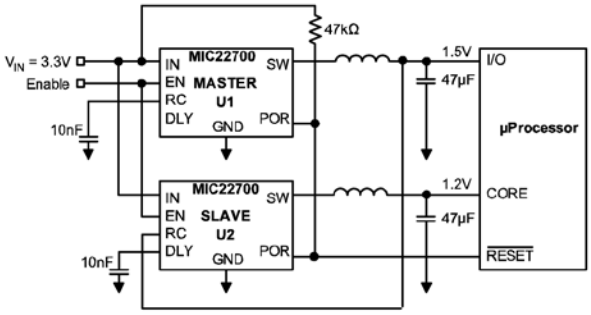
Typical Circuits and Waveforms

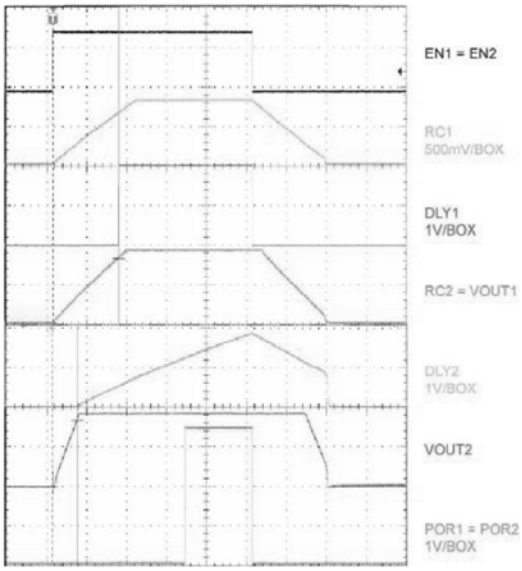
Sequencing Circuit and Waveform





Tracking Circuit and Waveform





Functional Diagram

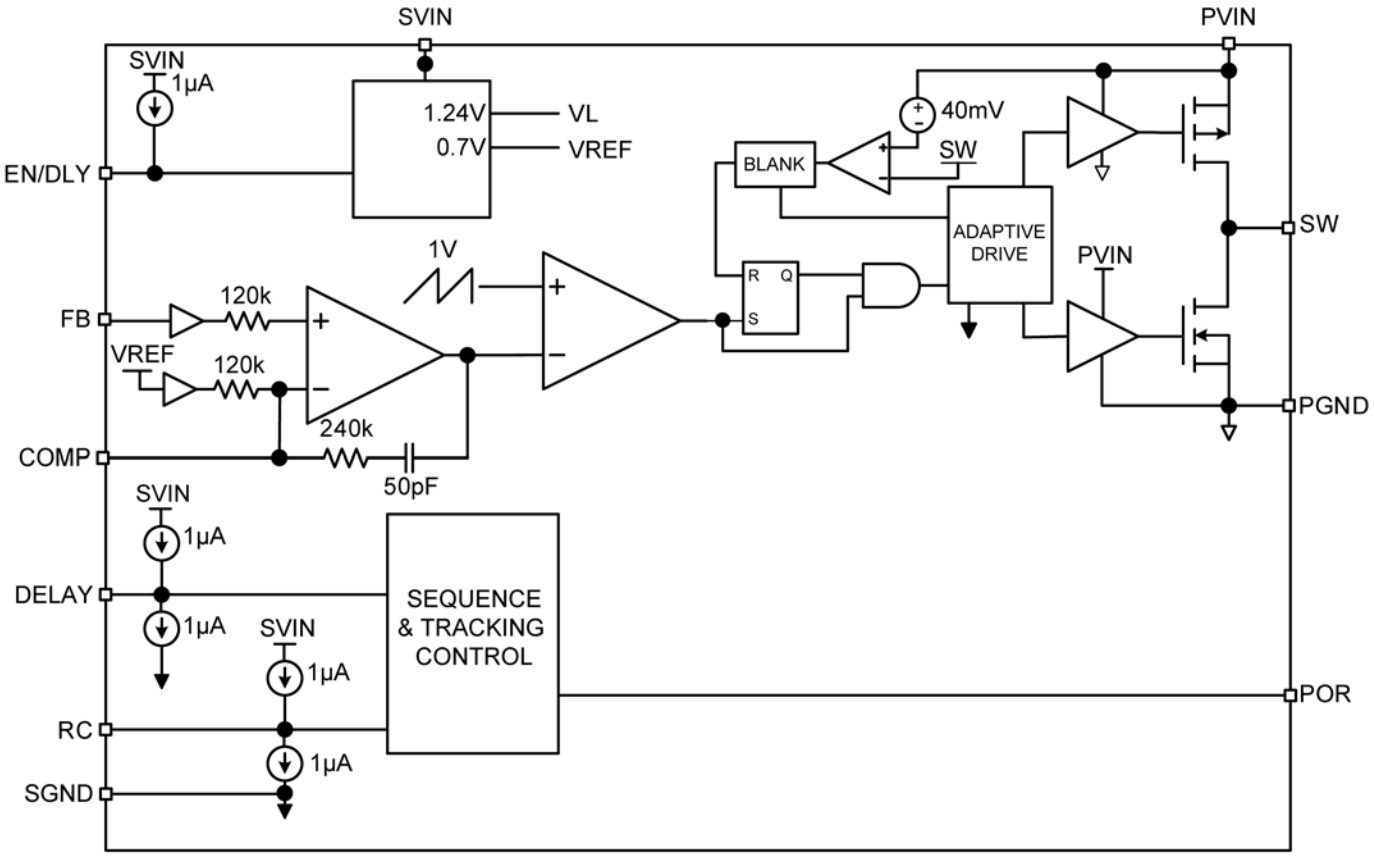


Figure 1. MIC22700 Block Diagram

Functional Description

PVIN, SVIN

PVIN is the input supply to the internal 30mΩ P-Channel Power MOSFET. This should be connected externally to the SVIN pin. The supply voltage range is from 2.6V to 5.5V. A 22µF ceramic is recommended for bypassing each PVIN supply.

EN/DLY

This pin is internally fed with a 1µA current source to VIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V.

RC

RC allows the slew rate of the output voltage to be programmed by the addition of a capacitor from RC to ground. RC is internally fed with a 1µA current source and VOUT slew rate is proportional to the capacitor and the 1µA source.

Delay

Adding a capacitor to this pin allows the delay of the POR signal.

When VOUT reaches 90% of its nominal voltage, the Delay pin current source (1µA) starts to charge the external capacitor. At 1.24V, POR is asserted high.

Comp

The MIC22700 uses an internal compensation network containing a fixed frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor will add the necessary pole and zero for voltage mode loop stability using low value, low ESR ceramic capacitors.

FB

The feedback pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the feedback section in the “Applications Information” for more detail.

POR

This is an open drain output. A 47.5kΩ resistor can be used for a pull up to this pin. POR is asserted high when output voltage reaches 90% of nominal set voltage and after the delay set by C_{DLY}. POR is asserted low without delay when enable is set low or when the output goes below the –10% threshold. For a Power Good (PG) function, the delay can be set to a minimum. This can be done by removing the Delay capacitor.

SW

This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high frequency high power connection; therefore traces should be kept as short and as wide as practical.

SGND

Internal signal ground for all low power sections.

PGND

Internal ground connection to the source of the internal N-Channel MOSFETs.

Application Information

The MIC22700 is a 7A Synchronous step down regulator IC with a fixed 1 MHz, voltage mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, power on reset.

Component selection

Input Capacitor

A minimum 22µF ceramic is recommended on each of the PVIN pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The MIC22700 was designed specifically for the use of ceramic output capacitors. 100µF can be increased to improve transient performance. Since the MIC22700 is in voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22700.

Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22700 is designed for use with a 0.47µH to 4.7µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the Current Limit of the MIC22700 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “Efficiency Considerations” below for a more detailed description.

Enable/DLY Capacitor

Enable/DLY sources 1µA out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1µA to charge C_{DLY} to 1.25V. Therefore:

$$T_{DLY} = \frac{1.24 \cdot C_{DLY}}{1 \times 10^{-6}}$$

Efficiency considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$Efficiency\ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time, critical in hand held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET $RDS_{(ON)}$ multiplied by the RMS Switch Current squared (I_{SW}^2). During the off cycle, the low side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor’s DCR and capacitor’s ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1MHz or 4MHz frequency and the switching transitions make up the switching losses.

Figure 2 shows an efficiency curve. The portion, from 0A to 1A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

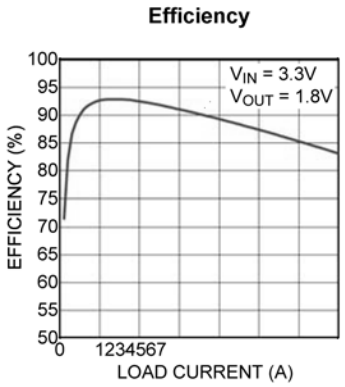


Figure 2. Efficiency Curve

The region, 1A to 7A, efficiency loss is dominated by MOSFET $RDS_{(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, reducing the internal $RDS_{(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$Efficiency\ Loss = \left[1 - \left(\frac{V_{OUT} \cdot I_{OUT}}{(V_{OUT} \cdot I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses.

The following graph in Figure 3 illustrates the effects of inductance value at light load.

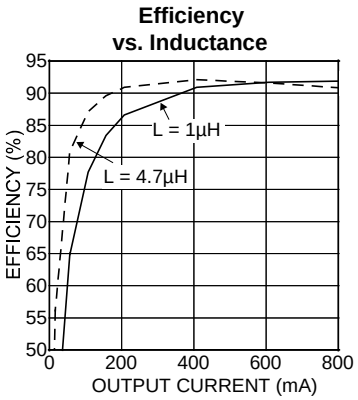


Figure 3. Efficiency vs. Inductance

Compensation

The MIC22700 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100-200kHz, the MIC22700 is capable of extremely fast transient responses.

The MIC22700 is designed to be stable with a typical application using a 1µH inductor and a 100µF ceramic (X5R) output capacitor. These values can be varied dependent upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency $\left(\frac{1}{2 \times \pi \times \sqrt{L \cdot C}}\right)$ ideally less than 26kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.47µH and minimum recommended output capacitor value is 22µF. The tradeoff between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20kΩ resistor) are shown below.

C→ / L↓	22-47µF	47µF-100µF	100µF-470µF
0.47µH	0*-10pF	22pF	33pF
1µH	0†-15pF	15-22pF	33pF
2.2µH	15-33pF	33-47pF	100-220pF
* VOUT > 1.2V, † VOUT > 1V			

Feedback

The MIC22700 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

where V_{REF} is 0.7V and V_{OUT} is the desired output voltage. A 10kΩ or lower resistor value from the output to the feedback is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

PWM Operation

The MIC22700 is a voltage mode, pulse width modulation (PWM) controller. By controlling the ratio of on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22700 will run at 100% duty cycle.

The MIC22700 provides constant switching at 1MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, very low power is dissipated during the off period.

PWM control provides fixed frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

Sequencing and tracking

The MIC22700 provides additional pins to provide up/down sequencing and tracking capability for connecting multiple voltage regulators together.

Enable/DLY pin

The Enable pin contains a trimmed, 1µA current source which can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20mV.

Delay Pin

The Delay pin also has a 1µA trimmed current source and a 1µA current sink which acts with an external capacitor to delay the operation of the Power On Reset (POR) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After Enable is driven high, V_{OUT} will start to rise (rate determined by RC capacitor). As the FB voltage goes above 90% of its nominal set voltage, Delay begins to rise as the 1µA source charges the external capacitor. When the threshold of 1.24V is crossed, POR is asserted high and Delay continues to charge to a voltage V_{DD}. When FB falls below 90% of nominal, POR is asserted low immediately. However, if enable is driven low, POR will fall immediately to the low state and Delay will begin to fall as the external capacitor is discharged by the 1µA current sink. When the threshold of V_{DD}-1.24V is crossed, V_{OUT} will begin to fall at a rate determined by the RC capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at $T_{POR} = \frac{1.24 \cdot C_{DLY}}{1 \times 10^{-6}}$

RC pin

The RC pin provides a trimmed 1µA current source/sink similar to the Delay Pin for accurate ramp up (soft start) and ramp down control. This allows the MIC22700 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

1. Externally driven from a voltage source
2. Externally attached capacitor sets output ramp up/down rate

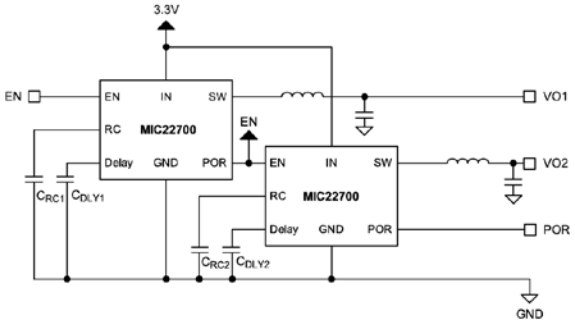
In the first case, driving RC with a voltage from 0V to V_{REF} will program the output voltage between 0 and 100% of the nominal set voltage.

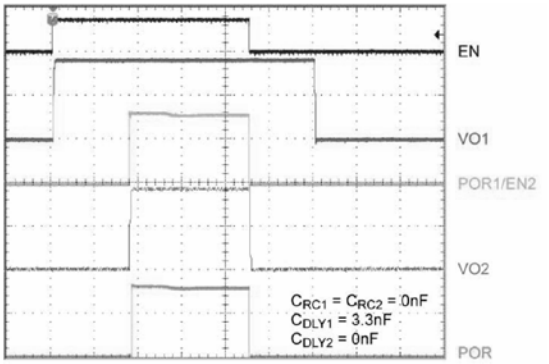
In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time is given by $T_{RAMP} = \frac{0.7 \cdot C_{RC}}{1 \times 10^{-6}}$ where T_{RAMP} is the time from 0 to 100% nominal output voltage.

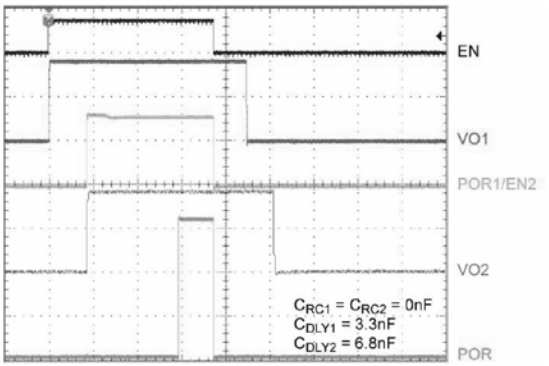
Sequencing & Tracking examples

There are four distinct variations which are easily implemented using the MIC22700. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22700's to achieve these requirements.

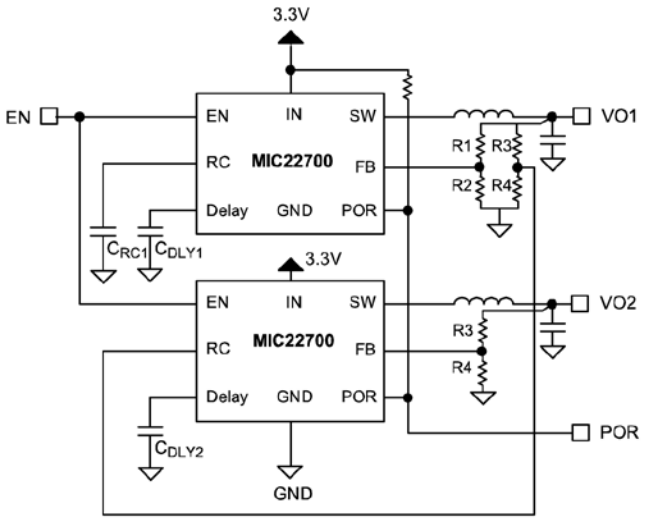
Sequencing:

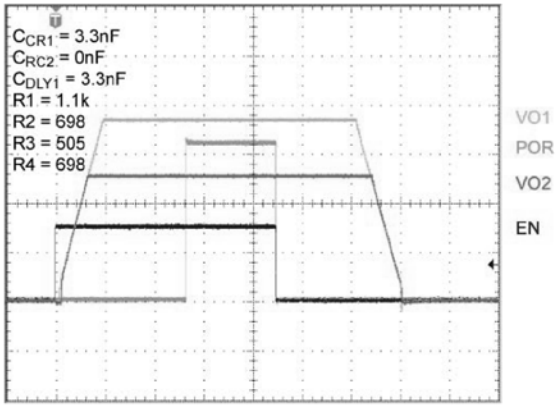




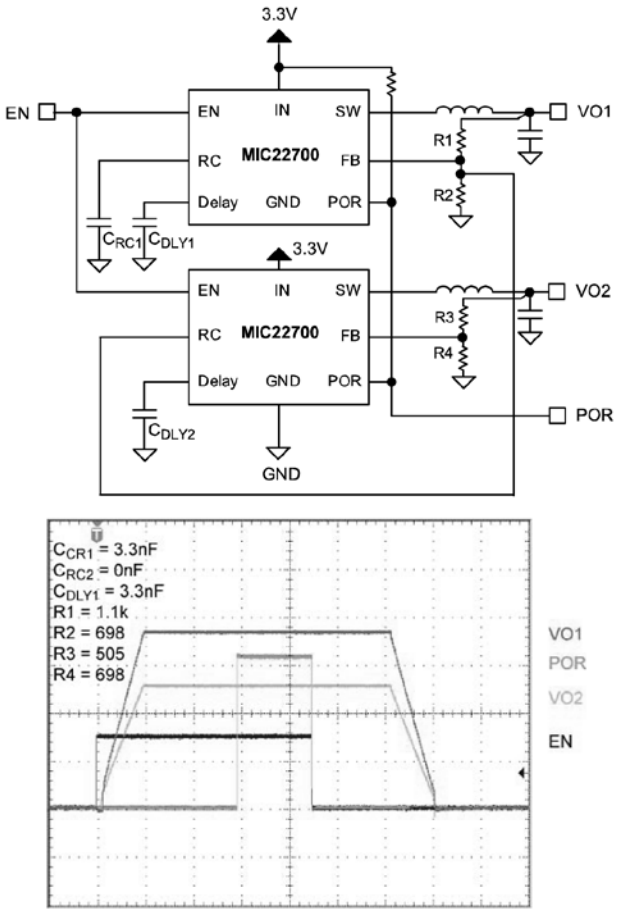


Normal Tracking:

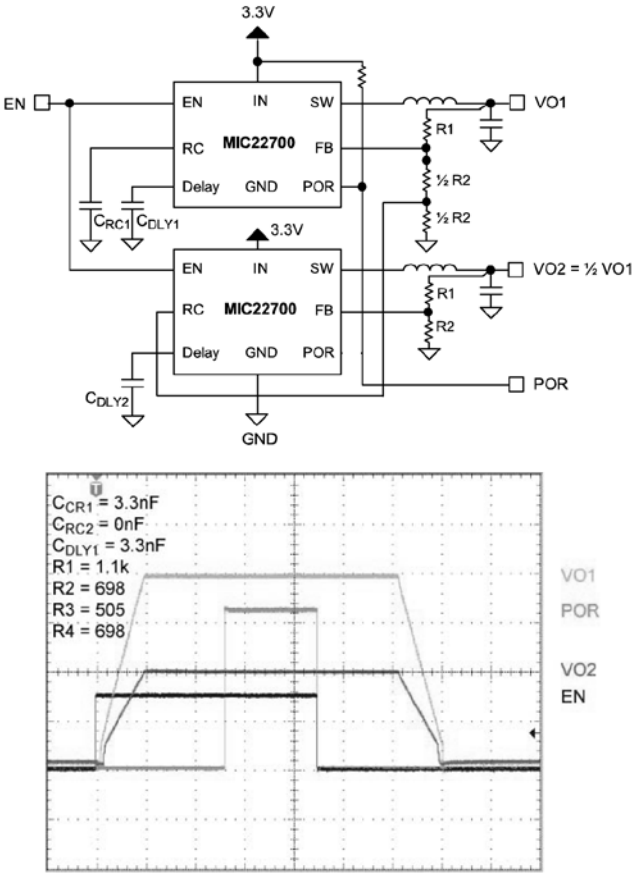




Ratio Metric Tracking:



An alternative method here shows an example of a V_{DDQ} and V_{TT} solution for a DDR memory power supply. Note that POR is taken from Vo1 as POR_2 will not go high. This is because POR is set high when FB > $0.9 \cdot V_{REF}$. In this example, FB_2 is regulated to $½ \cdot V_{REF}$:



Current Limit

The MIC22700 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is over temperature shutdown.

Current is limited by measuring the current through the high side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 4 describes the operation of the current limit circuit. Since the actual RDS_{ON} of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependent upon the RDS_{ON} value. Current limit is set to nominal value. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

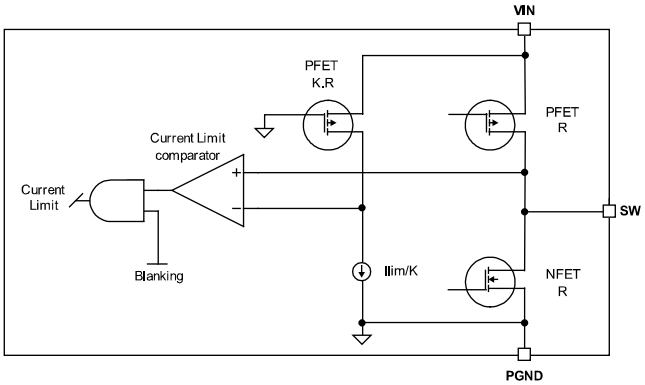


Figure 4. Current Limit Detail

Thermal Considerations

The MIC22700 is packaged in the MLF® 4mm x 4mm, a package that has excellent thermal performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_{AMB} + P_{DISS} \cdot R\theta_{JA}$$

Where:

- P_{DISS} is the power dissipated within the MLF® package and is typically 1.5W at 7A load. This has been calculated for a 1µH inductor and details can be found in table 1 below for reference.

- $R\theta_{JA}$ is a combination of junction to case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane to ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.

VIN→ / VOUT @7A↓	2.6V	3.3V	3.6V	4.5V	5.5V
0.7V	2.073	1.884	1.836	1.784	1.791
1.2V	2.133	1.896	1.853	1.786	1.796
1.8V	2.207	1.934	1.873	1.814	1.826
2.5V	—	1.953	1.881	1.797	1.803
3.3V	—	—	1.423	1.79	1.789

Table 1. Power Dissipation (W) for 7A output

- T_{AMB} is the Operating Ambient temperature.

Example:

The Evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the MLF 4x4 is 14°C/W.

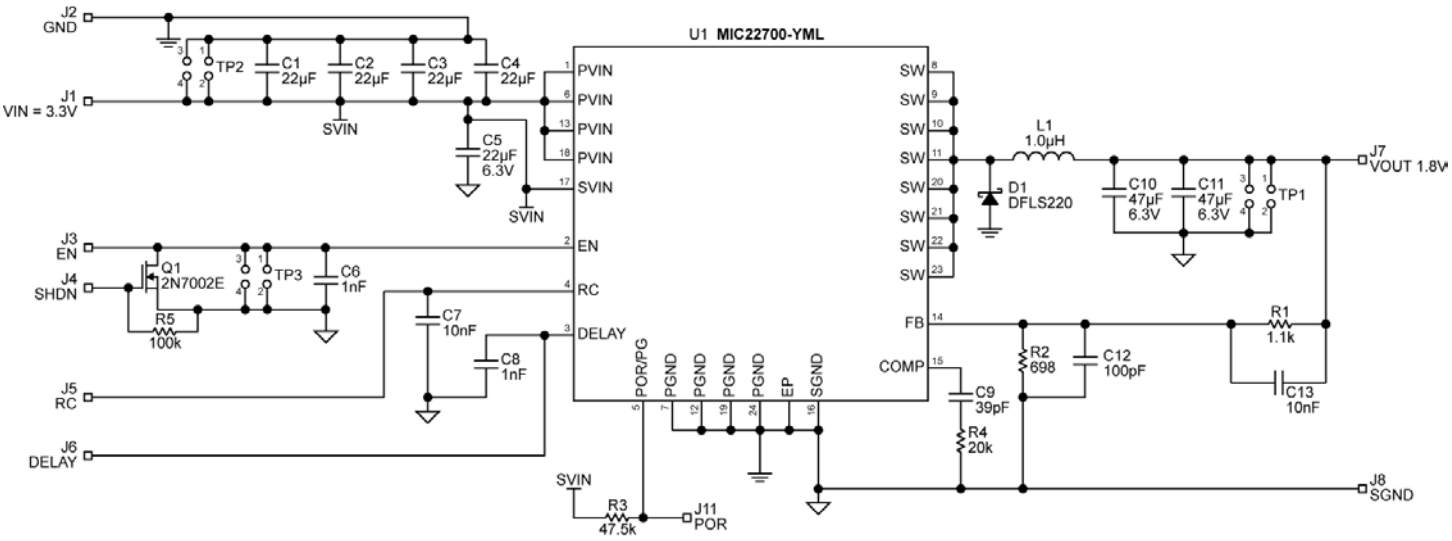
$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$
$$R\theta_{JA} = 14 + 25 = 39^oC/W$$

To calculate the junction temperature for a 50°C ambient:

$$T_J = T_{AMB} + P_{DISS} \cdot R\theta_{JA}$$
$$T_J = 50 + (1.5 \times 39)$$
$$T_J = 109°C$$

This is below the maximum of 125°C.

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4, C5	C2012X5R0J226M	TDK[1]	22µF/6.3V, 0805, Ceramic Capacitor	5
	08056D226MAT	AVX[2]		
	GRM21BR60J226ME39L	Murata[3]		
C7, C13	GRM188R71H103KA01D	Murata	10nF, 0603, Ceramic Capacitor	1
C6	Open(VJ0603Y102KXQCW1BC)	Vishay[4]	1nF, 0603, Ceramic Capacitor	1
	Open(GRM188R71H102KA01D)	Murata	1000pF/50V, X7R, 0603, Ceramic Capacitor	
	Open(C1608C0G1H102J)	TDK	1000pF/50V, COG, 0603, Ceramic Capacitor	
C8	VJ0603Y102KXQCW1BC	Vishay	1nF, 0603, Ceramic Capacitor,	1
	GRM188R71H102KA01D	Murata	1000pF/50V, X7R, 0603, Ceramic Capacitor	
	C1608C0G1H102J	TDK	1000pF/50V, COG, 0603, Ceramic Capacitor	
C9	GRM1555C1H390JZ01D	Murata	39pF/50V, COG, 0402, Ceramic Capacitor	1
	VJ0402A390KXQCW1BC	BC Components[5]	39pF /10V, 0402, Ceramic Capacitor	
C10, C11	C3216X5R0J476M	TDK	47µF/6.3V, X5R, 1206, Ceramic Capacitor	2
	GRM31CR60J476ME19	Murata	47µF/6.3V, X5R, 1206, Ceramic Capacitor	
	GRM31CC80G476ME19L	Murata	47µF/4V, X6S, 1206, Ceramic Capacitor	
C12	VJ0402A101KXQCW1BC	Vishay	100pF, 0603, Ceramic Capacitor	1
	GRM1555C1H101JZ01D	Murata	100pF/50V, COG, 0402, Ceramic Capacitor	
D1	SS2P2L	Vishay	Schottky Diode, 2A, 20V	1
	DFLS220	Diodes, Inc.[6]		
L1	SPM6530T-1R0M120	TDK	1µH, 12A, size 7x6.5x3mm	1
	HCP0704-1R0-R	Coiltronics[7]	1µH, 12A, size 6.8x6.8x4.2mm	

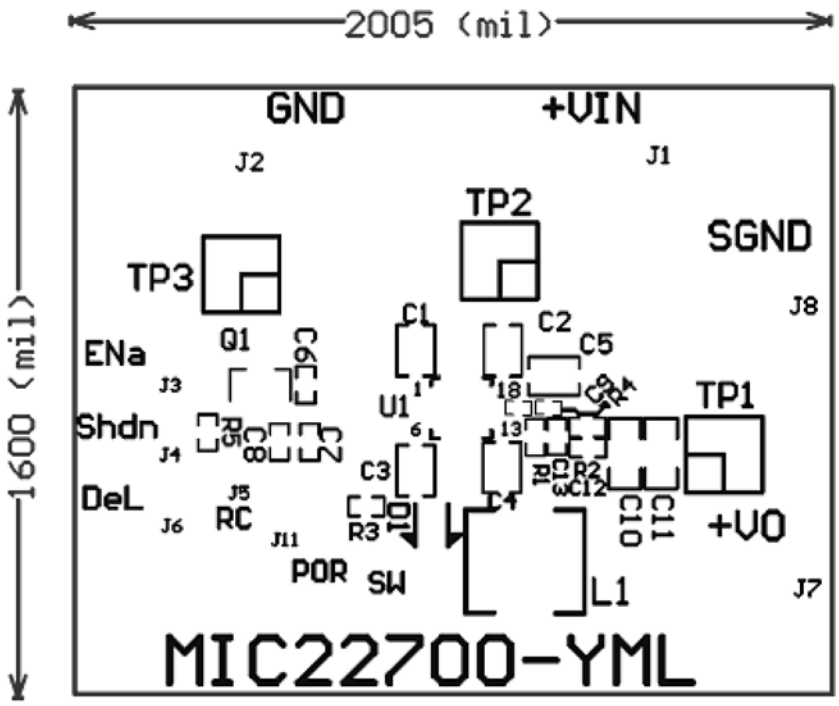
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R1	CRCW06031101FKEYE3	Vishay	Resistor, 1.1kΩ, 0603, 1%	1
R2	CRCW04026980FKEYE3	Vishay	Resistor, 698Ω, 0603, 1%	1
R3	CRCW06034752FKEYE3	Vishay	Resistor, 47.5kΩ, 0603, 1%	1
R4	CRCW04022002FKEYE3	Vishay	Resistor, 20kΩ, 0402, 1%	1
R5	Open(CRCW06031003FRT1)	Vishay	Resistor, 100kΩ, 0603, 1%	1
Q1	Open(2N7002E)	Vishay	Signal MOSFET – SOT-23-6	1
	Open(CMDPM7002A)	Central Semiconductor[8]		
U1	**MIC22700YML**	**Micrel[9]**	**Integrated 7A Synchronous Buck Regulator**	**1**

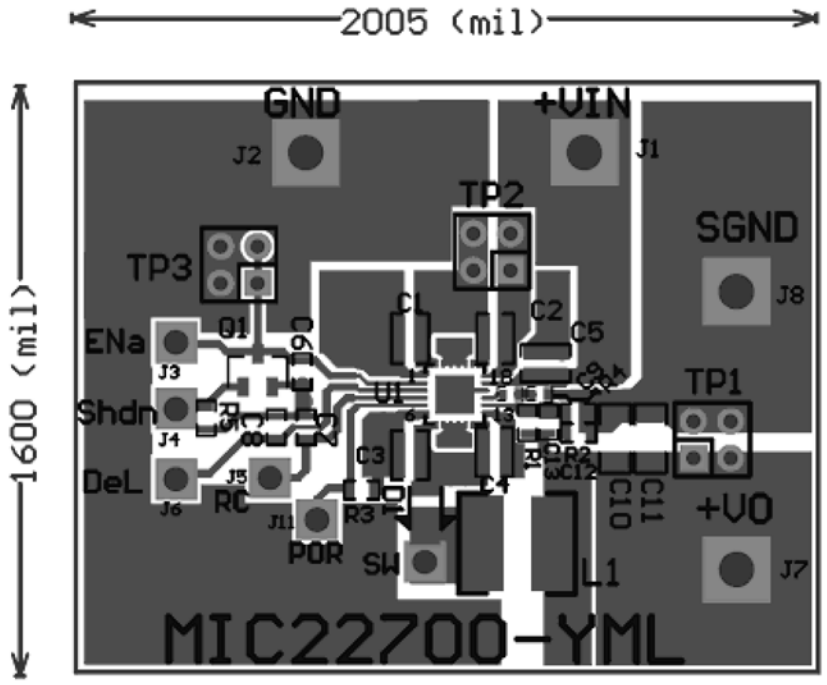
Notes:

1. TDK: www.tdk.com
2. AVX: www.avx.com
3. Murata: www.murata.com
4. Vishay: www.vishay.com
5. This part is now available through Vishay.
6. Diodes, Inc.: www.diodes.com
7. Coiltronics: www.coiltronics.com
8. Central Semiconductor: www.centralsemi.com
9. **Micrel, Inc.: www.micrel.com**

PCB Layout Recommendations



Top Silk



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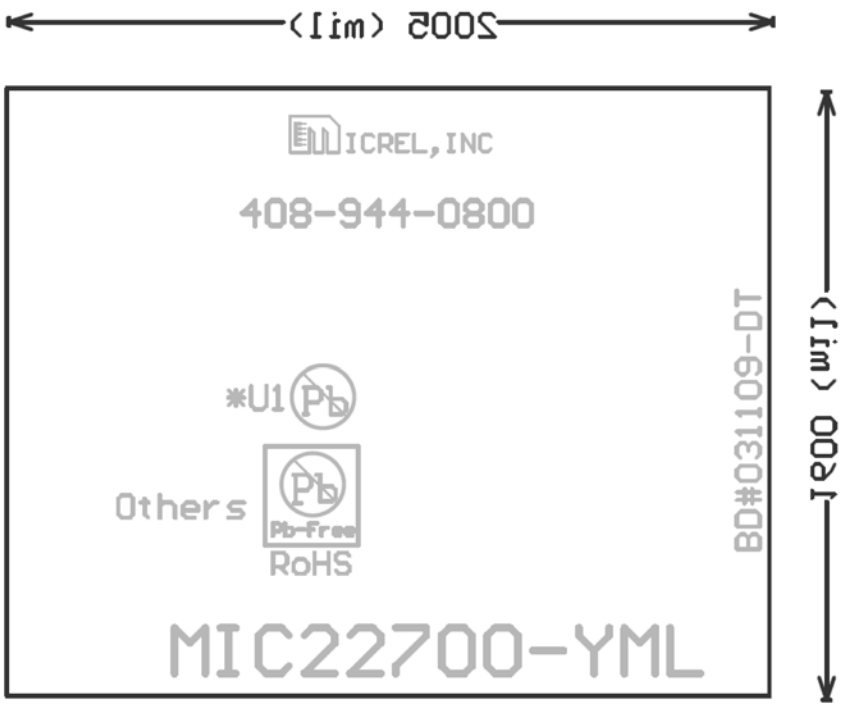
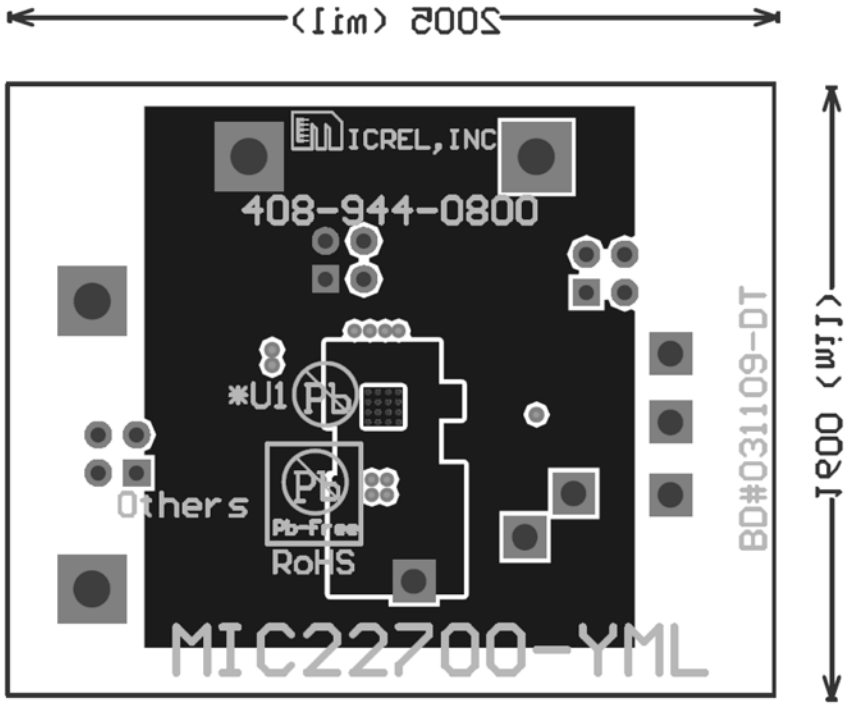
PCB Layout Recommendations (Continued)

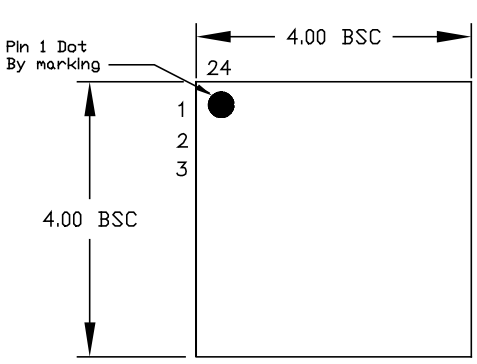


Bottom Silk

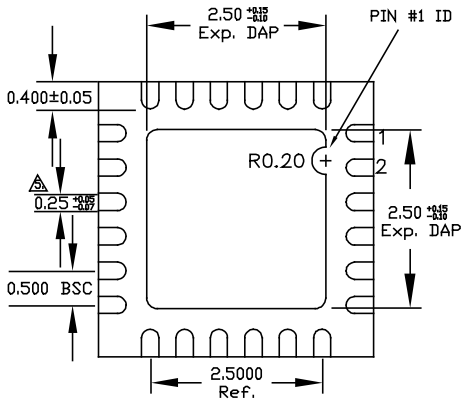


Bottom Layer

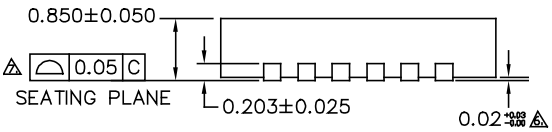
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin 4mm x 4mm MLF® (ML)

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