HV513

8-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, Polarity, Hi-Z and Short-Circuit Detect

Features

- Up to 250V Output Voltage
- Low-Power Level Shifting from 5V to 250V
- Shift Register Speed:
  - 8 MHz at V_{DD} = 5V
- Latched Data Outputs
- Output Polarity and Blanking
- Output Short-Circuit Detect
- Output High-Z (Hi-Z) Control
- CMOS-Compatible Inputs

Applications

- Piezoelectric Transducer Driver
- Braille Driver
- Weaving Applications
- Printer Drivers
- Microelectromechanical Systems Applications
- Displays

General Description

The HV513 is a low-voltage-to-high-voltage serial-to-parallel converter with eight high-voltage push-pull outputs. This device is designed to drive small capacitive loads such as piezoelectric transducers. It can also be used in any application requiring multiple high-voltage outputs with medium-current source-and-sink capabilities.

The device consists of an 8-bit Shift register, eight latches and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the Shift register on the low-to-high transition of the clock. A data output buffer is provided for cascading devices. The operation of the Shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$), polarity ($\overline{POL}$) and $\overline{Hi\text{-}Z}$ control inputs. The transfer of data from the Shift register to the latch occurs when the $\overline{LE}$ is high. The data in the latch is stored when $\overline{LE}$ is low. A $\overline{Hi\text{-}Z}$ pin is provided to set all the outputs in a High-Z state.

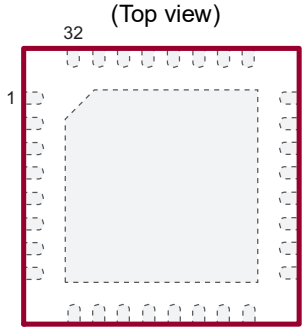
All outputs have short-circuit protection that detects if the outputs have reached the required output state. If an output does not track the required state, then the $\overline{SHORT}$ pin will be low. This output will pulse low during the output transition period under normal operation. See Figure 3-2 for details.

All outputs will have a break-before-make circuitry to reduce crossover current during output state changes.

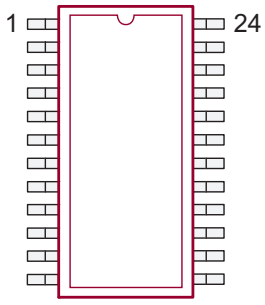
The $\overline{POL}$, $\overline{BL}$, $\overline{LE}$ and $\overline{Hi\text{-}Z}$ inputs have an internal pull-up resistor.

Package Types

32-lead QFN
(Top view)

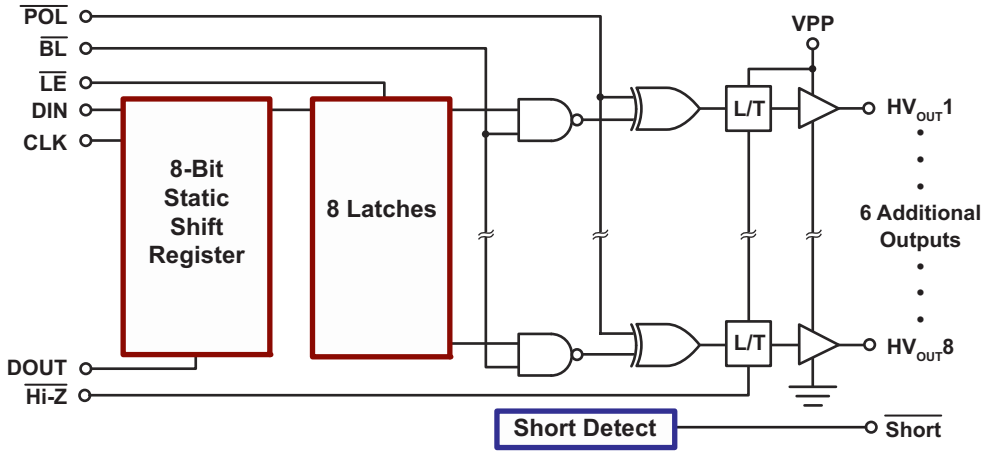


24-lead SOW
(Top view)



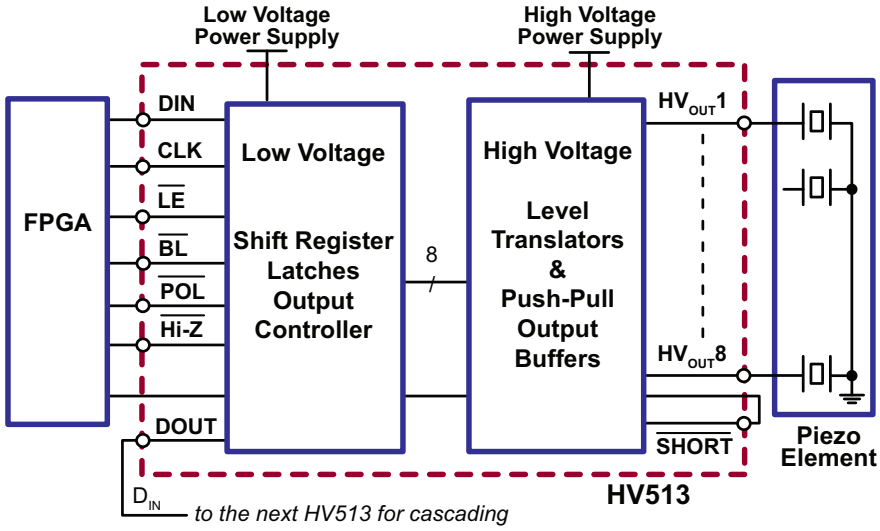
See Table 2-1 and Table 2-2 for pin information.

Functional Block Diagram



Note 1: $\overline{POL}$, $\overline{BL}$, $\overline{LE}$ and $\overline{Hi\text{-}Z}$ have internal 20 kΩ pull-up resistors.

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage, V_{DD} ..... –0.5V to +6V
High-Voltage Supply, V_{PP} ..... V_{DD} to +275V
Logic Input Levels ..... –0.5V to V_{DD} +0.5V
Ground Current (**Note 1**) 0.3A
High-Voltage Supply Current (**Note 1**) 0.25A
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
32-lead QFN (**Note 2**) ..... 750 mW
24-lead SOW (**Note 2**) ..... 750 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
2: For operations above 25°C ambient, derate linearly to 85°C at 12 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V	
High-Voltage Supply Voltage	V_{PP}	50	—	250	V	**Note 1**
High-Level Input Voltage	V_{IH}	V_{DD}–0.9V	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.9	V	
Operating Junction Temperature	T_J	–40	—	+85	°C	

Note 1: The output may not switch below the minimum V_{PP}.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over typical operating conditions unless otherwise specified, T_J = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current		I_{DD}	—	—	4	mA	f_{CLK} = 8 MHz, $\overline{LE}$ = Low
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	0.1	mA	All V_{IN} = V_{DD}
			—	—	2	mA	All V_{IN} = 0V
High-Voltage Supply Current		I_{PP}	—	—	100	µA	V_{PP} = 250V, f_{OUT} = 300 Hz, no load
Quiescent V_{PP} Supply Voltage		I_{PPQ}	—	—	100	µA	V_{PP} = 240V, outputs are static
High-Level Logic Input Current		I_{IH}	—	—	10	µA	V_{IH} = V_{DD}
Low-Level Logic Input Current		I_{IL}	—	—	–10	µA	V_{IL} = 0V
			—	—	–350	µA	V_{IL} = 0V, for inputs with pull-up resistors
High-Level Output	HV_{OUT}	V_{OH}	140	—	—	V	V_{PP} = 200V, I_{HVOUT} = –20 mA
	Data Out		V_{DD} –1V	—	—	V	I_{DOUT} = –0.1 mA
Low-Level Output	HV_{OUT}	V_{OL}	—	—	60	V	V_{DD} = 4.5V, I_{HVOUT} = 20 mA
	Data Out		—	—	1	V	I_{DOUT} = –0.1 mA

AC ELECTRICAL CHARACTERISTICS

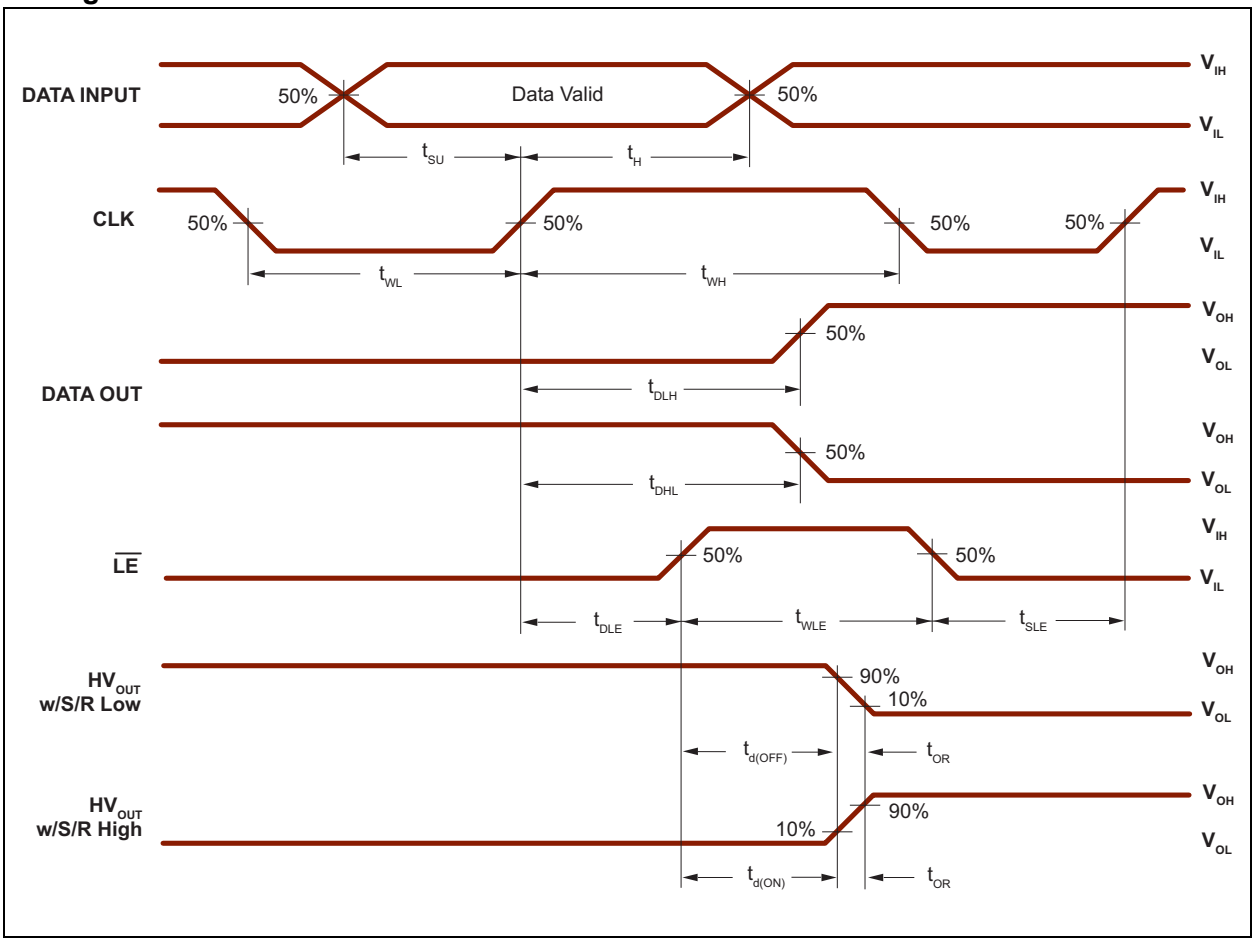
Electrical Specifications: Over typical operating conditions unless otherwise specified, T_J = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	0	—	8	MHz	
Output Switching Frequency (SOA Limited)	f_{OUT}	—	300	—	Hz	C_L = 50 nF, V_{PP} = 200V
Clock Width High and Low	t_{WL}, t_{WH}	62	—	—	ns	
Data Set-Up Time before Clock Rises	t_{SU}	15	—	—	ns	
Data Hold Time after Clock Rises	t_H	30	—	—	ns	
Latch Enable Pulse Width	t_{WLE}	80	—	—	ns	
Latch Enable Delay Time after Rising Edge of Clock	t_{DLE}	35	—	—	ns	
Latch Enable Set-Up Time before Clock Rises	t_{SLE}	40	—	—	ns	
HV_{OUT} Rise/Fall Time	t_{OR}, t_{OF}	—	—	1000	µs	C_L = 100 nF, V_{PP} = 200V
Delay Time for Output to Start Rise/Fall	$t_{dON/OFF}$	—	—	500	ns	
Delay Time Clock to Data Low to High	t_{DLH}	—	—	110	ns	C_L = 15 pF
Delay Time Clock to Data High to Low	t_{DHL}	—	—	110	ns	C_L = 15 pF
All Logic Inputs	t_r, t_f	—	—	5	ns	
Output Short-Circuit Detection	t_{SD}	—	—	500	ns	C_L = 15 pF, short to output fall of $\overline{SHORT}$
Output Short-Circuit Clear	t_{SC}	—	—	3000	ns	$\overline{Short}$ clear to output rise of $\overline{SHORT}$
Output High-Z State	t_{HI-Z}	—	—	500	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
32-lead QFN	θ_{JA}	—	22	—	°C/W	
24-lead SOW	θ_{JA}	—	44	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV513 32-lead QFN and 24-lead SOW packages are listed in Table 2-1 and Table 2-2, respectively. Refer to **Package Types** for the location of pins.

TABLE 2-1: 32-LEAD QFN PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	No connection
2	NC	No connection
3	NC	No connection
4	LGND	Low-voltage ground
5	HVGND	High-voltage ground
6	HVGND	High-voltage ground
7	NC	No connection
8	NC	No connection
9	HVOUT1	High-voltage push-pull output
10	HVOUT2	High-voltage push-pull output
11	HVOUT3	High-voltage push-pull output
12	HVOUT4	High-voltage push-pull output
13	HVOUT5	High-voltage push-pull output
14	HVOUT6	High-voltage push-pull output
15	HVOUT7	High-voltage push-pull output
16	HVOUT8	High-voltage push-pull output
17	NC	No connection
18	NC	No connection
19	VPP	High-voltage supply
20	VPP	High-voltage supply
21	VDD	Logic supply voltage
22	DOUT	Data output
23	NC	No connection
24	NC	No connection
25	$\overline{BL}$	Blanking. A logic input low sets all HVOUTs low.
26	NC	No connection
27	$\overline{POL}$	Polarity bar input logic
28	CLK	Clock. Shift registers shift data on the rising edge of input clock.
29	$\overline{LE}$	Latch enable bar input logic
30	$\overline{SHORT}$	If output does not reach its required state, a logic '0' will be asserted at the $\overline{SHORT}$ pin.
31	$\overline{Hi\text{-}Z}$	High-impedance pin. Logic input low sets all outputs in a High-impedance state.
32	DIN	Data input
Center Pad		Center Pad is at V_{PP} potential. Connect to VPP or leave floating.

TABLE 2-2: 24-LEAD SOW PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	No connection
2	VDD	Logic supply voltage
3	DOUT	Data output
4	$\overline{BL}$	Blanking. A logic input low sets all HVOUTs low.
5	$\overline{POL}$	Polarity bar input logic
6	CLK	Clock. Shift registers shift data on the rising edge of input clock.
7	$\overline{LE}$	Latch enable bar input logic
8	$\overline{SHORT}$	If output does not reach its required state, a logic '0' will be asserted at the $\overline{SHORT}$ pin.
9	$\overline{Hi\text{-}Z}$	High-impedance pin. Logic input low sets all outputs in a high-impedance state.
10	DIN	Data input
11	LGND	Low-voltage ground
12	NC	No connection
13	HVGND	High-voltage ground
14	HVGND	High-voltage ground
15	HVOUT1	High-voltage push-pull output
16	HVOUT2	High-voltage push-pull output
17	HVOUT3	High-voltage push-pull output
18	HVOUT4	High-voltage push-pull output
19	HVOUT5	High-voltage push-pull output
20	HVOUT6	High-voltage push-pull output
21	HVOUT7	High-voltage push-pull output
22	HVOUT8	High-voltage push-pull output
23	VPP	High-voltage supply
24	VPP	High-voltage supply

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV513.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove V_{PP}.
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove V_{DD}.
4	Apply V_{PP}.	4	Disconnect ground.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs				
							Shift Register		High-Voltage Output		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	$\overline{Hi\text{-}Z}$	1	2...8	1	2...8	*
All On	X	X	X	L	L	H	*	*...*	H	H...H	*
All Off	X	X	X	L	H	H	*	*...*	L	L...L	*
Invert Mode	X	X	L	H	L	H	*	*...*	$\overline{*}$	$\overline{*}$...$\overline{*}$	*
Load S/R	H or L	↑	L	H	H	H	H or L	*...*	*	*...*	*
Store Data in Latches	X	X	L	H	H	H	*	*...*	*	*...*	*
	X	X	L	H	L	H	*	*...*	$\overline{*}$	$\overline{*}$...$\overline{*}$	*
Transparent Latch Mode	L	↑	H	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	H	*...*	H	*...*	*
Outputs Hi-Z	X	X	X	X	X	L	*	*...*	High-impedance outputs		*
Outputs On	X	X	X	X	X	H	*	*...*	*	*...*	*

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↑ = Low-to-high transition
* = Dependent on the previous stage's state before the last CLK or last $\overline{LE}$ high

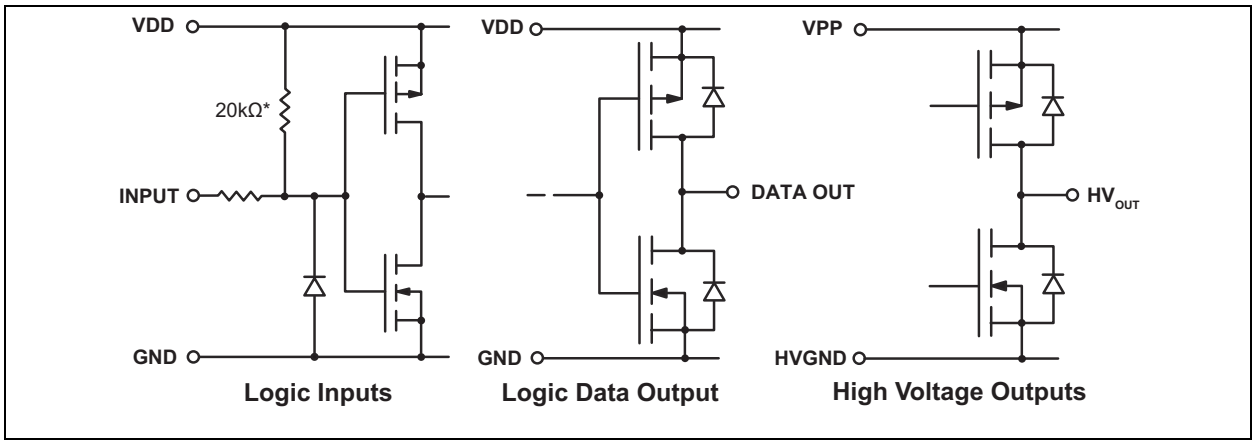
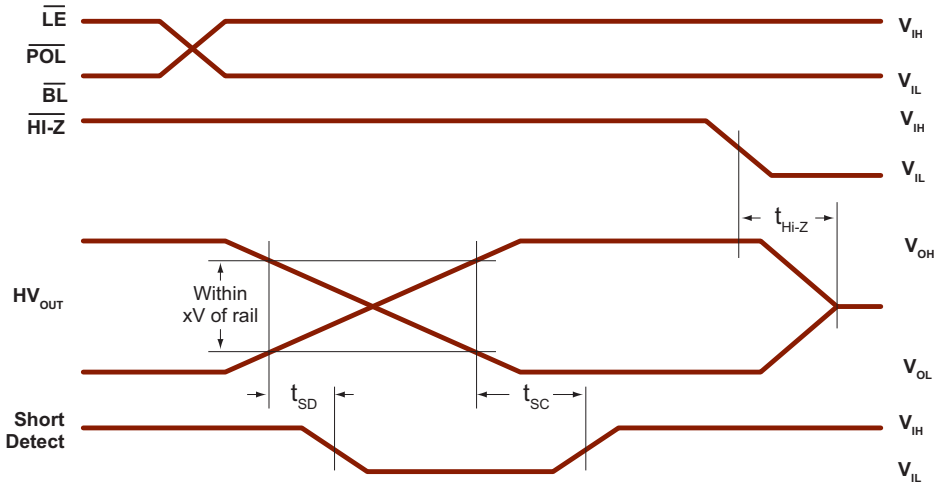


FIGURE 3-1: *Input and Output Equivalent Circuits.*



Note 1: For V_{PP} greater than 150V, the short detect output will flag short conditions. There are two possibilities:
Case 1: HV_{OUT} is higher than 10V when expected low.
Case 2: H_{VOUT} is lower than V_P–100V when expected high.

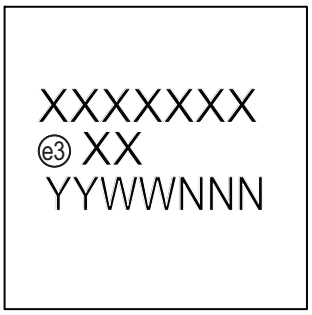
2: For V_{PP} greater than 150V, the short detect output will stay clear. There are two possibilities:
Case 1: HV_{OUT} is lower than 2V when expected low.
Case 2: HV_{OUT} is higher than V_{PP}–60V when expected high.

FIGURE 3-2: *Short-Circuit Detect Detail Timing.*

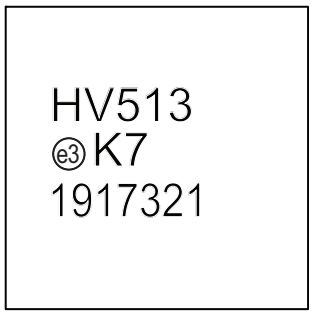
4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

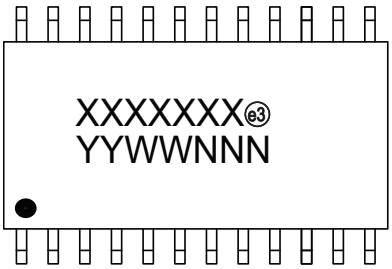
32-lead QFN



Example



24-lead SOW



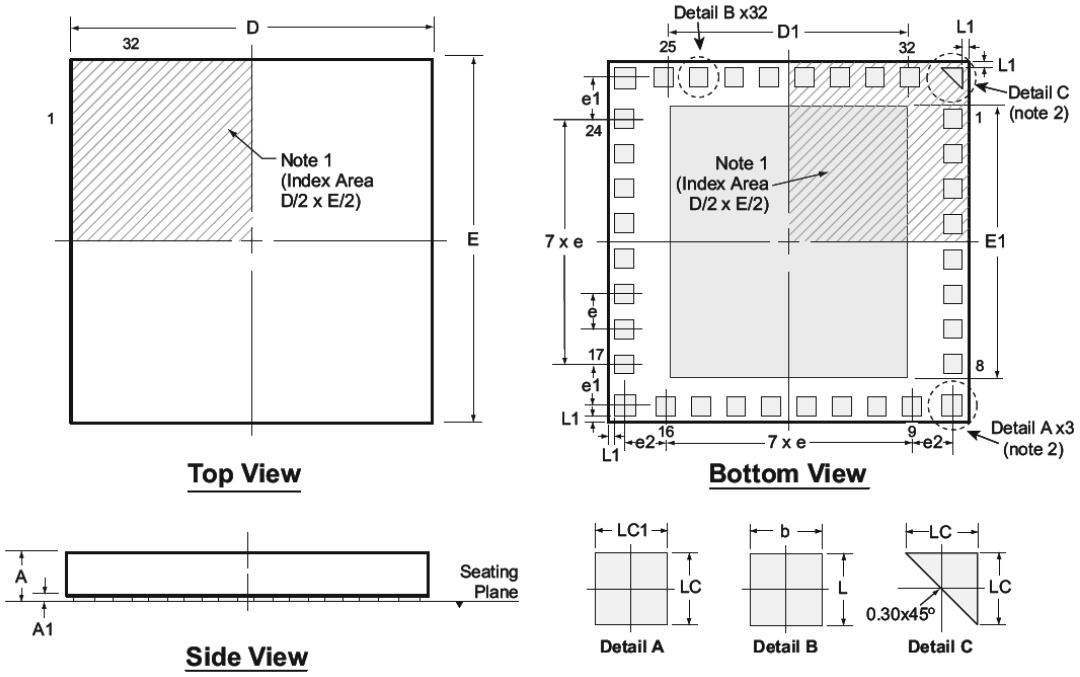
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

32-Lead QFN Package Outline (K7)

6.00x6.00mm body, 0.80mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

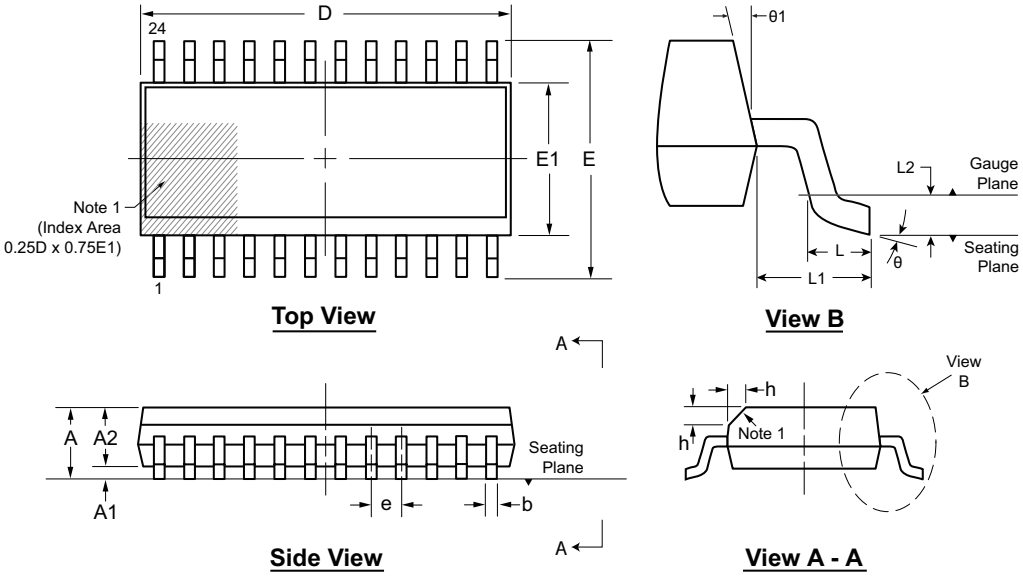
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The 4 corner pads are for mechanical placement only, they are not internally connected.*

Symbol		A	A1	b	D	D1	E	E1	e	e1	e2	L	L1	LC	LC1
Dimension (mm)	MIN	0.70	0.00	0.20	5.90	3.20	5.90	4.30	0.50 BSC	1.00 REF	0.975 REF	0.20	0.10 REF	0.20	0.25
	NOM	0.75	-	0.30	6.00	3.30	6.00	4.40				0.30		0.30	0.35
	MAX	0.80	0.05	0.40	6.10	3.40	6.10	4.50				0.40		0.40	0.45

Drawings not to scale.

24-Lead SOW (Wide Body) Package Outline (WG)

15.40x7.50 body, 2.65mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	15.20*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	15.40	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	15.60*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AD, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc # DSFP-HV513 to Microchip DS20005846B
- Removed “HVCMOS® Technology” in the Features section
- Changed the package marking format
- Removed the 32-lead (6 x 6) WQFN K7 M935 media type
- Changed the quantity of the 32-lead (6 x 6) WQFN K7 package from 400/Tray to 490/Tray
- Made minor changes throughout the document

Revision B (June 2019)

- Added Center Pad details to Table 2-1.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV513	=	8-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, Polarity, Hi-Z and Short-Circuit Detect
Packages:	K7	=	32-lead (6 x 6) WQFN
	WG	=	24-lead SOW
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	490/Tray for a K7 package
		=	1000/Reel for a WG package

Examples:

a) HV513K7-G: 8-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, Polarity, Hi-Z and Short-Circuit Detect, 32-lead (6 x 6) WQFN, 490/Tray

b) HV513WG-G: 8-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, Polarity, Hi-Z and Short-Circuit Detect, 24-lead SOW, 1000/Reel

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