



USB3280



Hi-Speed USB Device PHY with UTMI Interface

PRODUCT FEATURES

Data Brief

- Available in a 36-pin lead-free RoHS compliant (6 x 6 x 0.90mm) QFN package
- Interface compliant with the UTMI specification (60MHz, 8-bit bidirectional interface)
- Only one required power supply (+3.3V)
- USB-IF "Hi-Speed" certified to USB 2.0 electrical specification
- Supports 480Mbps Hi-Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45 Ω and 1.5k Ω termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 24MHz crystal
- Latch-up performance exceeds 150mA per EIA/JESD 78, Class II
- ESD protection levels of 5kV HBM without external protection devices
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- 55mA Unconfigured Current (typical) - ideal for bus powered applications.
- 83uA suspend current (typical) - ideal for battery powered applications.
- Industrial Operating Temperature -40°C to +85°C

Applications

The USB3280 is the ideal companion to any ASIC, SoC or FPGA solution designed with a UTMI Hi-Speed USB device (peripheral) core.

The USB3280 is well suited for:

- Cell Phones
- MP3 Players
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers

ORDER NUMBER(S):

USB3280-AEZG FOR 36-PIN, QFN PACKAGE (LEAD-FREE ROHS COMPLIANT)
USB3280-AEZG-TR FOR 36-PIN, QFN LEAD-FREE ROHS COMPLIANT (TAPE AND REEL)

Reel Size is 3000 pieces.



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General Description

The USB3280 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 36-pin lead-free RoHS compliant QFN package.

The USB3280 is an industrial temperature USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY uses an 8-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination and 5.25V short circuit protection of the DP/DM lines are internal to the chip. The USB3280 also has an integrated 1.8V regulator so that only a 3.3V supply is required.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

Block Diagram

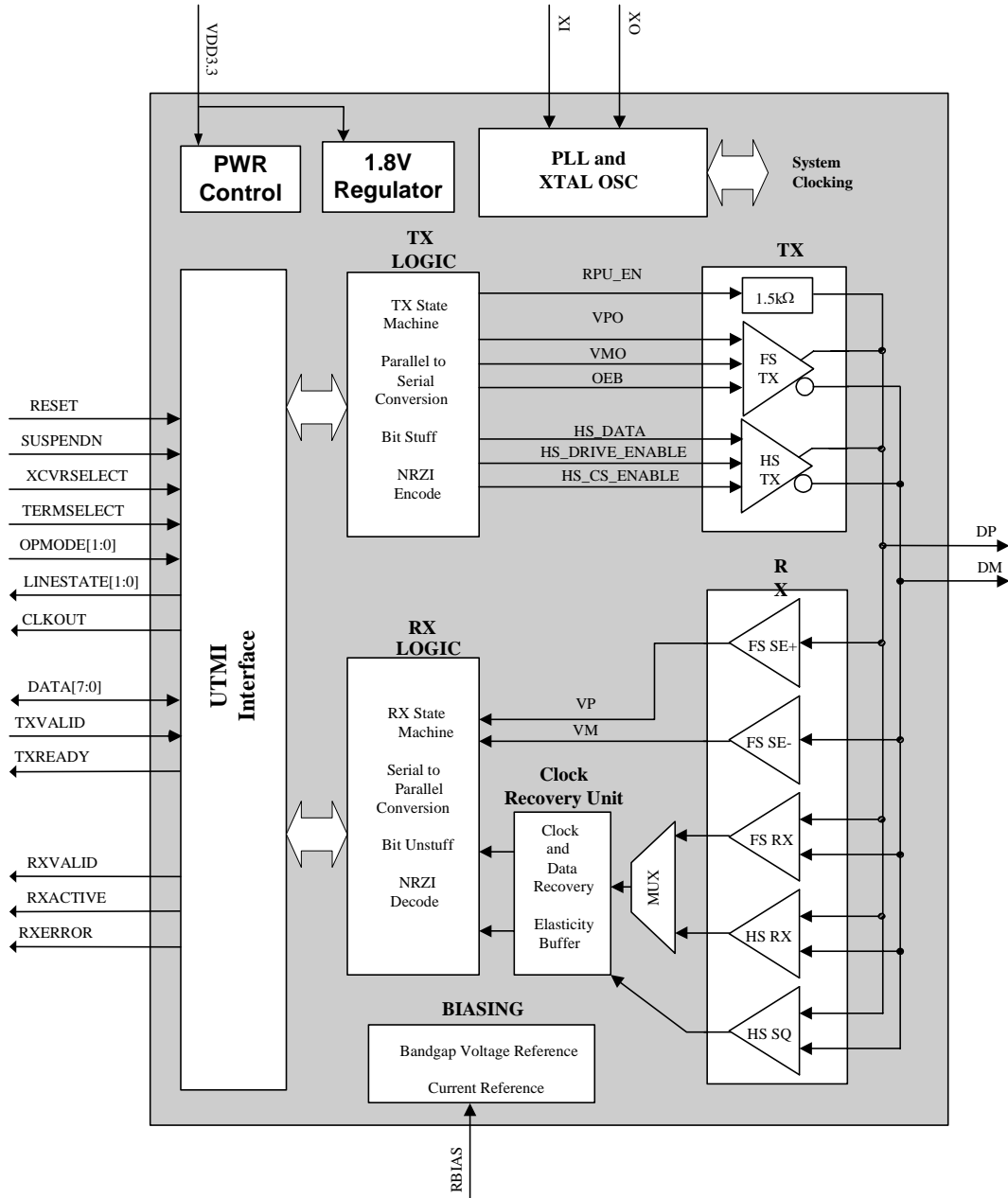


Figure 1 USB3280 Block Diagram

Package Outline

Revision 1.5 (11-15-07)

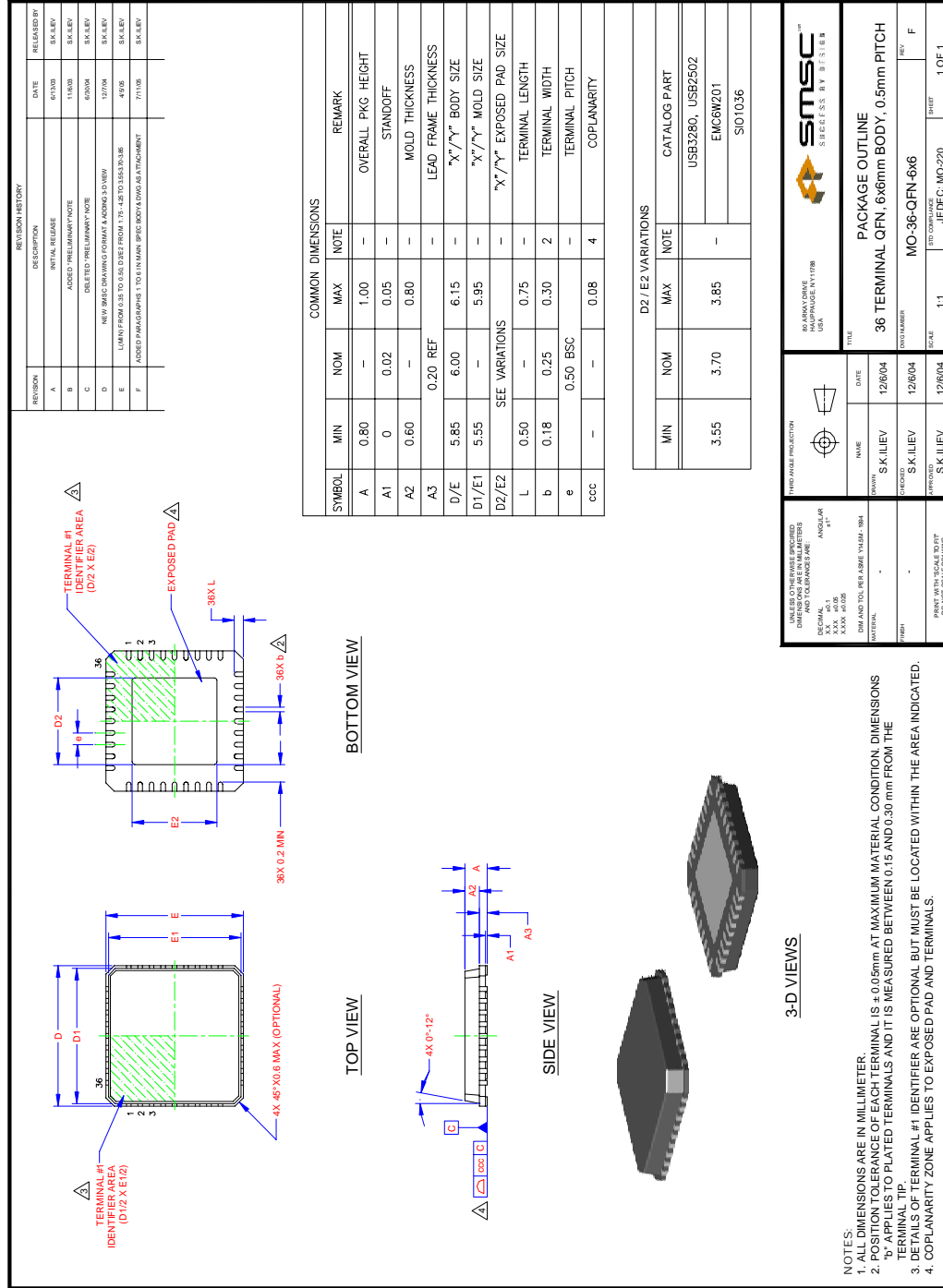


Figure 2 USB3280-AEZG 36-Pin QFN Package Outline and Parameters, 6 x 6 x 0.90 mm Body (Lead-Free RoHS Compliant)