10GbE and 10GFC Compliant Transceiver

FEATURES

GENERAL

- 10 Gbit/s bi-directional standards compliant transceiver.
- Four independent 1.2 - 3.2 Gbit/s SERDES.
- IEEE 802.3ae (10GbE) compliant including XAUI, XGXS, and XGMII.
- ANSI T11.2 (10 Gigabit & 2 Gigabit Fibre Channel) compliant.
- Supports PCI Express, Infiniband, Serial Rapid I/O, OC-48, OBSAI RP3, and other high speed backplane applications.
- Redundant XAUI links for working and protect backplane architectures.
- Integrated crossbar switch enables any port to any port configurations for both parallel and serial interfaces.
- Wide operating range from 1.2 Gbit/s - 3.2 Gbit/s enables backward compatibility
- Integrated serializer/deserializer, clock synthesis, clock recovery and 8B/10B encode/decode logic.
- Bypass of 8B/10B encode/decode for serialization of NRZ data streams.
- Pin configurable for standalone operation.

SERIAL I/O

- Fully redundant high-speed serial I/O channels for convenient switching to redundant fabric.
- High-speed outputs with programmable pre-emphasis to drive longer backplanes.
- High-speed inputs with programmable equalization to achieve superior bit-error rates.
- High-speed I/O with on-chip termination resistors to directly drive dual terminated 50 Ohm lines.

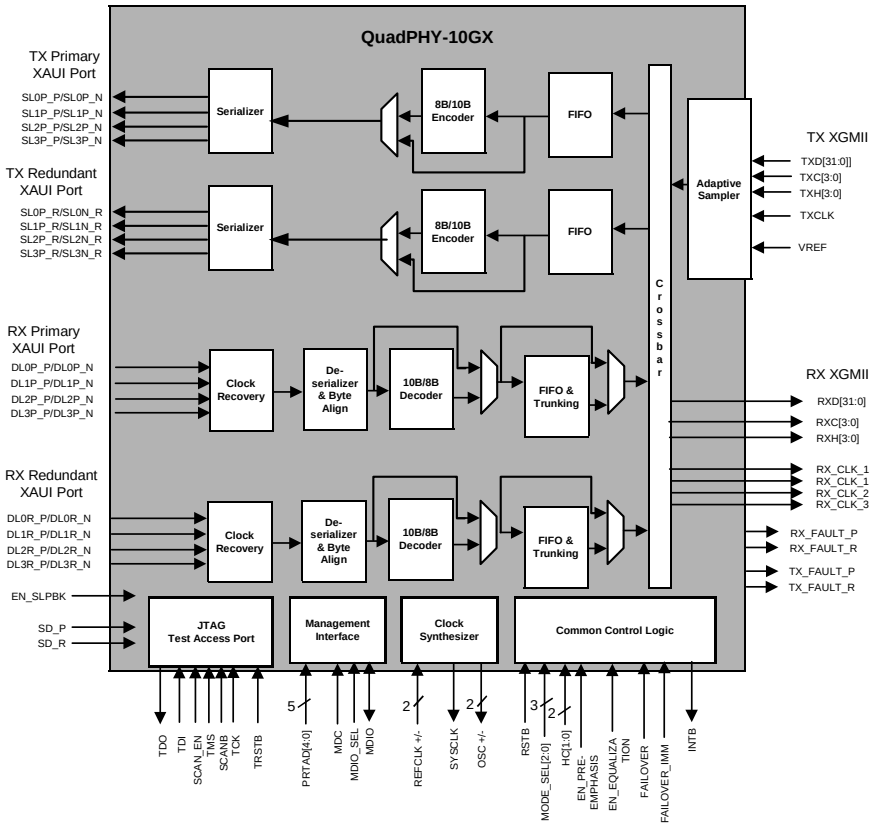
PARALLEL I/O

- 4 x 8 bit, 4 x 10 bit, 32 bit, or 40 bit Dual Data (DDR) parallel interface
- Adaptive timing provides improved TX XGMII timing margin.
- Selectable source simultaneous or source synchronous transmit and receive parallel interfaces.
- Convenient output clock for user friendly ASIC timing.
- Interoperates with the 1.5 V HSTL and 2.5 V SSTL_2 standards.

TRUNKING &TIMING

- Trunking feature de-skews and aligns all four channels to form a single 10 Gbit/s logical link.

BLOCK DIAGRAM



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TEST FEATURES

- Extensive control of loopback, BIST, and operating modes via an 802.3 compliant MDC/MDIO serial interface (1.2 V).
- On-chip packet generator/checker-provides at-speed diagnostics.
- Extensive built-in error counters per channel.
- Support for IEEE 1149.1 JTAG testing on all pins.
- Comprehensive evaluation platform for easy customer qualification.

PHYSICAL CHARACTERISTICS

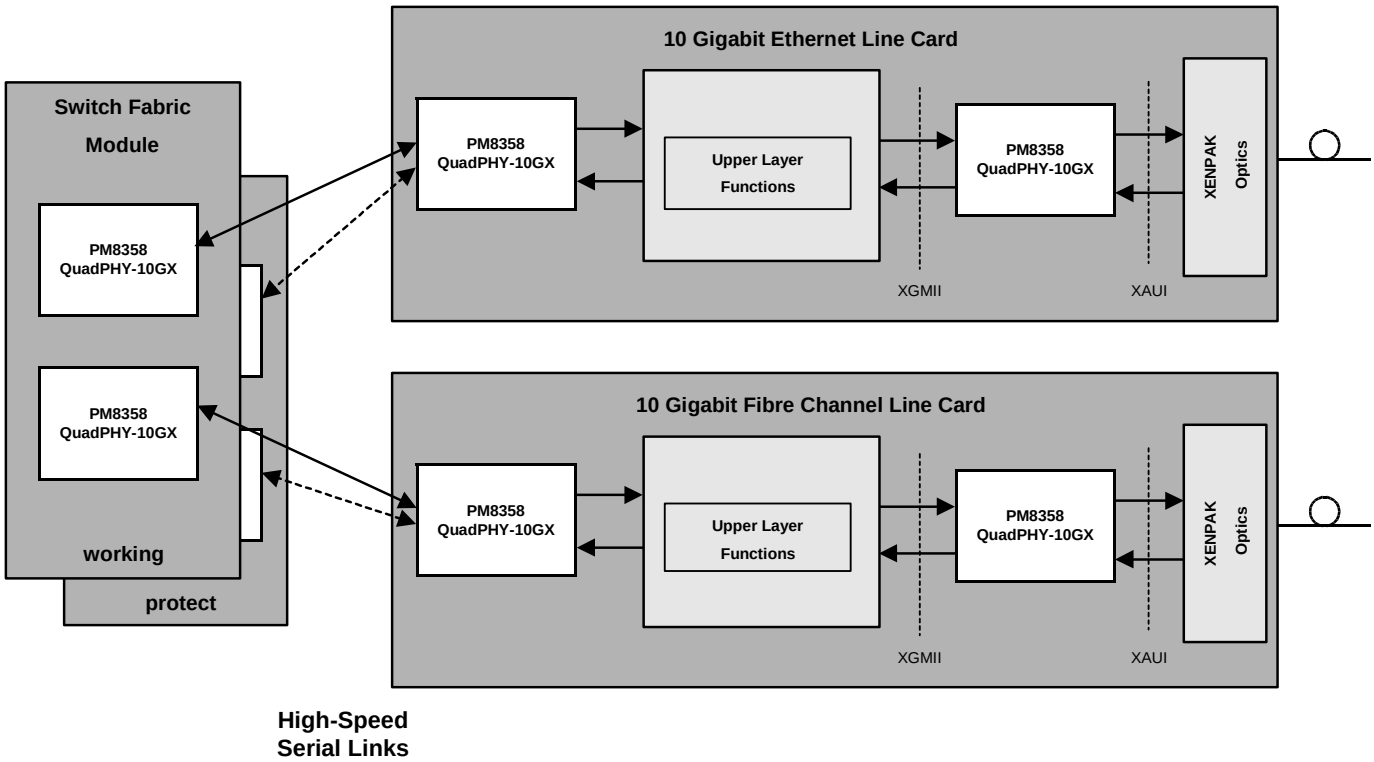
- 1.2/2.5 V, 0.13 µm CMOS technology.
- Small footprint 289-ball CABGA (19 mm x 19 mm).
- 1.3 W typical power at 3.2 Gbit/s (non redundant mode).

APPLICATIONS

- High-speed serial backplanes.
- 10GbE (XAUI) and 1GbE line cards.
- 10GFC and 2GFC line cards.
- Infiniband transceivers.
- OC-48 Serializer/Deserializer.
- PCI Express
- Serial Rapid I/O
- OBSAI RP3
- XAUI retimer.

TYPICAL APPLICATION

10GE AND 10GFC BACKPLANE DRIVER



Head Office:
PMC-Sierra, Inc.
8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 1.604.415.6000
Fax: 1.604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

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