IEEE 1588 & Synchronous Ethernet Packet Clock Network Synchronizer

Features

- Up to four independent clock channels
- Fully compliant to EEC (G.8262), SEC (G.813), GR-253 SMC and GR-1244 Stratum 3/3E
- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD basestations and small cell applications, with target performance less than ± 15 ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A applications with target performance less than ± 1 µs phase alignment.
- Client holdover and reference switching between multiple Servers
- Support for new ITU-T packet clock recommendations or drafts: G.8263 PEC-S, G.8273.2 T-BC, T-TSC, G.8273.4 T-BC-P, T-TSC-P & T-TSC-A

Ordering Information

ZL30701LDG6*	100 Pin aQFN	Trays
ZL30702LDG6*	100 Pin aQFN	Trays
ZL30703LDG6*	100 Pin aQFN	Trays
ZL30704LDG6*	100 Pin aQFN	Trays

*Pb Free Tin/Silver/Copper

Package size: 10 x 10 mm

-40°C to +85°C

- Excellent jitter performance of 180 fs rms (12 kHz to 20 MHz) meets 10G/40G and 100G PHY jitter requirements
- Up to four programmable digital PLLs/NCOs with loop bandwidth from 0.1 mHz to 470 Hz synchronize to any clock rate from 0.5 Hz to 900 MHz
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 0.1 ppb
- Any input reference can be fed with clock, sync (frame pulse), clock /sync pair or clock modulated with sync pulse (embedded PPS ePPS and embedded PP2S ePP2S)

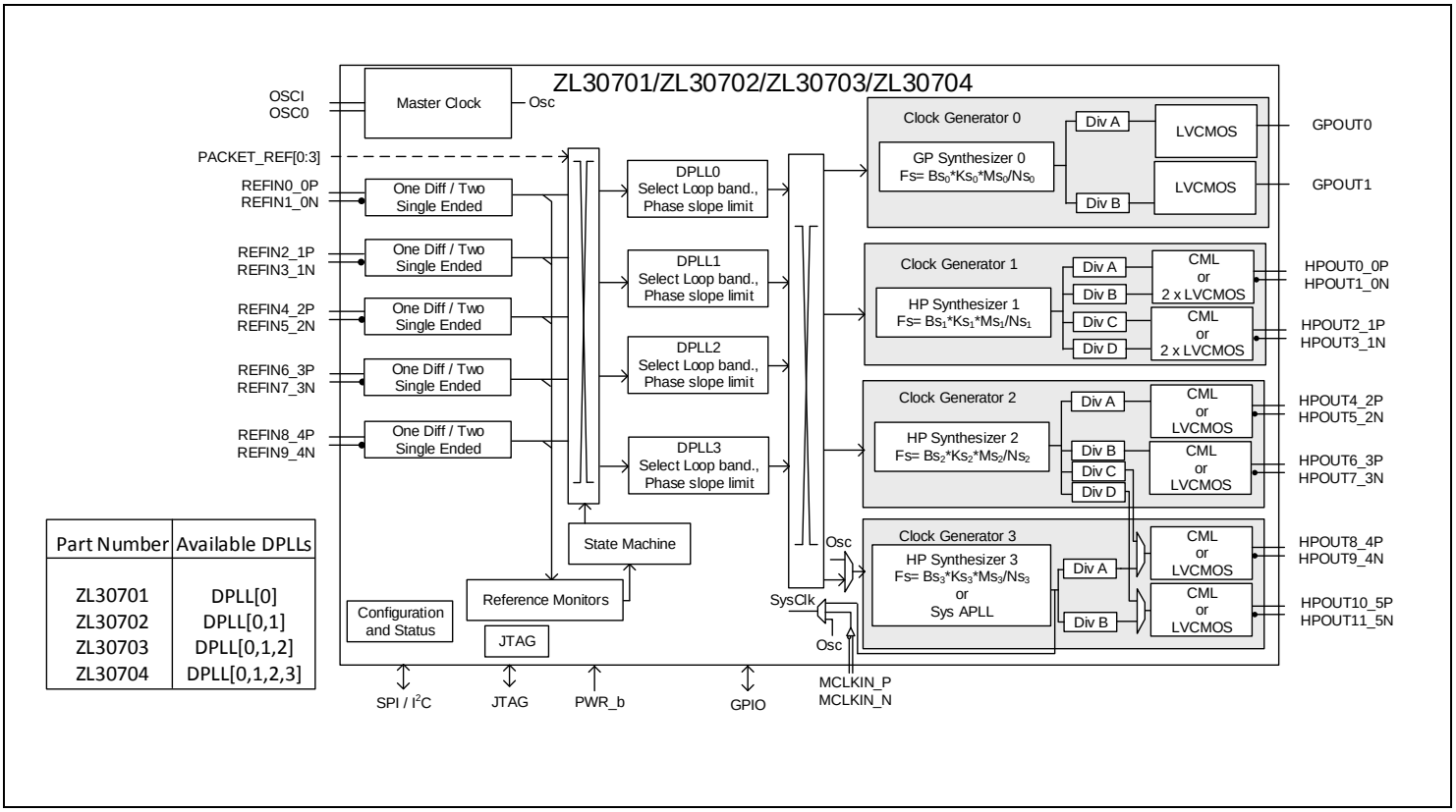

Figure 1. Functional Block Diagram

2 Feature List

2.1 General features

- Up to four independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - Supports split XO mode for low-frequency stability TCXO/OCXO with ultra-low jitter clock outputs
- Configurable from SPI/I2C bus or from pre-configured flash memory

2.2 Electrical Clock Inputs

- Accepts up to 10 LVCMOS or 5 LVDS/HCSL/LVPECL/CML inputs
- Frequencies from 0.5 Hz to 180 MHz for LVCMOS
- Frequencies from 0.5 Hz to 900 MHz for LVDS/HCSL/LVPECL/CML
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities.
  - Each input reference has its own set of monitors which can be independently programmed.
  - Loss of signal (LOS)
  - Single Cycle Monitor (Triggers on glitches or variation in duty-cycle)
  - Coarse Frequency Monitor
  - Precise Frequency Monitor
- Locks to gapped clocks

2.3 Electrical Clock Input-Output Special Formats

- Supports 64 kHz composite clocks with external glue logic
- Supports embedded pulse per second (ePPS) single wire for carrying high-speed clock & 1PPS
- Supports REF-SYNC pair, a combination of a high speed clock reference and a frame pulse sync pair
- Each output can generate clock, sync pulse, embedded pulse per second (ePPS) or embedded pulse per 2 seconds (ePP2S)
  - Clock modulated sync feature helps in reducing number of clock lines on backplane and in addition provides equal delay for both clock and sync signals.

2.4 Electrical Clock Engine

- Digital PLLs filter jitter from 0.1 mHz up to 470 Hz
- Multiple modes of operation
  - Freerun
  - Forced holdover
  - Forced reference
  - Automatic
  - NCO
- Internal state machine automatically controls state
  - Locked
  - Acquiring
  - Holdover
- Automatic hitless reference switching and digital holdover on reference fail
  - Physical-to-physical reference switching
  - Physical-to-packet reference switching
  - Packet-to-physical reference switching
  - Packet-to-packet reference switching
- Support for fast lock with lock times in seconds
- Support for hitless reference switching
- Internal, per DPLL, time of day counters maintaining full 48-bit seconds and 32-bit nanoseconds aligned to 1PPS rollover
- Holdover better than 0.01 ppb
- Full rate conversion between input and output clock frequencies
- Supports ITU-T G.823, G.824 and G.8261 for 2048 Kbit/s and 1544 Kbit/s interfaces
- Supports G.781 SETS

2.5 Electrical Clock Engine: Industry Specifications

- Support for wide variety of Equipment Clock specifications
  - SyncE
    - ITU-T G.8262 option 1 EEC (Europe/China)
    - ITU-T G.8262 option 2 (USA)
  - SONET/SDH
    - ITU-T G.813 option 1 SEC (Europe/China)
    - ITU-T G.813 option 2 (USA)
    - ANSI T1.105/Telcordia GR-253 Stratum 3 for SONET
    - Telcordia GR-253 SMC
  - PDH
    - ITU-T G.812 Type I SSU
    - ITU-T G.812 Type II, ANSI T1.101/Telcordia GR-1244 Stratum 2 (without optional freq monitoring at 16 ppb)
    - ITU-T G.812 Type III, ANSI T1.101/Telcordia GR-1244 Stratum 3E
    - ANSI T1.101/Telcordia GR-1244 Stratum 3
    - ANSI T1.101/Telcordia GR-1244 Stratum 4E/4

2.6 Electrical Clock Generation

- Four programmable synthesizers
- Precision Synthesizers
  - Each ultra-low jitter output can be independently set to be differential (CML) or two CMOS
  - Six CML outputs
    - Generate clock rates from 0.5 Hz to 900 MHz
    - Jitter performance of 180 fs rms (12 KHz – 20 MHz)
    - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
  - Twelve LVCMOS outputs
    - Generate clock rates from 0.5 Hz to 180 MHz
    - Jitter performance of 290 fs rms (12 kHz – 20 MHz)
- General Synthesizer
  - Two LVCMOS outputs
  - Generate clock rates from 1 Hz to 180 MHz
  - Jitter performance of 17 ps rms (12 kHz – 20 MHz)
- Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
- Each output has its own power supply pin which can be hooked to 3.3V, 2.5V or 1.8V supplies. Outputs may be disabled to save power

2.7 Packet Synchronization

The Time Synchronization Algorithm is suitable for use in a wide variety of markets and applications, including the following IEEE 1588-2008 Profiles

- Annex J.3 Delay Request-Response Default Profile
- Annex J.4 Peer-to-peer Default Profile
- ITU-T G.8265.1 Telecom Profile for Frequency Synchronization
- ITU-T G.8275.1 Telecom Profile for Phase with Full Timing Support Networks
- ITU-T G.8275.2 Telecom Profile for Phase with Partial Timing Support Networks
- CableLabs CM-SP-RDTI Remote DTI Profile
- SMPTE ST-2059-2 Professional Broadcast Environment Profile
- IEEE C37.238 Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications.
- IEC 61850-9-3 Power Utility Automation Profile
- IEEE802.1as AVB-TSN gPTP
- IEEE 1588-2018 Annex X High Accuracy Profile (based on White Rabbit)
- IETF TICTOC Enterprise Profile

2.7.1 Applications

The Time Synchronization Algorithm is suitable for many end application targets.

- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications, with target performance less than ± 15 ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications with target performance less than ± 1 μs phase alignment.
- Time Synchronization for TAI, UTC-traceability and GNSS/GPS replacement.

2.7.2 Packet Networks

The Time Synchronization Algorithm is suitable for high performance over a variety of packet networks

- ITU-T G.8261 Appendix VI
- ITU-T G.8261.1 network limit compliant
- ITU-T G.8271.1 network limit compliant
- ITU-T G.8271.2 (draft) network limit compliant
- Native Ethernet (switched) & IP (routed) networks
- xDSL
- Microwave
- Fully aware, partially aware and unaware timing supported networks
- Networks including intermediate Boundary Clocks and Transparent Clocks
- Networks with and without SyncE or frequency physical layer support

2.7.3 Clock Specifications

The Time Synchronization Algorithm is suitable to address a variety of standardized clock specifications, including

- ITU-T G.8263 PEC-S
- ITU-T G.8273.2 T-BC full on-path without SyncE
- ITU-T G.8273.2 T-BC full on-path with SyncE
- ITU-T G.8273.2 T-TSC full on-path without SyncE
- ITU-T G.8273.2 T-TSC full on-path with SyncE
- ITU-T G.8273.4 T-BC-P (draft)
- ITU-T G.8273.4 T-TSC-A (draft)
- ITU-T G.8273.4 T-TSC-P (draft)

2.7.4 Monitoring & Redundancy

The Time Synchronization Algorithm includes monitoring & redundancy for high availability synchronization, including

- Synchronization to the best available Server
- Client monitoring of secondary Server references
    - Monitoring includes full time synchronization reporting of secondary Server
    - Supports a programmable number of secondary Server connections
- Hitless reference switching between multiple Servers
- Holdover when Server packet connectivity is lost
- TIE clear option to build out, or clear, phase offsets between Server references

2.7.5 General

The Time Synchronization Algorithm includes many advanced features to aide in the high-accuracy & high-stability applications, including

- Full PLL state machine (Freerun, Holdover, Frequency Lock Acquiring, Frequency Lock Acquired, Phase Lock Acquired), with programmable thresholds for state transitions
- Programmable bandwidth configurability from sub-mHz to 100's of mHz.
- Programmable packet rates from 1 packet/second to over 128 packets/second
- User ability to manually add frequency offsets due to temperature or ageing (especially during holdover state)

3 Application Examples

The only difference between ZL30701/ZL30702/ZL30703/ZL30704 is the number of DPLLs. The least significant digit in the part number assigns the number of available DPLLs.

3.1 Packet Layer - Centralized Architecture

A typical ZL30701/ZL30702/ZL30703/ZL30704 application is IEEE1588 time synchronization with centralized architecture shown in Figure 2 . The application has three distinct modules: Ethernet PHY/MAC with timestamp capability, Host processor running IEEE1588 protocol and Microsemi Time Sync Frequency and Phase algorithm and the ZL30701/ZL30702/ZL30703/ZL30704 Synchronous Ethernet and IEEE1588 Packet Clock Network Synchronizer. Although Figure 2 shows a single board application commonly known as “Pizza Box”, the same type of architecture would be used in shelf based systems. Shelf based systems would have ZL30701/ZL30702/ZL30703/ZL30704 populated on active and redundant timing card and Ethernet PHY/MACs would be placed on line cards.

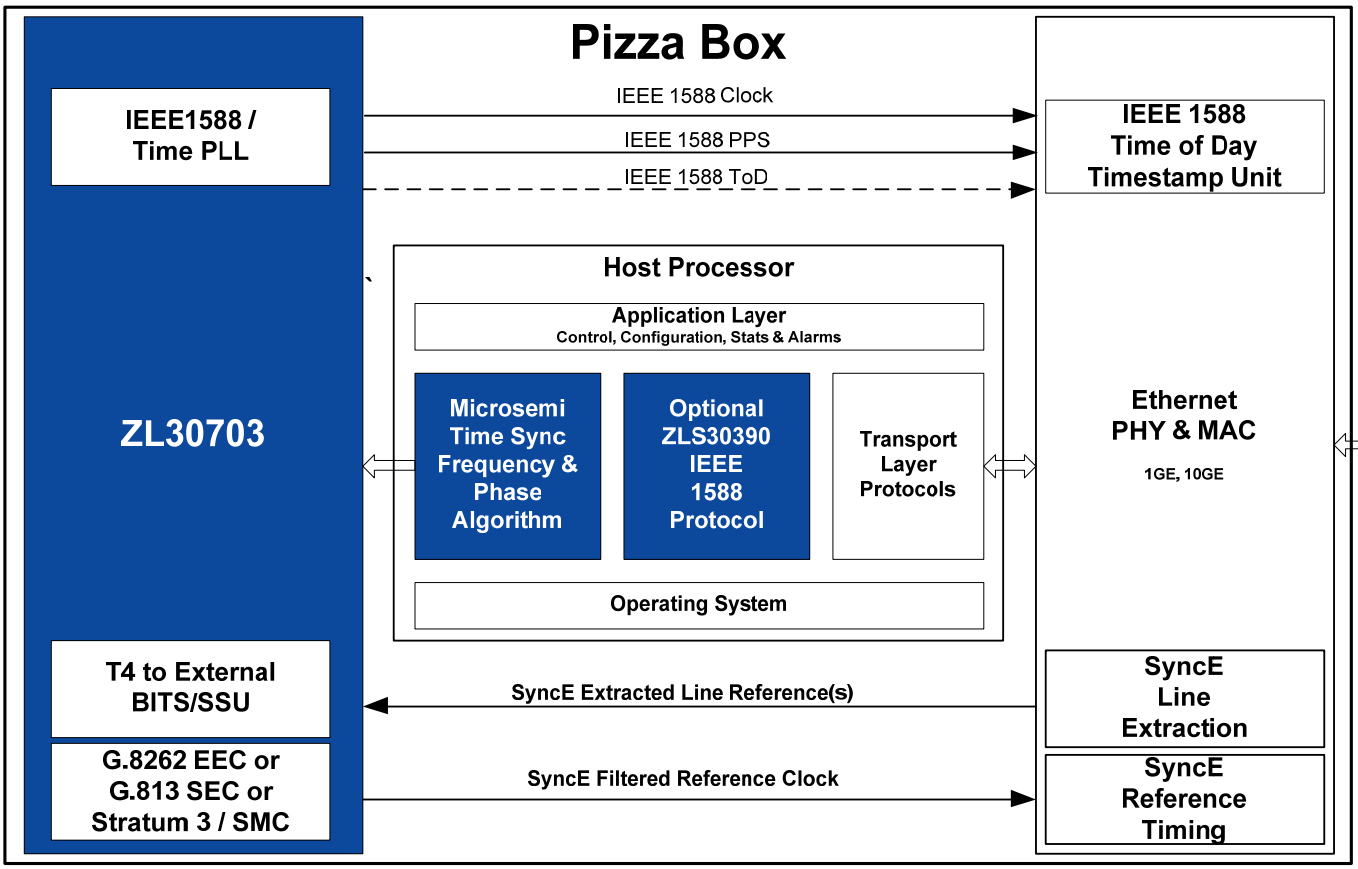

Figure 2. IEEE1588 Time Synchronization with Centralized Architecture

4 Product Family

There are several devices within the ZL30701/702/703/704 family. They are differentiated by the number of DPLL, as shown in

Table 1 · ZL3070x Product Family

Product Number	Number of DPLL Channels	Number of Synthesizers
ZL30701	1	4
ZL30702	2	4
ZL30703	3	4
ZL30704	4	4

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