Regulating Pulse Width Modulator

Description

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lower external parts count when used to implement all types of switching power supplies. The on-chip +5.1 V reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic, which results in a HIGH output level when OFF.

Features

- 8V to 35V Operation
- 5.1V Reference Trimmed to ±1%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-start
- Input Undervoltage Lockout
- Latching P.W.M. to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers

High Reliability Features

Following are the high reliability features of SG1525A and SG1527A:

- Available to MIL-STD-883, ¶ 1.2.1
- MIL-M38510/12602BEA - JAN1525AJ
- MIL-M38510/12604BEA - JAN1527AJ
- MSC-AMS level “S” Processing Available

Block Diagram

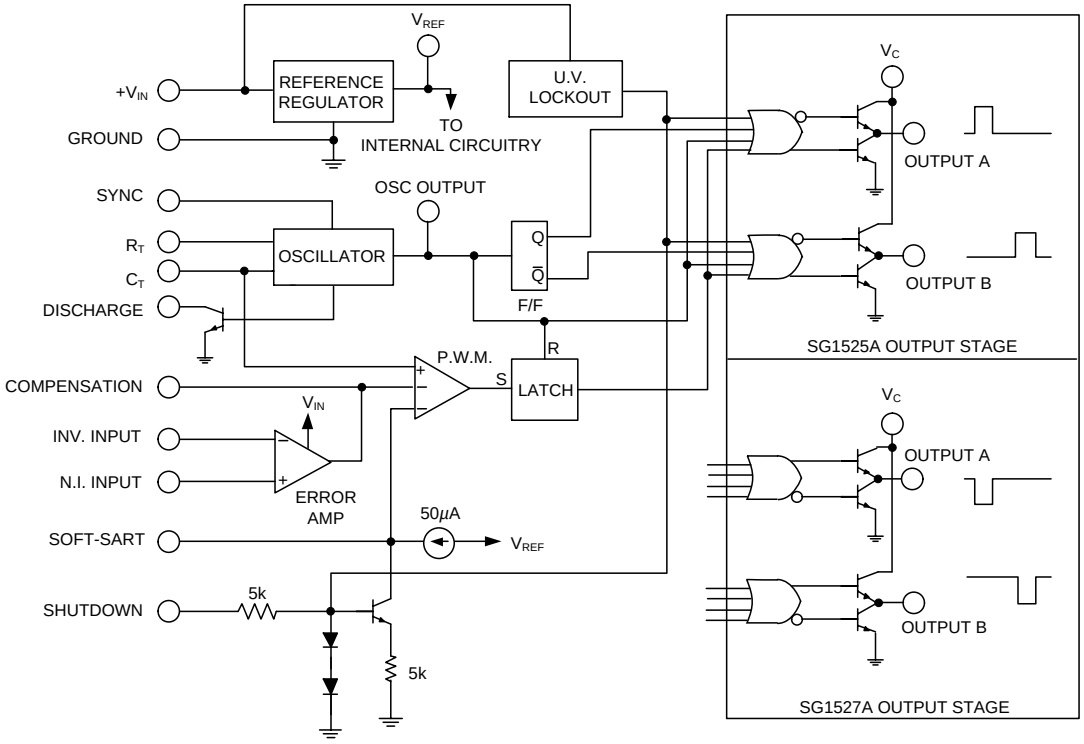
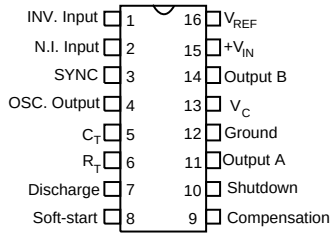
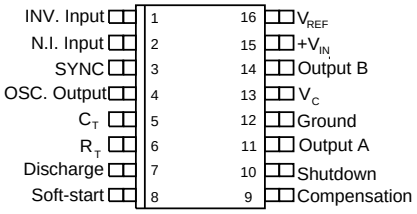
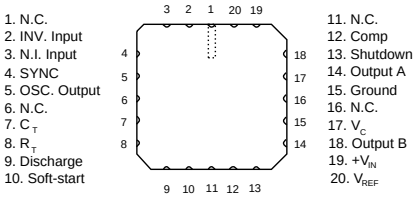


Figure 1 · Block Diagram

Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	J	16-PIN ceramic DIP	SG1525AJ-883B	CERDIP	 N Package: RoHS Compliant / Pb-free Transition DC: 0503 N Package: RoHS / Pb-free 100% Matte Tin Lead Finish
			SG1525AJ-JAN		
			SG1525AJ-DESC		
			SG1525AJ		
			SG1527AJ-883B		
			SG1527AJ-JAN		
			SG1527AJ-DESC		
			SG1527AJ		
-25°C to 85°C			SG2525AJ		
			SG2527AJ		
-0°C to 70°C			SG3525AJ		
			SG3527AJ		
-25°C to 85°C	N	16-PIN plastic DIP	SG2525AN	PDIP	
			SG2527AN		
-0°C to 70°C			SG3525AN		
			SG3527AN		
-25°C to 85°C	DW	16-pin wide body plastic SOIC	SG2525ADW	SOIC	 DW Package: RoHS Compliant / Pb-free Transition DC: 0516 DW Package: RoHS / Pb-free 100% Matte Tin Lead Finish
			SG2527ADW		
-0°C to 70°C			SG3525ADW		
			SG3527ADW		
-55°C to 125°C	L	20-pin ceramic leadless chip carrier (LCC)	SG1525AL-883B	CLCC	
			SG1525AL		
			SG1527AL-883B		
			SG1527AL		

Notes:

1. *Contact factory for JAN and DESC product availability.*
2. *All packages are viewed from the top.*
3. *Hermetic Packages J & L use Sn63Pb37 hot solder dip lead finish, contact factory for availability of RoHS compliant versions.*

Absolute Maximum Ratings[1]

Parameter	Value	Units
Supply Voltage ($+V_{IN}$)	40	V
Collector Supply Voltage (V_C)	40	V
Logic Inputs	-0.3 to 5.5	V
Analog Inputs	-0.3 to V_{IN}	V
Output Current, Source or Sink	500	mA
Reference Load Current	50	mA
Oscillator Charging Current	5	mA
Operating Junction Temperature		
Hermetic (J, L Packages)	150	°C
Plastic (N, DW Packages)	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10 seconds)	300	°C
RoHS Peak Package Solder Reflow Temp. (40 s max. exp.)	260 (+0, -5)	°C
Note: Values beyond which damage may occur		

Thermal Data

Parameter	Value	Units
J Package		
Thermal Resistance-Junction to Case, θ_{JC}	30	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	80	°C/W
N Package		
Thermal Resistance-Junction to Case, θ_{JC}	40	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	65	°C/W
DW Package		
Thermal Resistance-Junction to Case, θ_{JC}	40	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	95	°C/W
L Package		
Thermal Resistance-Junction to Case, θ_{JC}	35	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W

Notes:

1. *Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.*
2. *The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.*

Recommended Operating Conditions[1]

Parameter	Value	Units
Input Voltage ($+V_{IN}$)	8 to 35	V
Collector Voltage (V_C)	4.5 to 35	V
Sink/Source Load Current (steady state)	0 to 100	mA
Sink/Source Load Current (peak)	0 to 400	mA
Reference Load Current	0 to 20	mA
Oscillator Frequency Range	0.1 to 350	kHz
Oscillator Timing Resistor (R_T)	2 to 150	kΩ
Deadtime Resistor Range (R_D)	0 to 500	Ω
Maximum Shutdown Source Impedance	5	kΩ
Oscillator Timing Capacitor (C_T)	0.001 to 0.1	µF
Operating Ambient Temperature Range[1]		
SG1525A/SG1527A	-55 to 125	°C
SG2525A/SG2527A	-25 to 85	°C
SG3525A/SG3527A	0 to 70	°C
Note: Range over which the device is functional.		

Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1525A/SG1527A with -55°C ≤ T_A ≤ 125°C, SG2525A/SG2527A with -25°C ≤ T_A ≤ 85°C, SG3525A/SG3527A with 0°C ≤ T_A ≤ 70°C, and $+V_{IN}$ = 20V. Low duty cycle pulse testing techniques are used that maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Section[1]								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8V to 35V		10	30		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability[1]	Over Operating Temperature Range		20	50		20	50	mV
Total Output Voltage Range[1]	Over Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0V, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage[1]	10Hz ≤ f ≤ 10kHz, T_J = 25°C		40	200		40	200	µVrms
Long Term Stability[1]	T_J = 125°C		20	50		20	50	mV/khr

Notes:
1. *These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.*
2. *F_{OSC} = 40 kHz (R_T = 3.6k Ω, C_T = 0.01µF, R_D = 0Ω.).*
3. *Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.*

Electrical Characteristics *(continued)*

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A/SG3527A			Units
		Min	Typ	Max	Min	Typ	Max	
Oscillator Section[2]								
Initial Accuracy	T_J = 25°C	37.6	40	42.4	37.6	40	42.4	kHz
Voltage Stability	V_{IN} = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability[1]	MIN ≤ T_J ≤ MAX		±3	±6		±3	±6	%
Minimum Frequency[1]	R_T = 150kΩ, C_T = 0.1µF			150			150	Hz
Maximum Frequency[1]	R_T = 2 kΩ, C_T = 1nF	350			350			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		V
Clock Width	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	R_L ≥ 10MΩ, T_J = 25°C	60	75		60	75		dB
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2 V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	50	60		50	60		dB
PWM Comparator Section[2]								
Minimum Duty Cycle	V_{COMP} = 0.6V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Input Threshold[2]	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current			0.05	2.0		0.05	2.0	µA
Soft-Start Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A/SG3527A			Units
		Min	Typ	Max	Min	Typ	Max	
Output Drivers Section (each transistor, V_C = 20V)								
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.2		1.0	2.2	V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
Collector Leakage[3]	V_C = 35V			200			200	µA
Rise Time	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Shutdown Delay[1]	V_{SD} = 3V, C_S = 0, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Total Standby Current								
Standby Current	V_{IN} = 35V		14	20		14	20	mA

Notes:

1. *These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.*
2. *F_{OSC} = 40 kHz (R_T = 3.6k Ω, C_T = 0.01µF, R_D = 0Ω).*
3. *Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.*

Oscillator Section

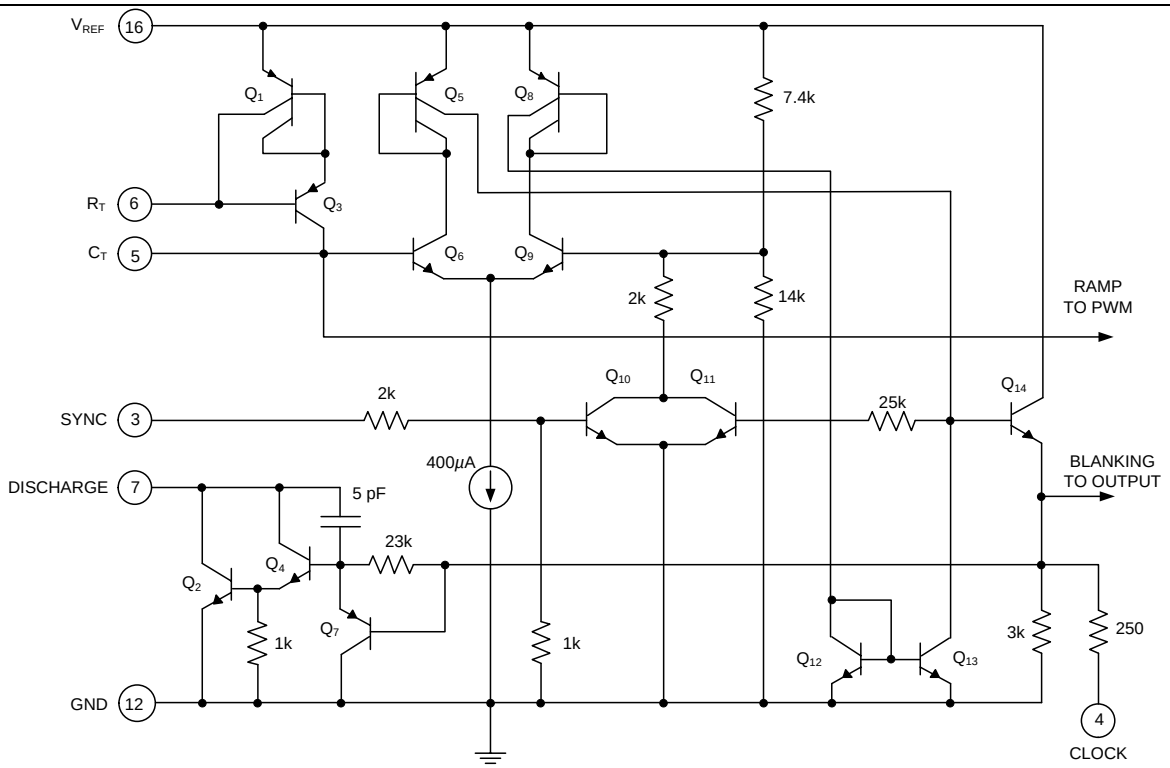


Figure 2 · Oscillator Schematic

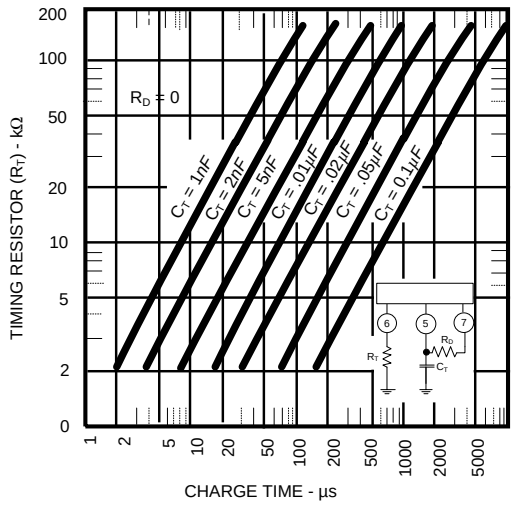


Figure 3 · Oscillator Charge Time versus R_T And C_T

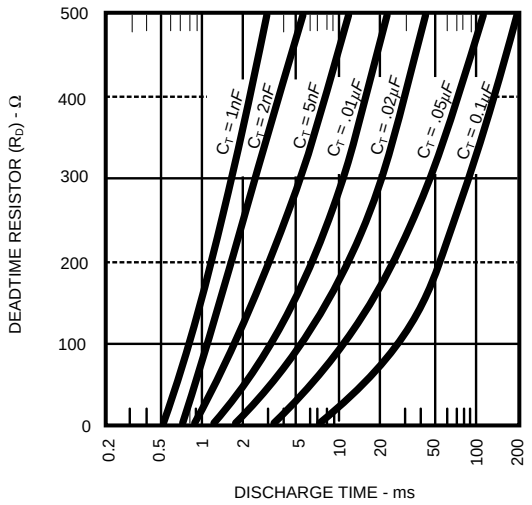


Figure 4 · Oscillator Discharge Time versus R_D And C_T

Error Amplifier Section

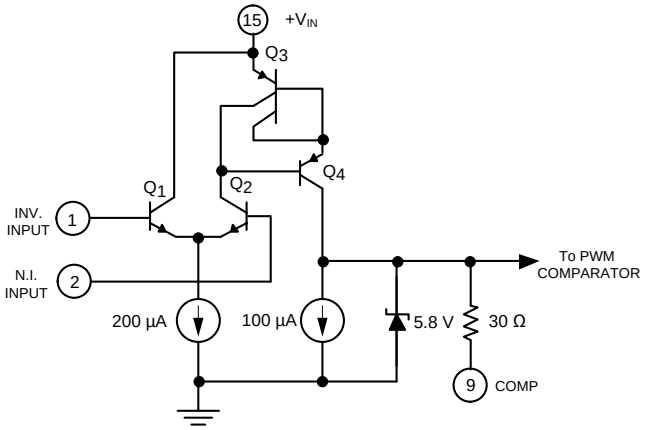


Figure 5 · Error Amplifier

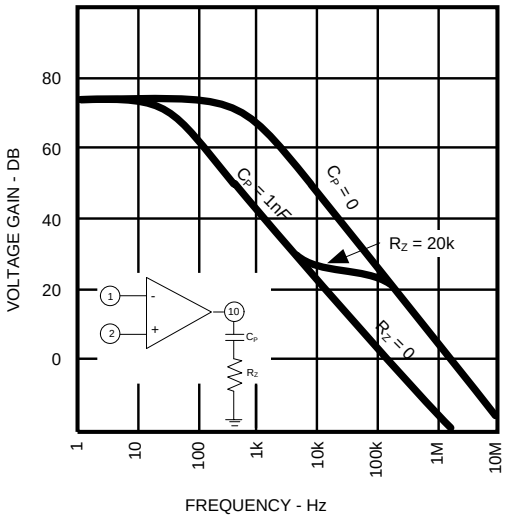


Figure 6 · Error Amplifier Open-Loop Frequency Response

Output Section

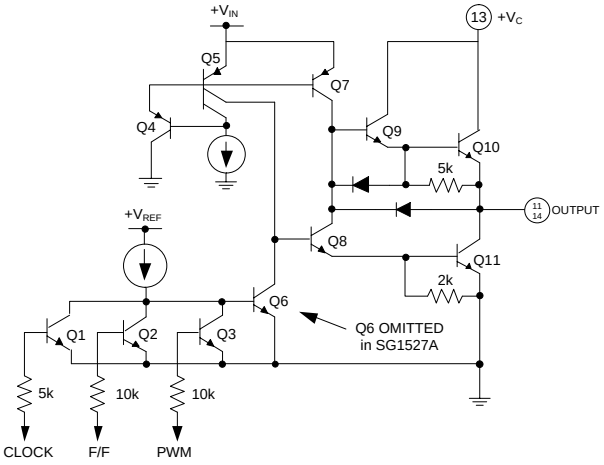


Figure 7 · Output Circuit (½ circuit shown)

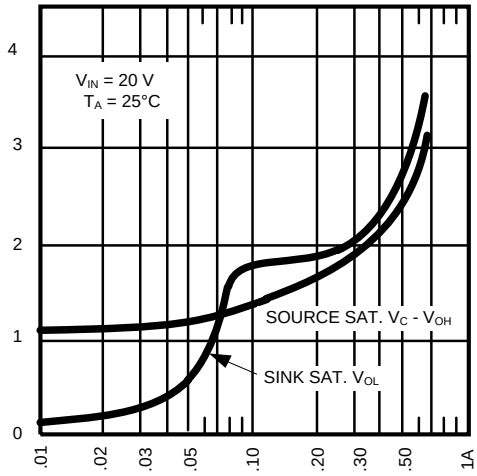
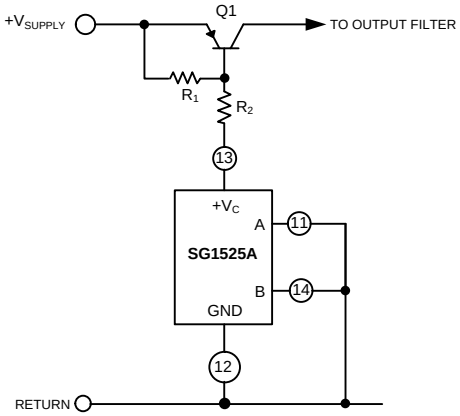
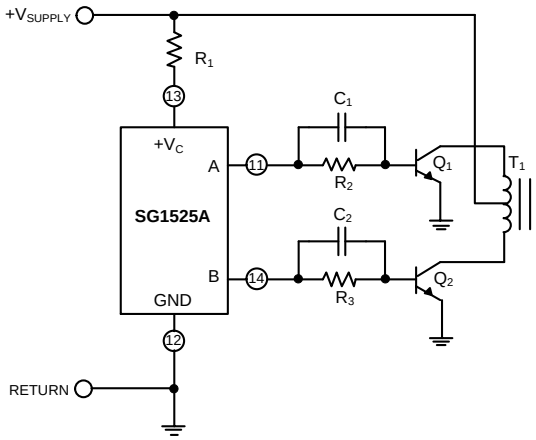


Figure 8 · Output Saturation Characteristics

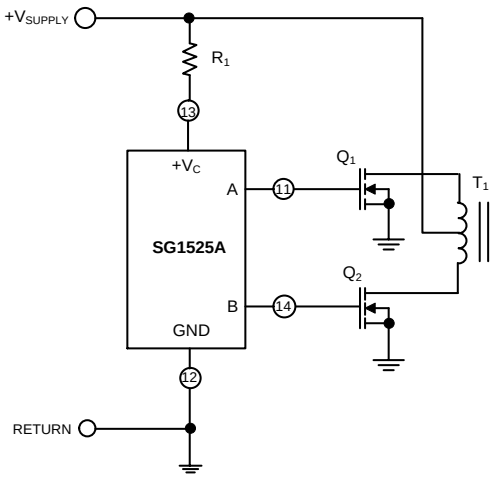
Application Information



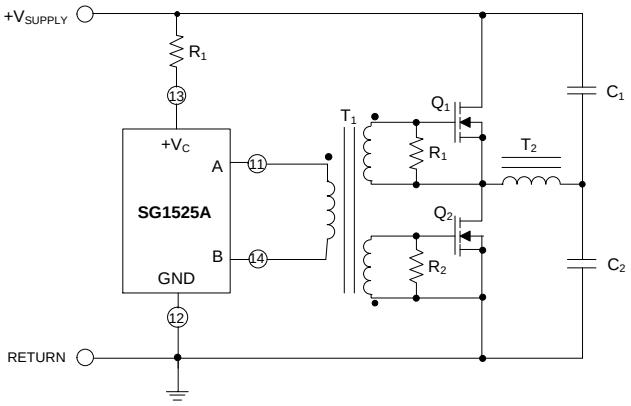
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3 .Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

Shutdown Options

1. Use an external transistor or open-collector comparator to pull down on the Comp terminal. This sets the PWM latch turning off both outputs. If the shutdown signal is momentary, pulse-by-pulse protection can be accomplished as the PWM latch resets with each clock pulse.
2. The same results can be accomplished by pulling down on the Soft-Start terminal with the difference that on this pin, shutdown does not affect the amplifier compensation network but must discharge any Soft-Start capacitor.
3. Apply a positive-going signal to the Shutdown terminal. This provides most rapid shutdown of the outputs but will not immediately set the PWM latch if there is a Soft-Start capacitor. This capacitor discharges but with a current of approximately twice the charging current.
4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Soft-Start terminal. Slow turn-on may still be accomplished by applying an external capacitor, blocking diode, and charging resistor to the comp terminal. (See SG1524 Application Note).

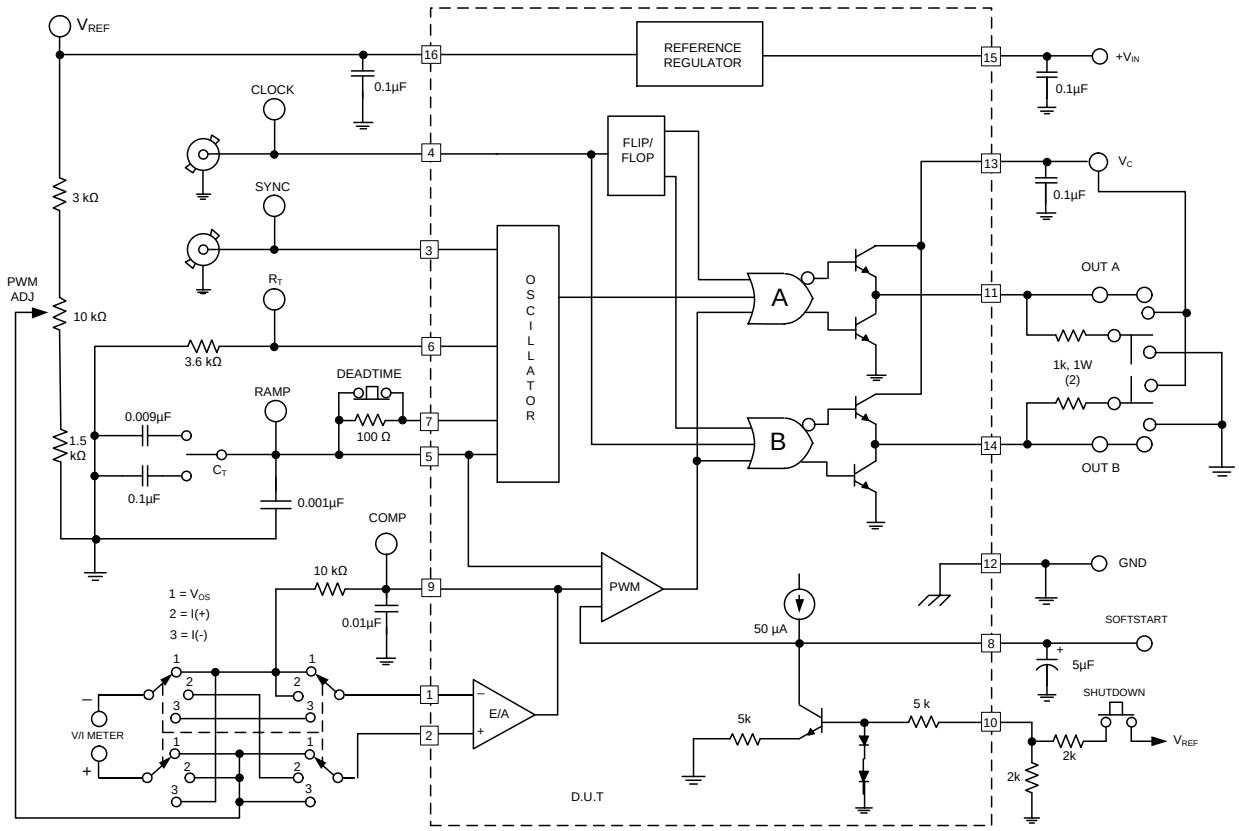
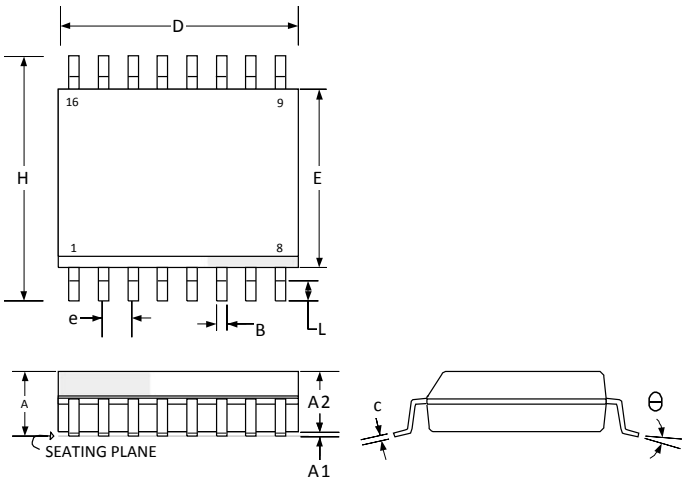


Figure 9 · SG1525A/1527A Lab Test Fixture

Package Outline Dimensions

Controlling dimensions are in metric, inches equivalents are shown for general information.



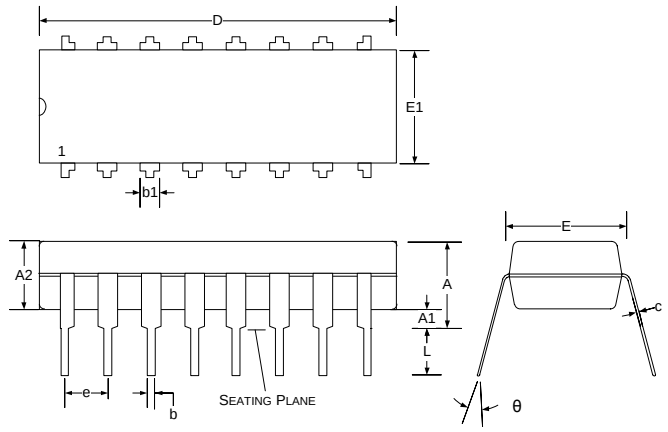
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.06	2.65	0.081	0.104
A1	0.10	0.30	0.004	0.012
A2	2.03	2.55	0.080	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	10.08	10.50	0.397	0.413
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	0.10	-	0.004

*Lead co planarity

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage. Dimensions are in mm, inches are for reference only.

Figure 10 · DW 16-Pin SOWB Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
A2	3.30 Typ.		0.130 Typ.	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	0.381	0.115	0.150
θ	-	15°	-	15°

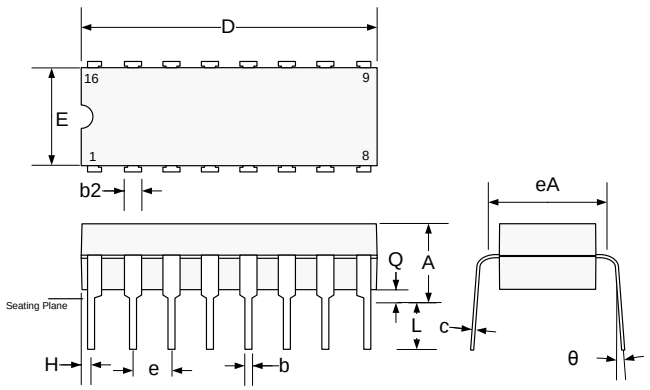
Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage. Dimensions are in mm, inches are for reference only.

Figure 11 · N 16-Pin Plastic Dual Inline Package Dimensions

Package Outline Dimensions (continued)

Controlling dimensions are in inches, metric equivalents are shown for general information.

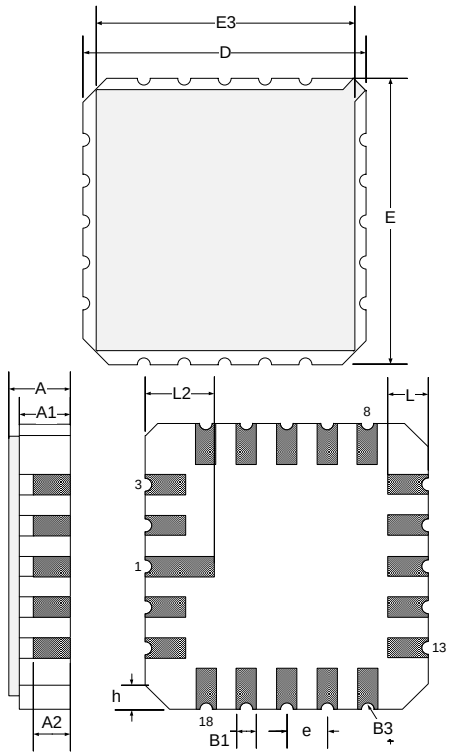


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 12 · J 16-Pin Ceramic Dual Inline Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 13 · L 20-Pin Ceramic LCC Package Outline Dimensions

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