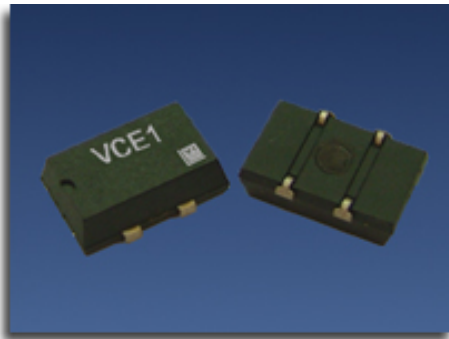
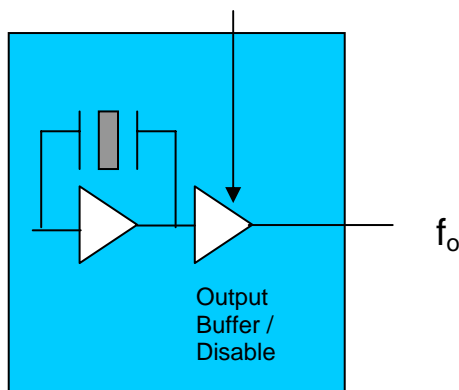



## VCE1 series 3.3, 5.0 volt CMOS Oscillator



The VCE1 Crystal Oscillator



### Features

- CMOS output
- Output frequencies to 66.667 MHz
- Tri-state output for board test and debug
- 0/70 or -40/85 °C operating temperature
- Low cost industry standard 14x9.8 mm package
- RoHS and lead free compliant construction 

### Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA

### Description

Vectron's VCE1 Crystal Oscillator (XO) is quartz stabilized square wave generator with a CMOS output, operating off a 3.3 or 5.0 volt supply.

## Performance Characteristics

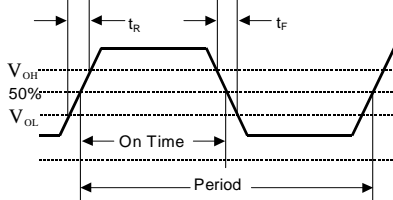
**Table 1. Electrical Performance, 5V option**

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	$f_O$	1.000		66.667	MHz
Operating Supply Voltage <sup>1</sup>	$V_{DD}$	4.5	5.0	5.5	V
Absolute Maximum Supply Voltage		-0.7		7.0	V
Supply Current, Output Enabled	$I_{DD}$			40	mA
Output Logic Levels					
Output Logic High <sup>2</sup>	$V_{OH}$	$0.9 \cdot V_{DD}$			V
Output Logic Low <sup>2</sup>	$V_{OL}$			$0.1 \cdot V_{DD}$	V
Output Rise/Fall Time <sup>2</sup>	$t_R/t_F$			8	ns
Duty Cycle <sup>3</sup> (ordering option)	SYM		40/60 or 45/55		%
Operating Temperature (ordering option)	$T_{OP}$		0/70 or -40/85		°C
Storage Temperature	$T_{STOR}$	-55		125	°C
Stability <sup>4</sup> (ordering option)	$\Delta F/T$		$\pm 50, \pm 100$		ppm
Output Enable/Disable <sup>5</sup>	E/D				V
Output Enabled		4.0			
Output Disabled				0.8	
Start-up time	$T_{SU}$			10	ms

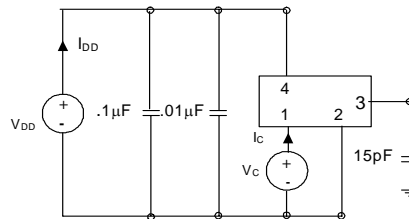
**Table 2. Electrical Performance, 3.3V option**

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	$f_O$	1.000		66.667	MHz
Operating Supply Voltage <sup>1</sup>	$V_{DD}$	2.97	3.3	3.63	V
Absolute Maximum Operating Voltage		-0.5		5.0	V
Supply Current, Output Enabled	$I_{DD}$			40	mA
Output Logic Levels					
Output Logic High <sup>2</sup>	$V_{OH}$	$0.9 \cdot V_{DD}$			V
Output Logic Low <sup>2</sup>	$V_{OL}$			$0.1 \cdot V_{DD}$	V
Output Rise/Fall Time <sup>2</sup>	$t_R/t_F$			8	ns
Duty Cycle <sup>3</sup> (ordering option)	SYM		40/60 or 45/55		%
Operating Temperature (ordering option)	$T_{OP}$		0/70 or -40/85		°C
Storage Temperature	$T_{STOR}$	-55		125	°C
Stability <sup>4</sup> (ordering option)	$\Delta F/T$		$\pm 50, \pm 100$		ppm
Output Enable/Disable <sup>5</sup>	E/D				V
Output Enabled		2.0			
Output Disabled				0.5	
Start-up time	$T_{SU}$			10	ms

1. A 0.01 $\mu$ F and a 0.1 $\mu$ F capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 3 defines these parameters. Figure 4 illustrates the operating conditions under which these parameters are tested and specified. For  $f_O > 90$  MHz, rise and fall time is measured 20 to 80%.
3. Symmetry is measured defined as On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration.
5. Output will be enabled if enable/disable is left open.



**Figure 3. Output Waveform**



**Figure 4. Typical Output Test Conditions (25 $\pm$ 5°C)**

### Enable/Disable Functional Description

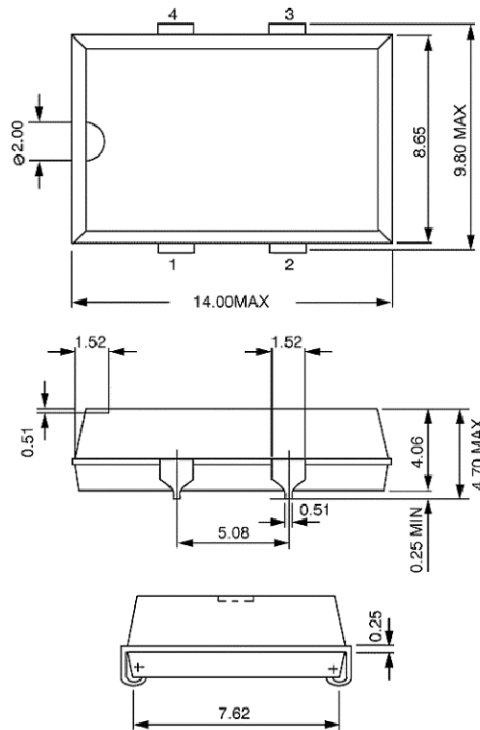
Under normal operation the Enable/Disable is left open or set to a logic high state. When the E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting.

### Tri-state Functional Description

Under normal operation the tri-state is left open or set to a logic high state. When the tri-state is set to a logic low, the oscillator remains active but the output buffer is in a high impedance state. This helps facilitate board testing and troubleshooting.

### Table 3. Outline Diagrams and Pin Out

Pin #	Symbol	Function
1	E/D or NC	Tri-state, Enable/Disable or NC
2	GND	Electrical and Case Ground
3	$f_o$	Output Frequency
4	$V_{DD}$	Supply Voltage



Pin #	Function
1	NC/3-State
2	GND
3	OUT
4	VDD

Figure 5, Package drawing

## VCE1 Data Sheet

### Reliability

The VCE1 qualification tests have included:

**Table 4. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2022
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015

### Handling Precautions

Although ESD protection circuitry has been designed into the the VCE1, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

**Table 5. ESD Ratings**

Model	Minimum	Conditions
Human Body Model	1000	MIL-STD-883 Method 3115
Charged Device Model	1500	JESD 22-C101

### Suggested IR profile

Devices are built using lead free epoxy, but are only rated for a maximum 240°C reflow. A typical reflow profile is shown below in Figure 6.

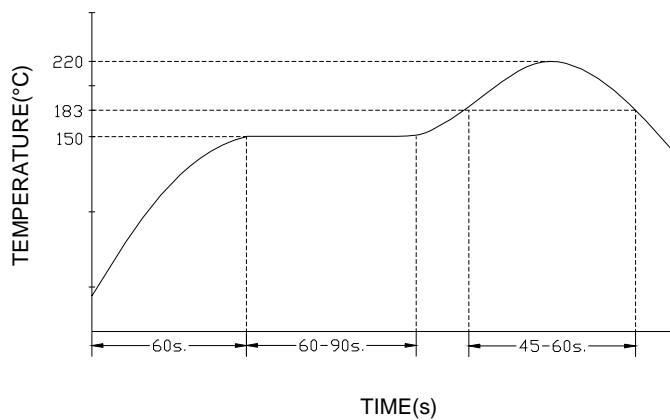
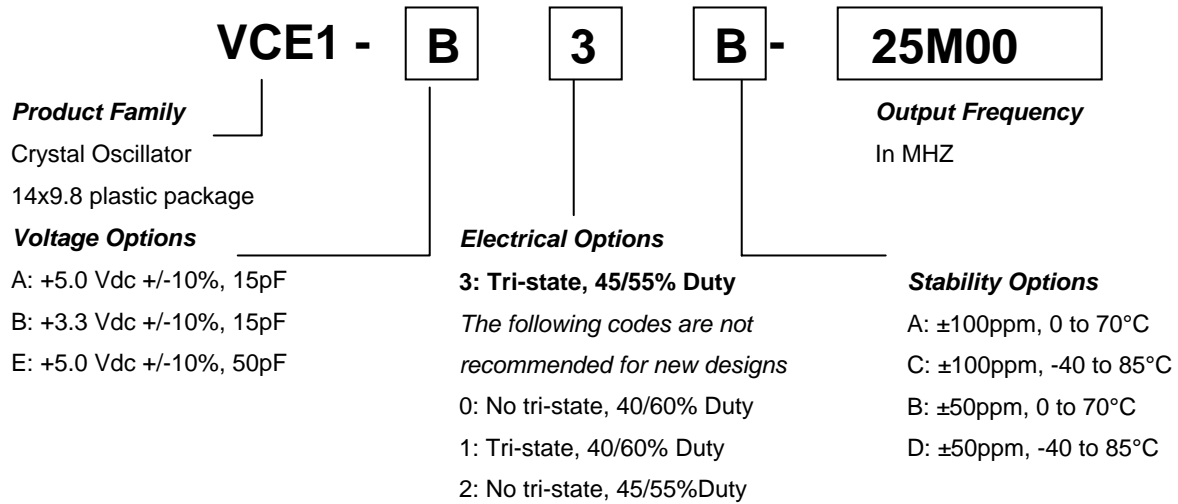


Figure 6. Suggested Reflow Profile

**Ordering Information:**



**Note: Not all combinations are available.**

*Tri-state with a 45/55% is the most common Electrical code and is recommended for most applications.*

*Devices will be shipped in Anti Static Tubes*

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