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Ethernet Switching Physical Layer Software Intellectual Property Signal Integrity Legacy

Dual Channel WAN/LAN/Backplane XAUI to SFP+/KR Transceiver with VeriTimeTM

Part of the SynchroPHY suite of 1GE, 10GE and 10GE OTN devices is the is the VSC8488-15 with VeriTime, Vitesse's patent-pending distributed timing technology that delivers the industry's most accurate IEEE 1588v2 timing implementation. The device is fully compliant with IEEE 1588v2 for timing-critical applications, including all industry-standard protocol encapsulations.



VSC8488 is a dual channel XAUI-to-serial transceiver that delivers minimum cost per channel with maximum port densities at the lowest power. The device achieves an excellent 1 W per channel power dissipation while supporting the increased port densities required for next-generation 10 Gbps platforms. VSC8488 integrates Vitesse's world-class electronic dispersion compensation (EDC) performance across multiple data rates: 9.95 Gbps WAN, 10.3 Gbps Ethernet (GbE), and 10.5 Gbps Fibre Channel. The device also meets the SFP+ SR/LR/LRM host requirements in accordance with the SFF-8431 and IEEE 802.3aq specifications. The EDC capabilities are optimized by the VScope[™] input signal monitoring integrated circuit, which delivers more accurate, in-line views of the post-equalization waveform. VSC8488 compensates for optical impairments in SFP+ LRM applications, along with degradations of the PCB, while providing wide system margin for SR and LR applications. The transmit path incorporates a multi-tap output driver to provide the flexibility required to meet the demanding 10GBASE-KR (IEEE 802.3ap) standard.

Product Variants	Description
VSC8488YJU	[NRND] 196-pin 15 x 15 mm FCBGA lead-free
VSC8488XJU	[NRND] 196-pin 15 x 15 mm FCBGA lead-free second-level interconnect
VSC8488YJU-15	[NRND] 196-pin 15 x 15 mm FCBGA lead-free, 1588 support
VSC8488XJU-15	[NRND] 196-pin 15 x 15 mm FCBGA lead-free second-level interconnect, 1588 support

 Key Features Minimum cost per channel 	
+ Applications	
+ Related Products	

ADDITIONAL RESOURCES

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	Product Brief	VSC8487-15 and VSC8488-15 Product Brief	A	1.0	03/04/2011	1	882 kB
	Product Brief	VSC8488 and VSC8484 Product Brief	ſ	1.1	08/09/2010	7	879 kB
	Datasheet	VSC8488 Datasheet		4.3	01/28/2014	74	3 MB
	Datasheet	VSC8488-15 Datasheet		4.3	01/17/2014	7	4 MB
	Application Note	Encapsulation Support in Vitesse IEEE 1588v2 PHYs	A	1.0	05/12/2014	7	196 kB
	Application Note	IEEE 1588v2 Support in the Vitesse PHY API		1.0	05/12/2014	7	480 kB
	Application Note	IEEE1588 and SyncE Clock Design		1.0	05/12/2014	1	244 kB
	Application Note	IEEE1588v2 and SyncE - Applications and Operation Using Vitesse's Synchronization Solution	A	3.0	05/12/2014	7	2 MB
	Application Note	One-step and Two-step Systems Using Vitesse 1588v2 PHYs	A	1.0	05/12/2014	7	194 kB
	Application Note	Synchronizing Local Time in Vitesse 1588v2 PHYs	A	1.0	05/12/2014	7	175 kB
	Application Note	VSC8484, VSC8487, VSC8488, VSC8487-15, and VSC8488-15 EDC Firmware Configuration Application Note	A	1.1	07/22/2013	7	198 kB
	Firmware	VSC8484, VSC8487, VSC8488, VSC8487-15, and VSC8488-15 EDC Firmware	A	1.14	10/22/2013	Q	224 kB
	Model	VSC8488 BSDL Model		0.5	06/06/2013	Q	3 kB
	Model	VSC8488-15 BSDL Model	A	1.0	06/06/2013	Q	3 kB
	Reference Design	VSC8488 Orcad Library		1.0	06/10/2013	Q	8 kB
	Software	VSC8484, VSC8487, VSC8487-15, VSC8488, and VSC8488-15 GUI		1.1	10/07/2013	Q	4 MB



White Paper	Precise Timing for Base Stations in the Evolution to LTE	A	00-04	02/19/2013	X	4 MB	
Reports	VSC8487XJU, VSC8487XJU-15, VSC8488XJU, VSC8488XJU-15 Material Composition Declaration		4.0	10/01/2012	1	23 kB	
Reports	VSC8487YJU, VSC8487YJU-15, VSC8488YJU and VSC8488YJU-15 Material Composition Declaration - Bump and Assy - ASE (Printed Bumps)		2.0	02/12/2015	7	21 kB	
Reports	First Level Product Qualification Report for VSC8488XJU		1.0	09/07/2011	7	86 kB	
Reports	First Level Product Qualification Report for VSC8488XJU-15		2.0	09/16/2011	A	87 kB	
Reports	First Level Product Qualification Report for VSC8488YJU - Bump and Assy - ASE (Printed Bumps)		1.0	01/16/2015	7	72 kB	
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