# VC-827

Differential (LVPECL, LVDS) Crystal Oscillator


## Description

Vectron's VC-827 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 1.8 (LVDS) 2.5 or 3.3 volt power supply in a hermetically sealed 3.2x2.5 mm ceramic package.

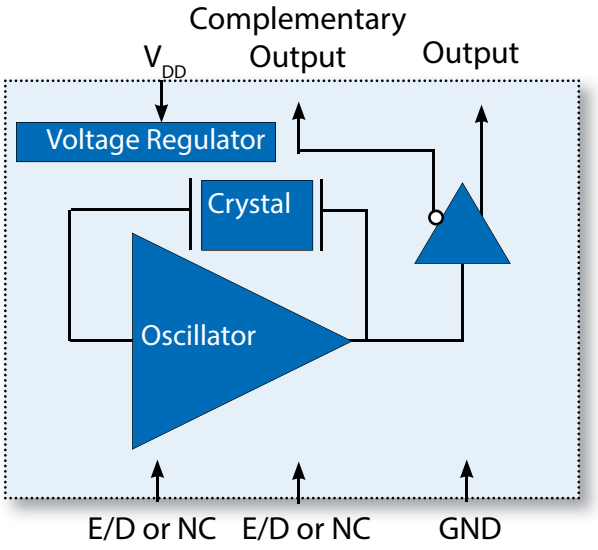
## Features

- Ultra Low Jitter Performance, 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range, -40 to 105°C
- 20MHz -220MHz Output Frequencies
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 1.8 (LVDS), 2.5 or 3.3 V ordering operations
- Hermetically Sealed 3.2x2.5mm Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

## Applications

- Ethernet, GbE, Synchronous Ethernet
- PCIe
- Fiber Channel
- Enterprise Servers and Storage
- Clock source for ADC's, DAC's
- Test and Measurement
- GPON
- Clock source for ADC's, DAC's, FPGA's

## Block Diagram



# Performance Specifications

| Table 1. Electrical Performance, LVPECL Option | | | | | |
|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typical | Maximum | Units |
| Supply Voltage[1] (Ordering Option) | $V_{DD}$ | 3.135<br>2.375 | 3.3<br>2.5 | 3.465<br>2.625 | V<br>V |
| Current Consumption, 3.3V<br>2.5V | $I_{DD}$ | | | 69<br>61 | mA<br>mA |
| **Frequency** | | | | | |
| Nominal Frequency (Ordering Option) | $f_N$ | 20 | | 220 | MHz |
| Stability[2] (Ordering Option) | | ±25, ±50 or ±100 | | | ppm |
| **Outputs** | | | | | |
| Output Logic Levels[3]<br>Output Logic High<br>Output Logic Low | <br>$V_{OH}$<br>$V_{OL}$ | <br>$V_{DD}$-1.025<br>$V_{DD}$-1.810 | | <br>$V_{DD}$-0.880<br>$V_{DD}$-1.620 | <br>V<br>V |
| Output Rise and Fall Time[3,4] | $t_R/t_F$ | | | 500 | ps |
| Load | | 50 ohms into $V_{DD}$-2.0V | | | |
| Duty Cycle[5] | DC | 45 | | 55 | % |
| Phase Noise, 3.3V, 156.25MHz[6]<br>10Hz<br>100Hz<br>1kHz<br>10kHz<br>100kHz<br>1MHz<br>20MHz<br>40MHz | $\phi_N$ | | <br>-80<br>-111<br>-134<br>-147<br>-153<br>-155<br>-156<br>-156 | | dBc/Hz |
| Jitter[6], 156.25MHz<br>12kHz -20MHz | $\phi_J$ | | 95 | 130 | fs |
| **Enable/Disable** | | | | | |
| Outputs Enabled[7]<br>Outputs Disabled | $V_{IH}$<br>$V_{IL}$ | 0.7*$V_{DD}$ | | <br>0.3*$V_{DD}$ | V<br>V |
| Disable Time | $t_D$ | | | 200 | ns |
| Enable/Disable Leakage Current | | | | ±200 | uA |
| Start-Up Time | $t_{SU}$ | | | 10 | ms |
| Operating Temp. (Ordering Option) | $T_{OP}$ | -10/70 or -40/85 or -40/105 | | | °C |

1. The VC-827 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines the test circuit and Figure 2 defines these parameters.
4. Output rise and fall time will be 600ps (max) for -40/105 °C operating temperature range.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C.
7. Outputs will be Enabled if Enable/Disable is left open.

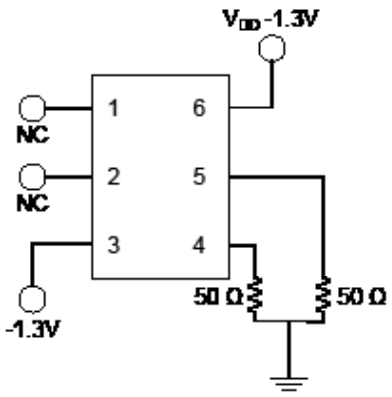



**Figure 1.**

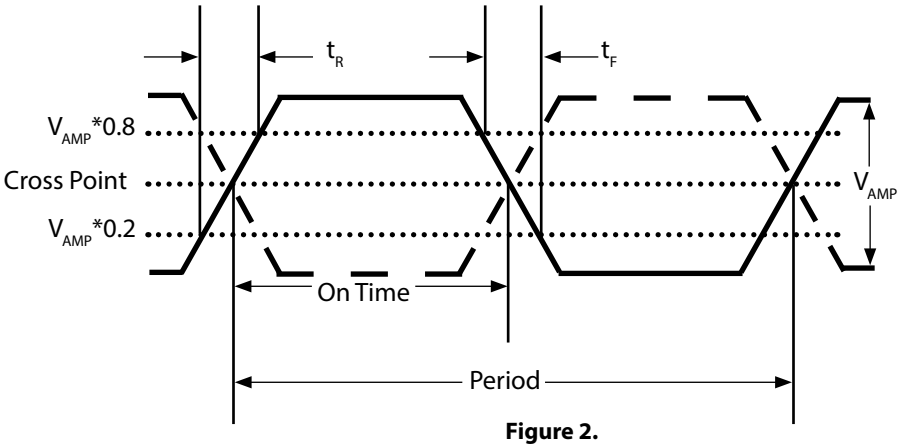



**Figure 2.**

# Performance Specifications

**Table 2. Electrical Performance, LVDS Option**

| Parameter | Symbol | Min | Typical | Maximum | Units |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply Voltage[1] (Ordering Option) | $V_{DD}$ | 3.135<br>2.375<br>1.71 | 3.3<br>2.5<br>1.8 | 3.465<br>2.625<br>1.89 | V<br>V<br>V |
| Current Consumption, 3.3V<br>2.5V<br>1.8V | $I_{DD}$ | | | 33<br>29<br>21 | mA<br>mA<br>mA |
| **Frequency** | | | | | |
| Nominal Frequency (Ordering Option)<br>1.8V | $f_N$ | 20<br>100 | | 220<br>175 | MHz<br>MHz |
| Stability[2] (Ordering Option) | | ±25, ±50 or ±100 | | | ppm |
| **Outputs** | | | | | |
| Output Logic Levels[3]<br>Output Logic High<br>Output Logic Low | <br>$V_{OH}$<br>$V_{OL}$ | <br><br>0.9 | <br>1.43<br>1.10 | <br>1.6<br> | <br>V<br>V |
| Output Amplitude | | 247 | 350 | 454 | mV |
| Differential Output Error | | | | 50 | mV |
| Offset Voltage | | 1.125 | 1.25 | 1.375 | V |
| Offset Voltage Error | | | | 50 | mV |
| Output Leakage Current, Outputs Disabled | | | | 10 | uA |
| Output Rise and Fall Time[3,4] | $t_R/t_F$ | | | 500 | ps |
| Load | | 100 ohms differential | | | |
| Duty Cycle[5] | DC | 45 | | 55 | % |
| Phase Noise, 3.3V, 156.25MHz[6]<br>10Hz<br>100Hz<br>1kHz<br>10kHz<br>100kHz<br>1MHz<br>20MHz<br>40MHz | $\phi_N$ | | <br>-77<br>-107<br>-134<br>-148<br>-154<br>-156<br>-157<br>-157 | | <br>dBc/Hz |
| Jitter[6], 156.25MHz<br>12kHz - 20MHz | $\phi_J$ | | 90 | 125 | fs |
| **Enable/Disable** | | | | | |
| Outputs Enabled[7]<br>Outputs Disabled | $V_{IH}$<br>$V_{IL}$ | 0.7*$V_{DD}$ | | <br>0.3*$V_{DD}$ | V<br>V |
| Disable Time | $t_D$ | | | 200 | ns |
| Enable/Disable Leakage Current | $I_{E/D}$ | | | ±200 | uA |
| Start-Up Time | $t_{SU}$ | | | 10 | ms |
| Operating Temp. (Ordering Option) | $T_{OP}$ | -10/70 or -40/85 or -40/105 | | | °C |

1. The VC-827 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 2 defines these parameters and Figure 3 defines the test circuit.
4. Output rise and fall time will be 600ps (max) for -40/105 °C operating temperature range.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C.
7. Outputs will be Enabled if Enable/Disable is left open.

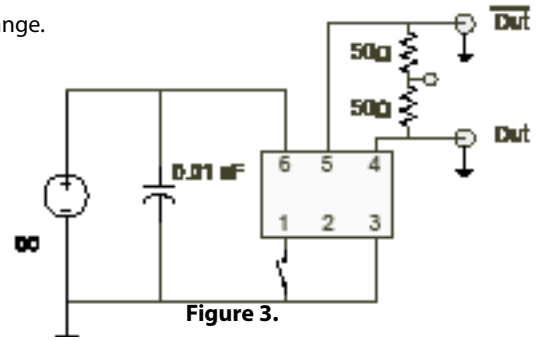
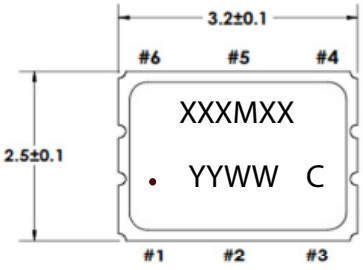
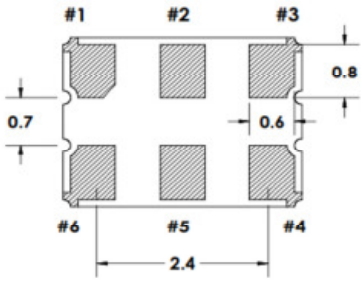
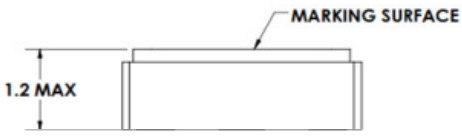



**Figure 3.**

# Package Outline Drawing



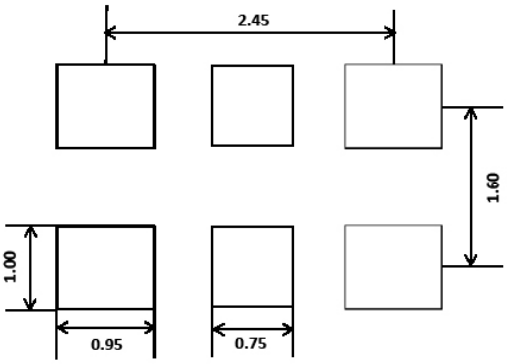




Dimensions in mm

**Marking Information:**
XXXMXX = Frequency (example: 100M00)
YY = Year of Manufacture
WW = Week of the Year
C = Manufacturing Location
• = Pin 1 Indicator

# Recommended Pad Layout




# Pin Diagram

**Table 3. Pinout**

| Pin # | Symbol | Function |
|---|---|---|
| 1 | E/D or NC | Enable/Disable or No Connection |
| 2 | E/D or NC | Enable/Disable or No Connection |
| 3 | GND | Electrical and Lid Ground |
| 4 | $f_O$ | Output Frequency |
| 5 | $Cf_O$ | Complementary Output Frequency |
| 6 | $V_{DD}$ | Supply Voltage |

**Table 4. Enable Disable Function (optional on pin 1 or pin2)**

| E/D Pin | Output |
|---|---|
| High | Clock Output |
| Open | Clock Output |
| Low | High Impedance |

# LVPECL Application Diagrams

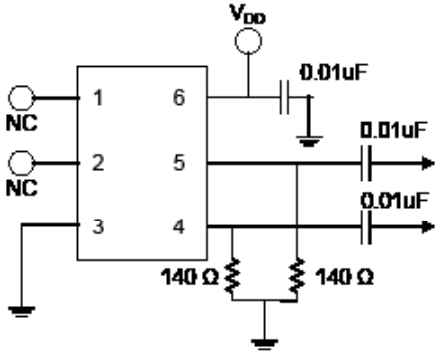



**Figure 4. Single Resistor Termination Scheme**
Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

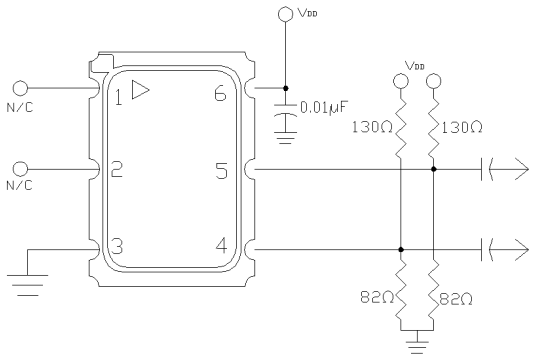



**Figure 5. Pull-Up Pull Down Termination**
Resistor values shown are typical for 3.3 V operation. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 250 ohms

The VC-827 incorporates a standard PECL output scheme, which are un-terminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, or for best 50 ohm matching a pull-up/pull-down scheme as shown in Figure 5 should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## LVDS Application Diagrams

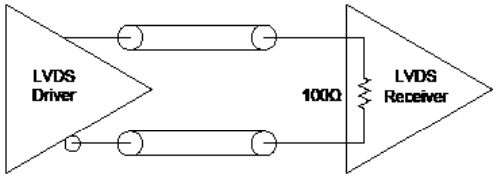



**Figure 6. LVDS to LVDS Connection, Internal 100ohm Resistor**

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

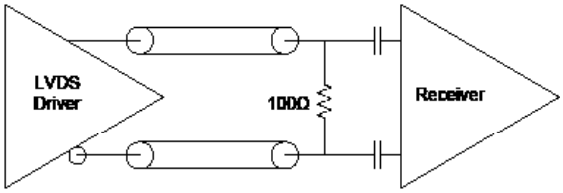



**Figure 7. LVDS to LVDS Connection**

Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

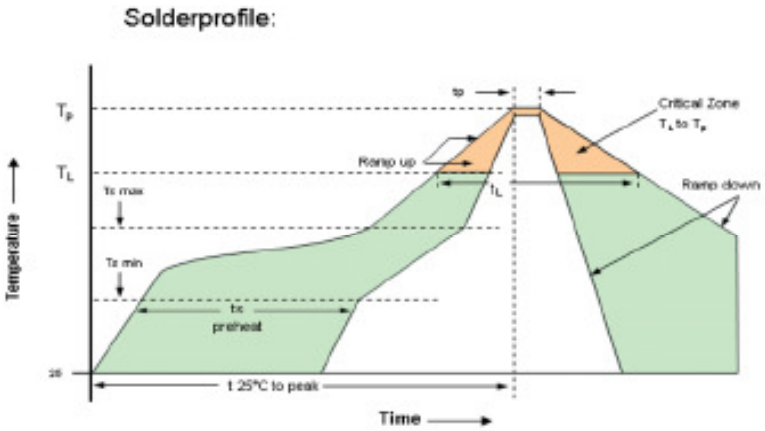
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## IR Compliance

### Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 4. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

| Table 5. Reflow Profile | | |
|---|---|---|
| Parameter | Symbol | Value |
| PreHeat Time | ts | 200 sec Max |
| Ramp Up | $R_{UP}$ | 3°C/sec Max |
| Time above 217°C | tL | 150 sec Max |
| Time to Peak Temperature | tAMB-P | 480 sec Max |
| Time at 260°C | tP | 30 sec Max |
| Time at 240°C | tP2 | 60 sec Max |
| Ramp down | $R_{DN}$ | 6°C/sec Max |



# Environmental Compliance

| Table 6. Environmental Compliance | |
|---|---|
| Parameter | Condition |
| Mechanical Shock | MIL-STD-883 Method 2002 |
| Mechanical Vibration | MIL-STD-883 Method 2007 |
| Temperature Cycle | MIL-STD-883 Method 1010 |
| Solderability | MIL-STD-883 Method 2003 |
| Fine and Gross Leak | MIL-STD-883 Method 1014 |
| Resistance to Solvents | MIL-STD-202 Method 2015 |
| Moisture Sensitivity Level | MSL1 |
| Contact Pads | Gold (0.3-1.0um) over Nickel |
| ThetaJC (bottom of case), Maximum Junction Temperature | 23 °C/W, 150°C |
| Weight | 28 mg |

# Maximum Ratings, Tape & Reel

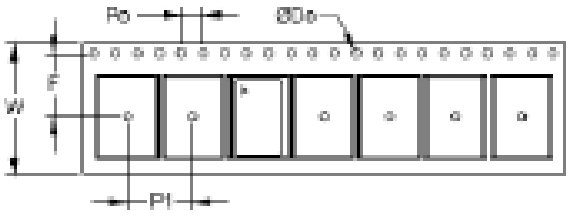
**Absolute Maximum Ratings and Handling Precautions**

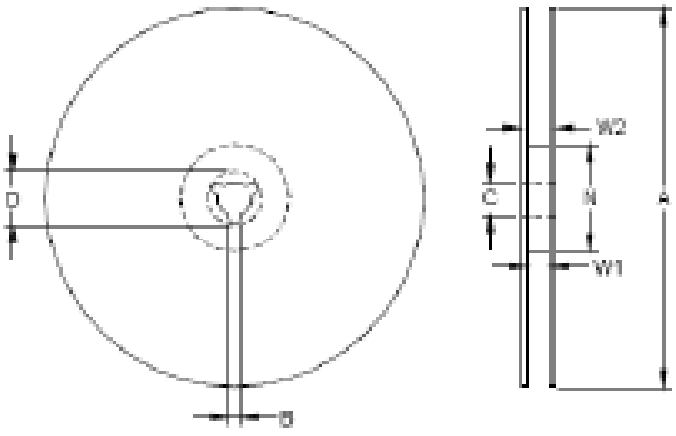
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Although ESD protection circuitry has been designed into the VC-827, proper precautions should be taken when handling and mounting, Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

| Table 7. Maximum Ratings | | |
|---|---|---|
| Parameter | | Unit |
| Storage Temperature | -55 to 125 | °C |
| Junction Temperature | 150 | °C |
| Supply Voltage | -0.5 to 5.0 | V |
| Enable Disable Voltage | -0.5 to $V_{DD}$+0.5 | V |
| ESD, Human Body Model | 1500 | V |
| ESD, Charged Device Model | 1500 | V |

**Table 8. Tape and Reel Information**

| Tape Dimensions (mm) | | | | | Reel Dimensions (mm) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | F | Do | Po | P1 | A | B | C | D | N | W1 | W2 | #/Reel |
| 8 | 3.5 | 1.5 | 4 | 4 | 178 | 2 | 13 | 21 | 60 | 10 | 14 | 3000 |



# Ordering Information

**VC-827- E C E - K A A N - xxxMxxxxxxXX**

**Product**
XO

**Package**
3.2x2.5mm

**Voltage Options**
E: +3.3 Vdc ±5%
H: +2.5 Vdc ±5%
J: +1.8 Vdc ±5% *(LVDS only)*

**Output**
C: LVPECL
D: LVDS

**Temp Range**
W: -10/70°C
E: -40/85°C
F: -40/105°C

**Packaging**
TR: Tape and Reel
blank: Cut Tape / non Tape and Reel quantities
_SNPB: Tin lead solder dipped

**Frequency** in MHz

**Other (Future Use)**
N: Standard

**Enable/Disable Pin**
A: Pin 1 (Pin 2 = No Connection)
B: Pin 2 (Pin 1 = No Connection)

**Enable/Disable Logic**
A: Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low

**Stability**
F: ±25ppm
K: ±50ppm
S: ±100ppm

**Notes:**
a) Only ±100ppm stability option is available for temperature range of -40/105 °C. ±50ppm is available in some cases.
b) Not all combinations of options are available. Other specifications may be available upon request. Consult with factory.

| **Example:** | |
|---|---|
| **VC-827-ECE-KAAN-125M000000TR** | **Tape and Reel** |
| **VC-827-ECE-KAAN-125M000000** | **Cut Tape** |
| **VC-827-ECE-KAAN-125M000000_SNPB** | **Tin lead solder dipped** |

# Revision History

| Revision Date | Approved | Description |
|---|---|---|
| Dec 07, 2016 | RC | Rev 0.0: VC-827 Preliminary datasheet for factory approval (Internal Revision) |
| May 31, 2017 | VN | Rev 0.1: Internal Revision based on factory information |
| June 14, 2017 | VN | Rev 0.2: Initial Product Release in Website |
| Sept 06, 2018 | FB | Update logo and contact info, add thetaJC, add SNPBDIP ordering option |
| May 09, 2019 | FB | Update logo and contact information, change to SNPB ordering option, increase frequency range to 220MHz |
| Dec 10, 2019 | FB | Add 1.8V LVDS ordering option and maximum junction temperature |
| April 30, 2020 | FB | Add tape and reel ordering option, updates and corrections as needed |

# Contact Information


***USA:***
100 Watts Street
Mt Holly Springs, PA 17065
Tel: 1.717.486.3411
Fax: 1.717.486.5920

***Europe:***
Landstrasse
74924 Neckarbischofsheim
Germany
Tel: +49 (0) 7268.801.0
Fax: +49 (0) 7268.801.281