Semiconductor Devices, Silicon
Hybrid Switching Regulators
High Reliability Types

7

	Test Level T_1	Test Level T_2
PIC 645/646/647	PIC 7513/7514/7515	PIC 7531/7532/7533
PIC 655/656/657	PIC 7516/7517/7518	PIC 7534/7535/7536

Contents

Microsemi Corp.
Watertown
The diode experts

1.0 SCOPE

This specification defines the detail requirements for High Reliability Hybrid Switching regulators. Very extensive 100% testing for parameter stability has been included in the Quality Assurance Provisions.

1.1a Absolute Maximum Ratings

	T_1 PIC7513 / T_2 PIC7531 (PIC645)	T_1 PIC7514 / T_2 PIC7532 (PIC646)	T_1 PIC7515 / T_2 PIC7533 (PIC647)	T_1 PIC7516 / T_2 PIC7534 (PIC655)	T_1 PIC7517 / T_2 PIC7535 (PIC656)	T_1 PIC7518 / T_2 PIC7536 (PIC657)
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Continuous Output Current, I_1	15A	15A	15A	−15A	−15A	−15A
Peak Output Current	20A	20A	20A	−20A	−20A	−20A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	2°C/W					
Commutating Diode	2°C/W					
Case to Ambient, θ_{C-A}	30.0°C/W					
Operating Temperature Range, T_C	−55°C to +125°C					
Maximum Junction Temperature, T_j	+150°C					
Storage Temperature Range	−65°C to +150°C					

	Test	Symbol	PIC7513/14/15 PIC7531/32/33 Min.	Typ.	Max.	PIC7516/17/18 PIC7534/35/36 Min.	Typ.	Max.	Units	Conditions
1	Current Delay Time	t_{di}	—	35	60	—	35	60	ns	V_{in} = 25V (−25V)
2	Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	V_{out} = 5V (−5V)
3	Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	I_{out} = 7A (−7A)
4	Voltage Storage Time	t_{sv}	—	1200	—	—	1200	—	ns	I_3 = −30mA (30mA) (Note 5)
5	Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 1
6	Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See Notes 1, 2, 4
7	Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
8	On-State Voltage (Note 3)	$V_{4-1\,(on)}$		1.0	1.5	—	−1.0	−1.5	V	I_4 = 7A (−7A), I_3 = −0.03A (0.03A)
9	On-State Voltage (Note 3)	$V_{4-1\,(on)}$	—	2.5	3.5	—	−2.5	−3.5	V	I_4 = 15A (−15A), I_3 = −0.03A (0.03A)
10	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	0.85	1.25	—	−0.85	−1.25	V	I_2 = 7A (−7A)
11	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	0.95	1.75	—	−0.95	−1.75	V	I_2 = 15A (−15A)
12	Off-State Current	I_{4-1}	—	0.1	10	—	−0.1	−10	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	—	10	1000	—	−10	1000	μA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	—	1.0	10	—	−1.0	−10	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	—	500	1000	—	−500	−1000	μA	V_1 = Rated output voltage, T_A = 100°C

Notes:

1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 1). Therefore, Voltage Delay Time (t_{DV}) ≅ t_{di} + t_{ri} and Current Storage Time (t_{si}) ≅ t_{sv} + t_{fv}.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the PIC600 series switching regulators.
3. Pulse test. Duration = ≤ 400 μsec.
4. As can be seen from the switching waveforms shown in Figure 1, no reverse or forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
5. To insure safe operation, the absolute value of I_3 should be a minimum of 30 mA during $t_{(on)}$. Operation with I_3 below 30 mA can permanently damage the device.

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Power Dissipation Considerations

The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.

The switching losses curve presents data for a frequency of 20 kHz. To find losses at any other frequency, multiply by f/20 kHz. The D.C. losses curves present data for a duty cycle of 0.2. To find D.C. losses at any other duty cycle, multiply by D/0.2 for the power switch and by (1-D)/0.8 for the diode.

At frequencies much below 10 kHz the above method for determining the allowable case of ambient temperature becomes invalid and a detailed transient analysis must be performed. Microsemi will supply transient thermal impedance information on request.

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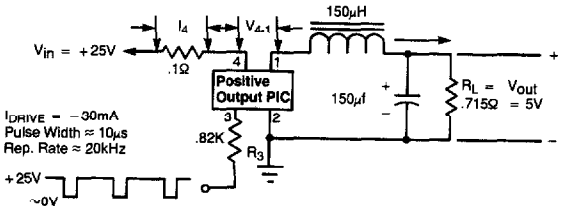
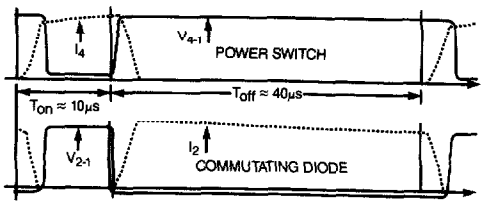


Positive Output Switching Speed Circuit



Note: No Diode Reverse or Forward Recovery Spike (See note 4.)!

Positive Output Switching Waveforms

Note: Negative output circuit and waveforms are identical but of opposite polarity (V_{in} = −25V, V_{out} = −5V, I_{DRIVE} = +30mA).

Figure 1.

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2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of invitations for bids, form a part of this specification to the extent specified herein.

MIL-S-19500 — General Specification for Semiconductor Devices

MIL-S-19491 — Preparation for Delivery of Semiconductor Devices

3.0 REQUIREMENTS

3.1 Design and Construction

The Hybrid devices supplied under this specification shall have a design and construction such that they will meet all of the requirements specified herein. The dimensions and physical characteristics shall be as specified in Figure 2.

3.2 Performance Characteristics

The performance characteristics of the Hybrid device supplied under this specification shall be as specified in Group A inspection *defined in Table I.*

3.3 Quality Assurance

The Quality Assurance Provisions shall be defined in paragraph 4.0.

3.4 Test Methods

Test methods shall be as specified herein.

3.5 Marking

The markings on the devices supplied shall be permanent and legible and shall include the Manufacturer's name or trademark, a Manufacturing Date Code in accordance with MIL-S-19500 and the specific device type number.

3.6 Preparation for Delivery

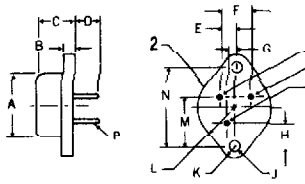
The Hybrid devices supplied under this specification shall be prepared for delivery in accordance with level C of MIL-S-19491 unless otherwise directed in the specific contract or purchase order.

3.7 Ordering Data

Procurement document should specify the following:

a. Specific item type number
b. Number and date of this specification
c. Quality Assurance Test level required
d. Any special packaging if required

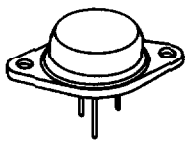
MECHANICAL SPECIFICATIONS



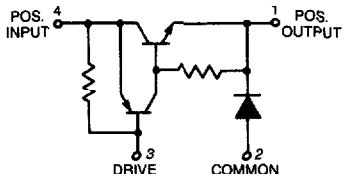
	ins.	mm
A	.875 MAX.	22.23 MAX.
B	.135	3.43
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.205-.225	5.21-5.72
F	.420-.440	10.67-11.18
G	.145-.165	3.68-4.19
H	.395-.405	10.03-10.29
J	.151-.161 DIA.	3.84-4.09 DIA.
K	.188 MAX. RAD.	4.78 MAX. RAD.
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.708-.728	17.98-18.49
N	1.177-1.197	29.90-30.40
P	.038-.043 DIA.	.97-1.09 DIA.

Note: Loads may be soldered to within $1/16''$ of base provided temperature-time exposure is less than 260°C for 10 seconds.

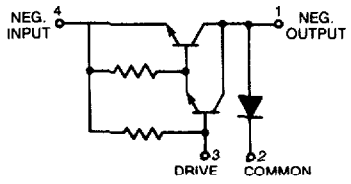
3 Pin TO-3



SCHEMATIC



PIC7513/14/15
PIC7531/32/33



PIC7516/17/18
PIC7534/35/36

Figure 2. Physical Dimensions and Biasing Diagrams

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4.0 QUALITY ASSURANCE PROVISIONS

4.1 General Provisions

4.1.1 Inspection Responsibility — The supplier is responsible for the performance of all inspection requirements and acceptability of results as specified herein for the Test Level identified in the contract or purchase order.

4.1.2 Controlled Manufacture — The devices supplied under this specification shall be manufactured under controlled conditions using formally defined quality assurance methods and systems.

4.1.3 Manufacturing Traceability — Each device supplied under this specification shall be traceable to a specific process group, to permit tracing of its full manufacturing history. Process group records shall indicate the exact date that each manufacturing operation was performed and identify materials and process procedures which were used. The manufacturer shall keep these records on file for at least five years.

4.1.4 Definitions

4.1.4.1 Inspection Lot — An "inspection lot" is a collection of devices from which a sample is withdrawn and inspected to determine compliance with the acceptability criterion. It shall consist of one or more "inspection sublots" of the device types defined in this specification. The maximum inspection lot size shall be 5000 units.

4.1.4.2 Inspection Sublot — An "inspection sublot" shall consist of a collection of devices of a single type which have been manufactured under the same conditions and with the same materials.

4.1.4.3 Shipment Lot — A "shipment lot" shall consist of devices taken from an accepted inspection lot for the purpose of shipment on a specific contract or order.

4.1.4.4 Group A Inspection — Group A inspection shall consist of the examinations and tests specified in Table I, and shall be performed on a sublot basis.

4.1.4.5 Controlled Inventory — The controlled inventory shall consist of lots which have successfully passed the acceptance inspection and are being held in storage prior to actual shipment. A controlled inventory shall have adequate safeguards to insure that no defective or untested devices can be included in it. It shall be accessible only to those individuals who are formally identified as authorized personnel.

4.2 Acceptance Inspection

The acceptance inspection requirements shall be as defined by the applicable test level. The procedures of MIL-S-19500 shall apply to Group A inspection. Inspection lots which have been inspected and accepted shall be kept in a controlled inventory. Shipment lots shall be formed using devices taken from accepted inspection lots.

4.2.1 Test Level T2 Requirements — Test level T2 shall consist of the following requirements.

4.2.1.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Prior to starting the Blocking Stability test defined in paragraph 4.3.6, each device shall be serialized for individual identity. Variables test data for the controlled electrical parameters shall be recorded before and after stressing. The same procedure shall apply for the Power Stress stability test defined in paragraph 4.3.8.

4.2.1.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by variables with test data recorded.

4.2.1.3 With each shipment lot, the supplier shall provide a Certificate of Compliance to test level T2 of this specification.

4.2.2 Test Level T1 Requirements — Test level T1 shall consist of the following requirements.

4.2.2.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Electrical parameter testing as specified shall be performed by attributes.

4.2.2.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by attributes with test data recorded.

4.2.2.3 The supplier shall provide a Certificate of Compliance to test level T1 of this specification with each shipment lot.

4.3 Parameter Stability Tests

Each Hybrid device is to be supplied under this specification and shall receive the following tests in addition to other standard testing performed by the manufacturer.

4.3.1 Temperature Storage — Each Hybrid device shall be subjected, in a non-operating state, to a temperature of 150°C for a minimum period of 48 hours.

4.3.2 Temperature Cycling — Each Hybrid device shall be temperature cycled from −55°C to 150°C for a minimum of 10 cycles. Each cycle shall consist of at least 15 minutes at each temperature extreme with a maximum transition time of 5 minutes between each temperature extreme.

4.3.3 Hermetic Seal Test — Fine Leak — Each Hybrid device shall be tested for a case leakage rate of 1×10^{-8} cc/sec or smaller using a helium mass spectrometer or equivalent method. Devices with a case leakage rate greater than specified shall be removed from the lot.

4.3.4 Hermetic Seal Test — Gross Leak — Each Hybrid device shall be tested for gross leaks using fluorocarbon gross leak test or equivalent method. Devices with any indication of case leakage shall be removed from the lot.

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4.3.5 Reverse Bias Clamp Inductive Test —

V_{4-2} = Rated Input Voltage
I_4 = 5A., f = 25 kHz, E_{out} = 5V
T_C = 25°C, see Figure 4

4.3.6 High Temperature Reverse Bias — Each Hybrid device will be high temperature reversed biased in the circuit shown in Figure 3. The conditions of this test are as follows:

T_A = +125°C
Time = 16 hours $^{+8}_{-0}$ hours
Circuit and voltages as shown in Figure 3 for the appropriate device.

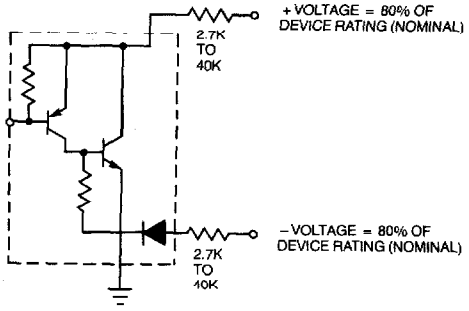
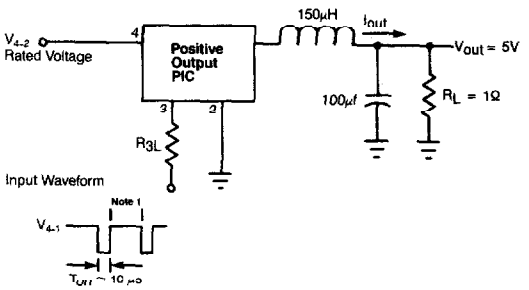


Figure 3. High Temperature Reverse Bias Circuit

4.3.7 The following measurements will be made before and after the high temperature reverse bias test. The unit measurements shall be recorded or the devices will be celled in order to compare and guarantee the delta (Δ) requirements depending on the test level the lot is being prepared to.



Note 1: Adjust T_{off} to obtain specified I_{out}.

Note 2: Negative output test circuits and waveforms are identical but of opposite polarity.

Note 3: R_{3L} = 2KΩ for the PIC 7513/16/31/34
R_{3L} = 2.7KΩ for the PIC 7514/17/32/35
R_{3L} = 3.3KΩ for the PIC 7515/18/33/36

Figure 4. Reverse Bias Clamp Inductive Test Circuit

Type Number	Test 1.1a	Maximum Readings Initial & Final	Delta Change	Symbol
PIC7513/14/15/31/32/33	8	1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7516/17/18/34/35/36	8	−1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7513/14/15/31/32/33	10	1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7516/17/18/34/35/36	10	−1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7513/14/15/31/32/33	12	10μA	±1.0 or ±100%[1]	I_{4-1}
PIC7516/17/18/34/35/36	12	−10μA	±1.0 or ±100%[1]	I_{4-1}
PIC7513/14/15/31/32/33	14	10μA	±2.0 or ±100%[1]	I_{1-2}
PIC7516/17/18/34/35/36	14	−10μA	±2.0 or ±100%[1]	I_{1-2}

[1] Whichever is greater.

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4.3.8 Power Stress — Each Hybrid device shall be burned-in using the circuit shown in Figure 5. The conditions are as follows:

T_A = +25°C
Time = 40 hours minimum
Circuit and conditions as shown in Figure 5.

4.3.9 The readings before and after burn-in shall be as specified in paragraph 4.3.7.

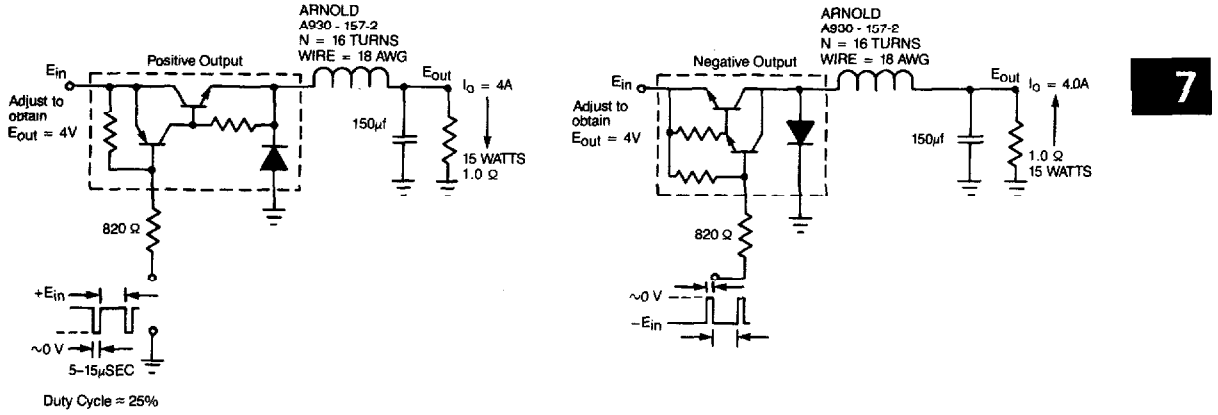

Figure 5. Burn in Circuits

Table I. Group A Inspection

Examination or Test	Symbol	Electrical Spec Test Number	Sample Size (LTPD)	Max. Acc. No.
Subgroup 1				
Visual and Mechanical	—	—	22 (10)	0
Subgroup 2 25°C Tests				
On-State Voltage	$V_{4\text{-}1\ on}$	8	45	0
On-State Voltage	$V_{4\text{-}1\ on}$	9	(5)	
Diode Forward Voltage	$V_{2\text{-}1\ on}$	10		
Diode Forward Voltage	$V_{2\text{-}1\ on}$	11		
Off-State Current	$I_{4\text{-}1}$	12		
Diode Reverse Current	$I_{1\text{-}2}$	14		
Subgroup 3 T_A = +100°C Tests				
Off-State Current	$I_{4\text{-}1}$	13	45	0
Off-State Current	$I_{1\text{-}2}$	15	(5)	
Subgroup 4 25°C Tests				
Current Delay Time	t_{dl}	1		
Current Rise Time	t_{rl}	2		
Voltage Rise Time	t_{rv}	3	45	0
Voltage Fall Time	t_{fv}	5	(5)	
Current Fall Time	t_{fi}	6		