VITESSE®

Making next-generation networks a reality.

PRODUCT BRIEF

VSC7323

VSC7323 Meigs-IIe™ - 10 x 1G and 10G Ethernet MAC Chip

The VSC7323 (Meigs™-IIe) is a versatile building block for a range of high-density Gigabit Ethernet (GbE) and 10 GbE applications within the Enterprise, Metro, and Core. The VSC7323 integrates 10 triple-speed MACs with integrated SerDes, a single 10 Gigabit Ethernet (GbE) MAC with an integrated 10 Gigabit Attachment Unit Interface (XAUI), an OIF-compliant SPI-4.2 interface, a configurable parallel/serial CPU interface, and dual MII Management interface.

Interfacing to the triple-speed MAC ports is accomplished using MII for 10/100 Ethernet support and RGMII/GMII for GbE support. The integrated GbE SerDes enables high density, cost-efficient per port pricing for Ethernet aggregation services.

The full duplex, IEEE 802.3ae-compliant 10 GbE MAC performs pad insertion to ensure minimum frame length and CRC generation as well as preamble, SFD, and IFG insertion on transmit. On the receive side, the 10 GbE MAC performs Ethernet framing, CRC validation, and length monitoring.

The VSC7323 connects seamlessly to 10 Gbps optical modules such as XENPAK, X2, and XPAK using the integrated XAUI compliant serial interface. The quad lane 3.125 Gbps interface implements programmable pre-emphasis on transmit to compensate for inter-symbol interference (ISI) and equalization on receive to ensure reliability in high loss, high distortion environments.

The internal ingress (Rx) and egress (Tx) FIFOs, which are provisionable on a per port basis in increments of 2 kB, are capable of handling short-haul flow control and accommodating bursty traffic between the Ethernet MACs and the SPI-4.2 system interface. The FIFO structures are independently configurable for either cut-through or store-and- forward modes.

The system side of the VSC7323, an industry standard OIF SPI-4.2 interface, is used to seamlessly transfer packet data between the VSC7323 and other devices such as network processors, SONET/SDH mappers, and customer ASICs. The 16-bit SPI-4.2 interface can transmit (ingress) data at 312.5/390.625 MHz DDR and receive (egress) data in the range of 311 to 450 MHz DDR.

The CPU interface can be configured as either a parallel interface for seamless connection to PowerPC™ and Intel™ microprocessors or as a simple 4-line serial interface for device initialization, control register, and per port statistic access. The VSC7323 also integrates two MII Management (MIIM) interfaces for managing and gathering status from the PHY devices.

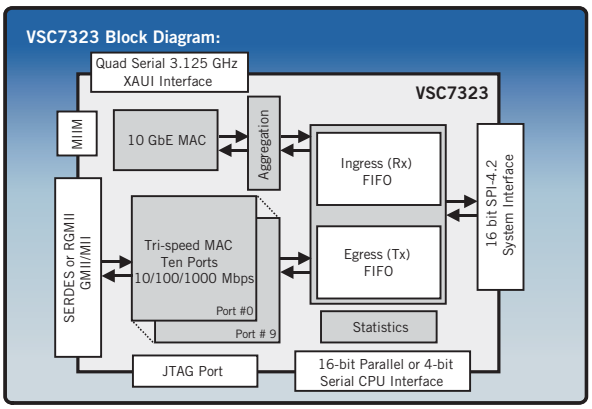
APPLICATIONS

- Enterprise and Metro Ethernet switches
- Multi-service provisioning platforms
- Metro SONET/SDH transport (ADMs)
- Edge and core aggregation routers
- DWDM transport terminals (Wavelength Routers)

SPECIFICATIONS

- Implemented in low power 0.18 micron CMOS technology, 2.5V/3.3V IO
- Industrial Temperature Range (-40ºC to +85ºC)
- Standard 5-Pin P1149.1 JTAG Test Port
- Packaged in a 728-pin TBGA

The VSC7323 is an ideal solution for OEMs designing 10 Gbps or higher solutions that require GbE and 10 GbE support. The VSC7323 also provides a seamless solution for frame-mapped (GFP-F) Ethernet-over-SONET/SDH applications when used in conjunction with Vitesse's VSC9118, a 10 Gbps SONET/SDH VC and GFP Mapper.



Features

- Ten triple-speed Ethernet MACs with support for RGMII/GMII/MII
- Integrated GbE SerDes for direct connection to optical modules
- Intelligent VLAN and MPLS identification
- Loss-less flow control in Metro applications up to 10km
- 10 GbE MAC with integrated XAUI SerDes interface compliant to IEEE 802.3ae
- Low pin count, low power OIF SPI-4.2 system interface
- Extensive loopback capabilities for both line and system side
- Configurable parallel or serial CPU interface
- Dual MIIM interface for managing PHY devices
- Independent egress and ingress shaping/policing
- Rate limiting in 1 Mbps increments
- 802.3ad compliant link aggregation and trunking
- Statistical support for RMON 1 (RFC2819), IEEE 802.3 Annex 30A, and SNMP (RFC 1213, 1573, and 1643)
- Supports both minimum size 64B frames as well as 9600B jumbo frames
- Automatic generation of PAUSE frames based on programmable per port FIFO watermarks

Related Vitesse Products

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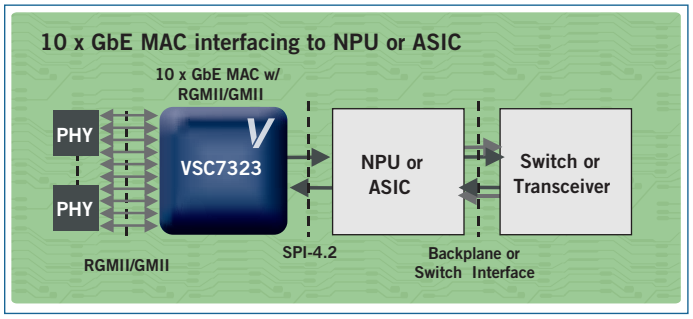
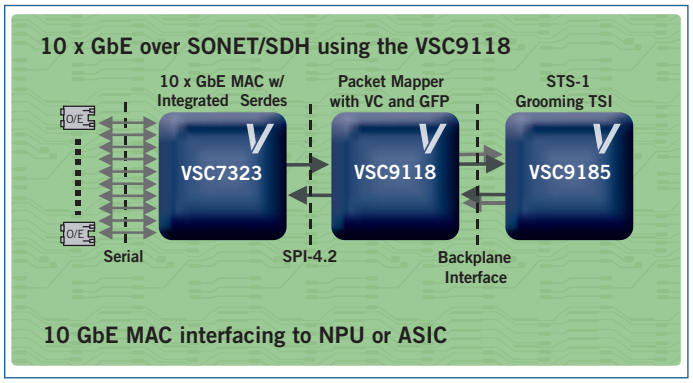
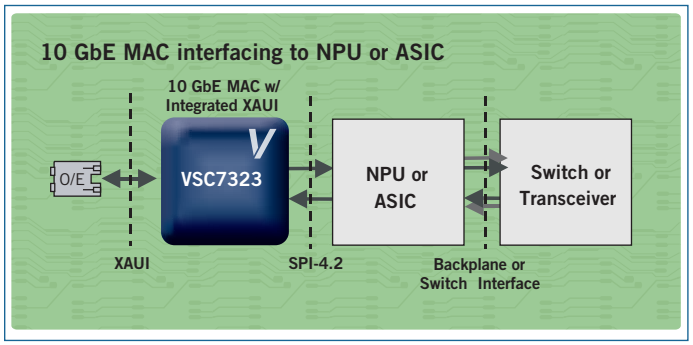
VSC7323 Applications







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