SM803XXX

Flexible Ultra-Low Jitter Clock Synthesizer

Clockworks™ *FLEX2*

General Description

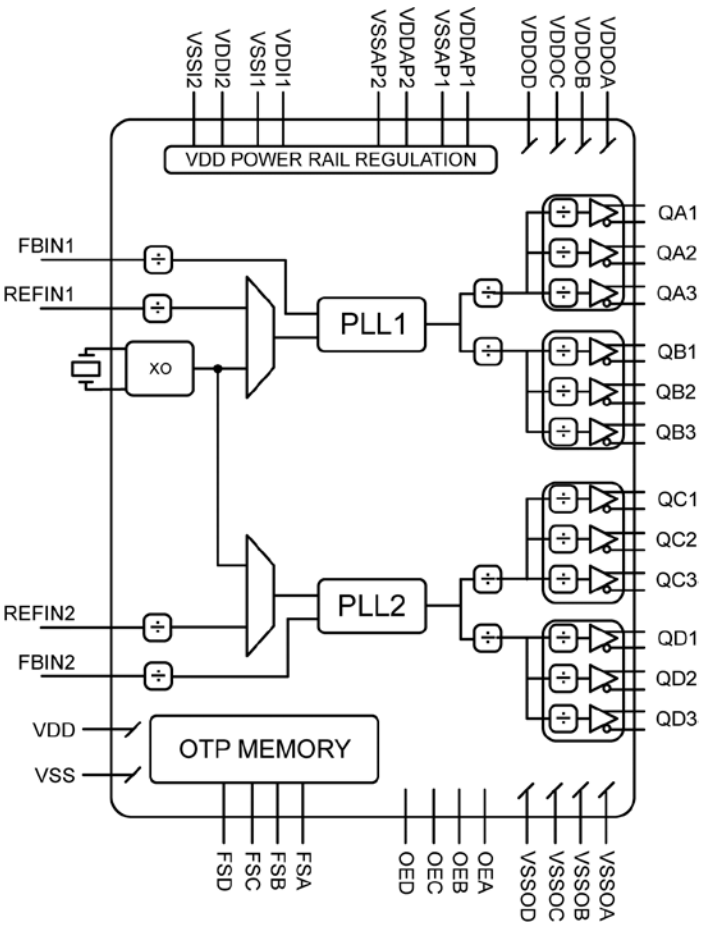
The SM803xxx is a dual-PLL clock generator that achieves ultra-low phase jitter (75fs RMS). With 12 total outputs and dividers on each output, this device can generate 12 different frequencies up to 850MHz, from a low-cost quartz crystal or a reference clock input.

Each of 12 outputs can be independently programmed to LVPECL, LVDS, HCSL, or LVCMOS logic. For LVCMOS, only the true side of the channel is used.

The SM803xxx is packaged in a 48-pin QFN with up to 10 outputs, or 84-pin QFN with 12 outputs.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Generates up to 12 differential or single-ended frequencies
- 75fs phase jitter @ 156.25MHz (1.875MHz to 20MHz)
- 180fs phase jitter @ 156.25MHz (12kHz to 20MHz)
- On-chip power supply regulation for excellent power supply noise immunity
- Two high-performance PLL synthesizers to generate multiple frequencies
- Independently programmable output logic and frequency:
  - Output logic: LVPECL, LVDS, HCSL, LVCMOS
- Selectable input:
  - Crystal: 12MHz to 50MHz
  - Reference input: 12MHz to 850MHz
- SPI programmable (see FLEX SPI documentation)
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Separate output power supplies:
  - Each bank can be at different power supply voltage levels (4 banks of 3 outputs each)
- Feedback input pins for use as zero delay buffer
- Industrial temperature range, –40°C to +85°C
- Green, RoHS, and PFOS compliant QFN packages:
  - 84-pin, 7mm × 7mm (12 Diff. or Single ended outputs)
  - 48-pin 7mm × 7mm (10 Diff. or Single ended outputs)

Applications

- 1/10/40/100 Gigabit Ethernet – (GbE)
- SONET/SDH
- PCI-Express
- CPRI/OBSAI – Wireless base station
- Fibre Channel
- SAS/SATA
- DIMM (DDR2/DDR3/AMB)

Ordering Information

Part Number	Marking	Shipping	Ambient Temperature Range	QFN Package
SM803xxxUMG	803xxx	Tray	–40°C to +85°C	48-pin, 7mm × 7mm
SM803xxxUMGR	803xxx	Tape and Reel	–40°C to +85°C	48-pin, 7mm × 7mm
SM803xxxUMY	803xxx	Tray	–40°C to +85°C	84-pin, 7mm × 7mm
SM803xxxUMYR	803xxx	Tape and Reel	–40°C to +85°C	84-pin, 7mm × 7mm

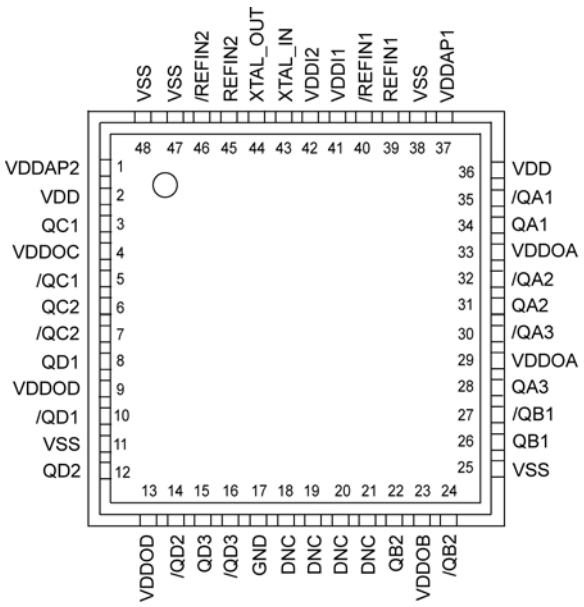
Package Options

Package Option[1]	QFN Package	# of Outputs	OE Control	FSEL Control
#1	48-pin, 7mm × 7mm	10	No	No
#2	48-pin, 7mm × 7mm	8	Yes	No
#3	48-pin, 7mm × 7mm	8	No	Yes
#4	84-pin, 7mm × 7mm	12	Yes	Yes

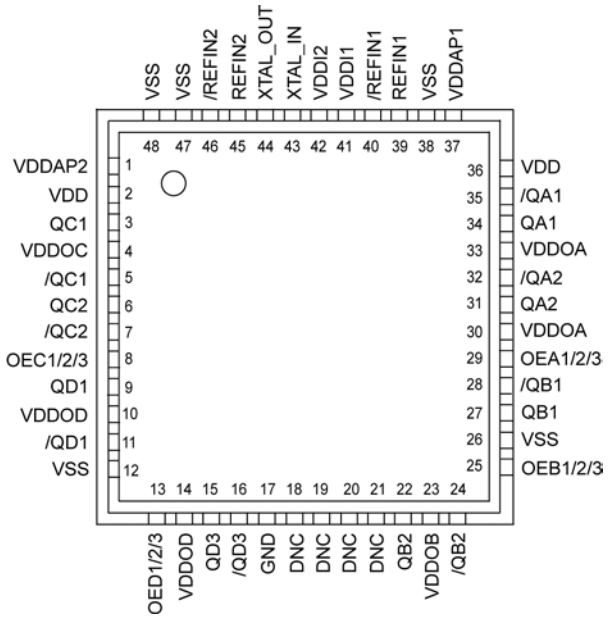
Note:

1. Use the web tool at http://clockworks.micrel.com/micrel/ to determine the desired configuration.

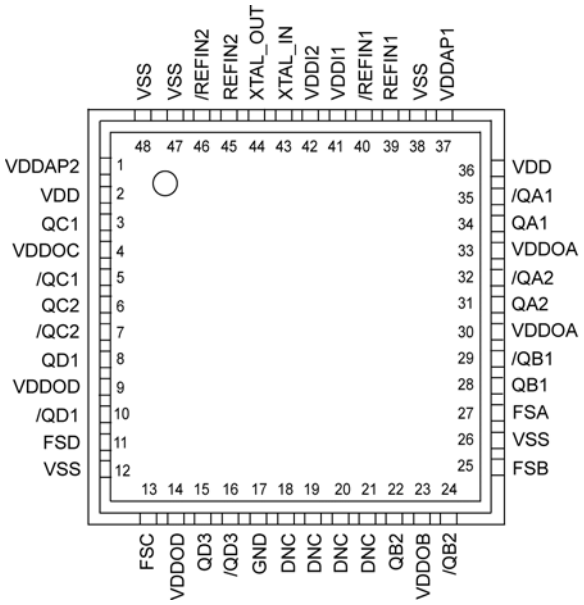
Pin Configurations



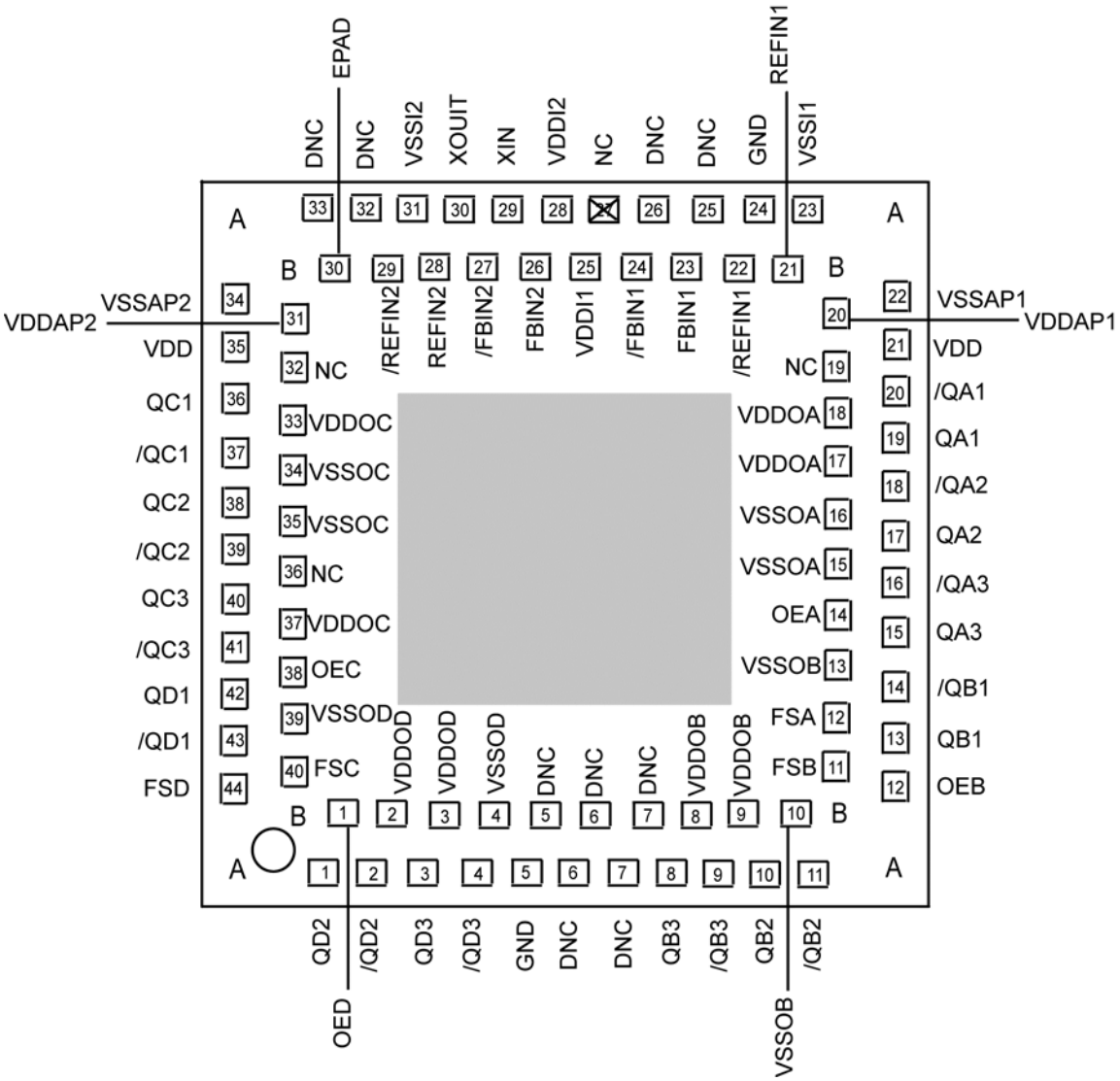
Option #1 (10 outputs)
48-Pin 7mm x 7mm QFN



Option #2 (8 outputs with OE)
48-Pin 7mm x 7mm QFN



Option #3 (8 outputs with FSEL)
48-Pin 7mm x 7mm QFN



Option #4
84-Pin 7mm × 7mm QFN

Pin Description

Pin Numbers by Package Option				Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 84-pin				
34	34	34	A19	QA1	O, (DIF/SE)	LVPECL LVDS HCSL LVCMOS (Q only)	Differential / SE Clock Output (LVCMOS)
35	35	35	A20	/QA1			
31	31	31	A17	QA2			
32	32	32	A18	/QA2			
28			A15	QA3			
30			A16	/QA3			
26	27	28	A13	QB1			
27	28	29	A14	/QB1			
22	22	22	A10	QB2			
24	24	24	A11	/QB2			
			A8	QB3			
			A9	/QB3			
3	3	3	A36	QC1			
5	5	5	A37	/QC1			
6	6	6	A38	QC2			
7	7	7	A39	/QC2			
			A40	QC3			
			A41	/QC3			
8	9	8	A42	QD1			
10	11	10	A43	/QD1			
12			A1	QD2			
14			A2	/QD2			
15	15	15	A3	QD3			
16	16	16	A4	/QD3			
		27	B12	FSA	I, (SE)	LVCMOS	Frequency Select, on-chip 75kΩ pull-up 1 = Primary Selection 0 = Secondary Selection
		25	B11	FSB			
		13	B40	FSC			
		11	A44	FSD			
2	2	2	A21	VDD	PWR		Power Supply
36	36	36	A35				
29	30	29	B18	VDDOA	PWR		Power Supply for Outputs QA1–3
33	33	33	B17				
23	23	23	B8	VDDOB	PWR		Power Supply for Outputs QB1–3
			B9				
4	4	4	B33	VDDOC	PWR		Power Supply for Outputs QC1–3
			B37				
9	10	9	B2	VDDOD	PWR		Power Supply for Outputs QD1–3
13	14	14	B3				

Pin Numbers by Package Option				Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 84-pin				
37	37	37	B20	VDDAP1	PWR		Power Supply for PLL1
1	1	1	B31	VDDAP2	PWR		Power Supply for PLL2
41	41	41	B25	VDDI1	PWR	3.3V only	Power Supply for Input circuits
42	42	42	A28	VDDI2	PWR	3.3V only	Power Supply for Input circuits
11 25 38 47 48 EPAD	12 26 38 47 48 EPAD	12 26 38 47 48 EPAD	A22 A23 A31 A34 B4 B10 B13 B15 B16 B30 B34 B35 B39 EPAD	VSS (Exposed Pad)	PWR		Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
	29		B14	OEA1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QA1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
	25		A12	OEB1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QB1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
	8		B38	OEC1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QC1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
	13		B1	OED1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QD1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
39 40	39 40	39 40	B21 B22	REFIN1 /REFIN1	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input 1
45 46	45 46	45 46	B28 B29	REFIN2 /REFIN2	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input2

Pin Numbers by Package Option				Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 84-pin				
			B23 B24	FBIN1 /FBIN1	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input 1 For Zero Delay Buffer function
			B26 B27	FBIN2 /FBIN2	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input 2 For Zero Delay Buffer function
43	43	43	A29	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed
44	44	44	A30	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed
			A25 A26 A32 A33	DNC			Leave open, do not connect to anything
			A27 B19 B32 B36	NC			Leave open or connect to VSS
18 19 20 21	18 19 20 21	18 19 20 21	A6 A7 B5 B6 B7	SPI	I/O, (SE)	LVCMOS	SPI bus pins for programming. Leave open; for normal operation, do not connect to anything. See FLEX SPI documentation for programming features.
17	17	17	A5 A24	GND	I		These pins are not Power Supply grounds but must be tied to VSS for proper operation.

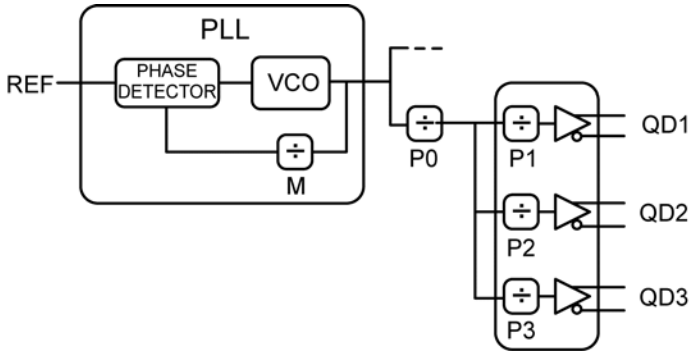
Truth Tables

OEA	OEB	OEC	OED	OUTPUT
0	1	1	1	3 QA outputs tri-state
1	0	1	1	3 QB outputs tri-state
1	1	0	1	3 QC outputs tri-state
1	1	1	0	3 QD outputs tri-state

FSA	FSB	FSC	FSD	OUTPUT FREQUENCY
0	1	1	1	3 QA outputs: Secondary output dividers Other outputs: Primary output dividers
1	0	1	1	3 QB outputs: Secondary output dividers Other outputs: Primary output dividers
1	1	0	1	3 QC outputs: Secondary output dividers Other outputs: Primary output dividers
1	1	1	0	3 QD outputs: Secondary output dividers Other outputs: Primary output dividers

Key Programmable Parameters

Frequency Settings for One PLL and One Output Bank



The REF input frequency can be from a crystal or from a reference clock input. If a crystal is used, the REF input frequency range is 12MHz to 50MHz.

The VCO in the PLL has a range of 2875MHz to 3510MHz.

Counters M and P0 have a range of 4 to 259.
Counters P1, P2 and P3 have a range of 1 to 16.

$F_{VCO} = REF \times M$

$QD1 = F_{VCO} \div (P0 \times P1)$

$QD2 = F_{VCO} \div (P0 \times P2)$

$QD3 = F_{VCO} \div (P0 \times P3)$

Output Logic Programming:

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS.

Each output can be programmed individually to one of the four logic types.

All logic types are differential except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled and the complementary channel is disabled. With LVCMOS there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength.

Unused outputs are disabled to high impedance.

Input Selection

The reference input for the PLLs can be programmed to be either a crystal or a reference clock.

The crystal oscillator circuit has capacitors on the IC so external capacitors are not required.

There are two reference clock inputs, one for each PLL. Make sure they are connected to the same reference input source. The reference inputs can be differential or single-ended and require only a small amplitude. See Figure 1 and Figure 2.

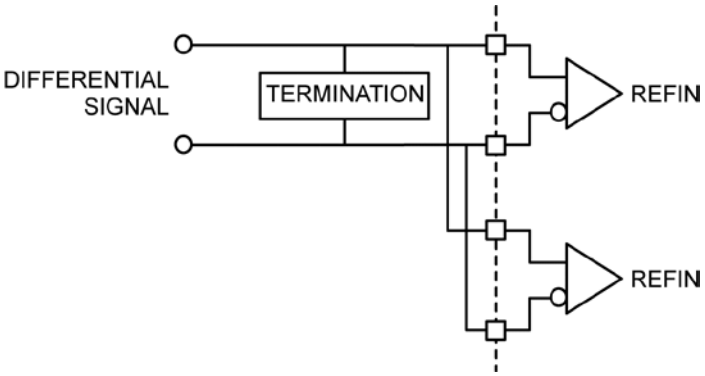


Figure 1. Differential Signal

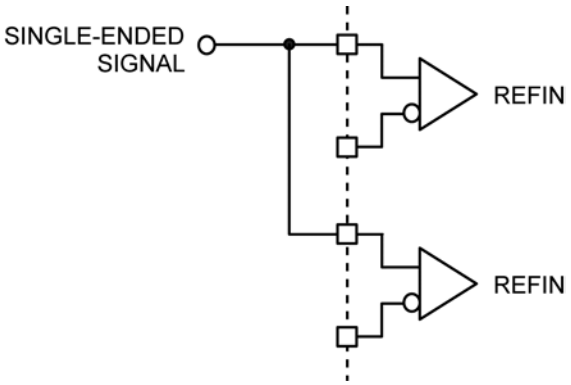


Figure 2. Single-Ended Signal

The single-ended signal input can be LVCMOS, but smaller amplitudes like >800mVpp clipped sine wave from a TCXO will also work.

Frequency Select Programming

Each of the four output banks has a frequency select pin. For each bank, two P0, P1, P2 and P3 counter values can be programmed, a primary and a secondary value. The frequency select pin toggles between the two values assigned to each counter, changing the output frequencies.

Absolute Maximum Ratings[2]

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... -0.50V to 4.6V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Machine Model 200V
ESD Human Body Model 2000V

Operating Ratings[3]

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
QFN (T_{JA}) Still Air ..... 24°C/W

Electrical Characteristics

Typical values are T_A = 25°C, min/max across –40°C≤ T_A ≤ +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDO}	Supply Voltage	2.5V Operation	2.375	2.5	2.625	V
		3.3V Operation	3.135	3.3	3.465	
V_{DDI1}, V_{DDI2}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	PLL Core Voltage		2.375		3.465	V
I_{DDA}	PLL Core Current Consumption	Per active PLL			60	mA
I_{DDI}	Analog Current Consumption				10	mA
I_{DDO}	Output Stage Current Consumption	Per output bank, unloaded			70	mA
I_{DD}	SPI and Miscellaneous Logic				8	mA

LVPECL DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	50Ω to V_{DDO} – 2V	V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V
V_{OL}	Output Low Voltage	50Ω to V_{DDO} – 2V	V_{DDO} – 2	V_{DDO} – 1.78	V_{DDO} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage	Figure 5	0.65	0.77	0.95	V

LVDS DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage	Figure 5	245	350	454	mV
V_{CM}	Common Mode Voltage		1.125	1.2	1.375	V
V_{OH}	Output High Voltage		1.248	1.375	1.602	V
V_{OL}	Output Low Voltage		0.898	1.025	1.252	V

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.

HCSL DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		660	700	850	mV
V_{OL}	Output Low Voltage		–150	0	27	mV
V_{CROSS}	Crossing Point Voltage			350		V

LVCMOS DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO}/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Highest drive (default)	V_{DD} – 0.8			V
V_{OL}	Output Low Voltage				0.5	V
V_{IH}	Input High Voltage		V_{DD} – 0.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{SS} – 0.3		0.3 × V_{DD}	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

REF_IN DC Electrical Characteristics

V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CMR}	Input Common Mode Voltage		0.3		V_{DD} – 0.3	V
V_{SWING}	Input Voltage Swing	Peak to Peak, each side of the Diff Input	0.2			V_{PP}

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF load typical	Fundamental, Parallel Resonant			
Frequency		12		50	MHz
Equivalent Series Resistance (ESR)				60	Ω
Load Capacitance, C_L			12		pF
Shunt Capacitor, C0			2	4	pF
Correlation Drive Level			10	100	µW

AC Electrical Characteristics

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

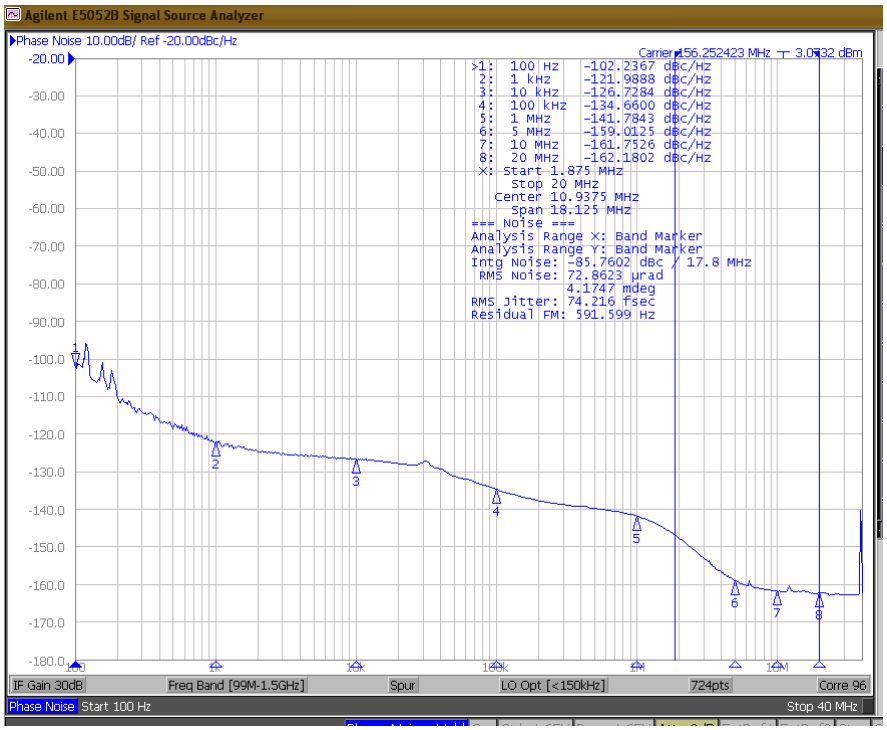
T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{IN}	Input Frequency	XO	12		50	MHz
		Reference input	12		850	MHz
F_{OUT}	Output Frequency	LVPECL, LVDS, HCSL	12		850	MHz
		LVCMOS	12		250	MHz
T_R/T_F	Output Rise/Fall Time[4]	LVPECL output	85	135	350	ps
		LVDS output	85	140	300	ps
		HCSL output	175	340	700	ps
		LVCMOS output (default drive)	100	200	400	ps
ODC	Output Duty Cycle	All output frequencies	45	50	55	%
		< 350MHz output frequencies	48	50	52	%
Tpd	Input to Output Propagation Delay	ZDB mode	–100		100	ps
		Synthesizer/Bypass mode		4		ns
T_{SKEW}	Output-to-Output Skew[5, 6]	Note 6, same output bank			50	ps
T_{LOCK}	PLL Lock Time			5	20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[7, 8]	Integration range (12kHz–20MHz)		182		fs
		Integration range (1.875MHz–20MHz)		74		

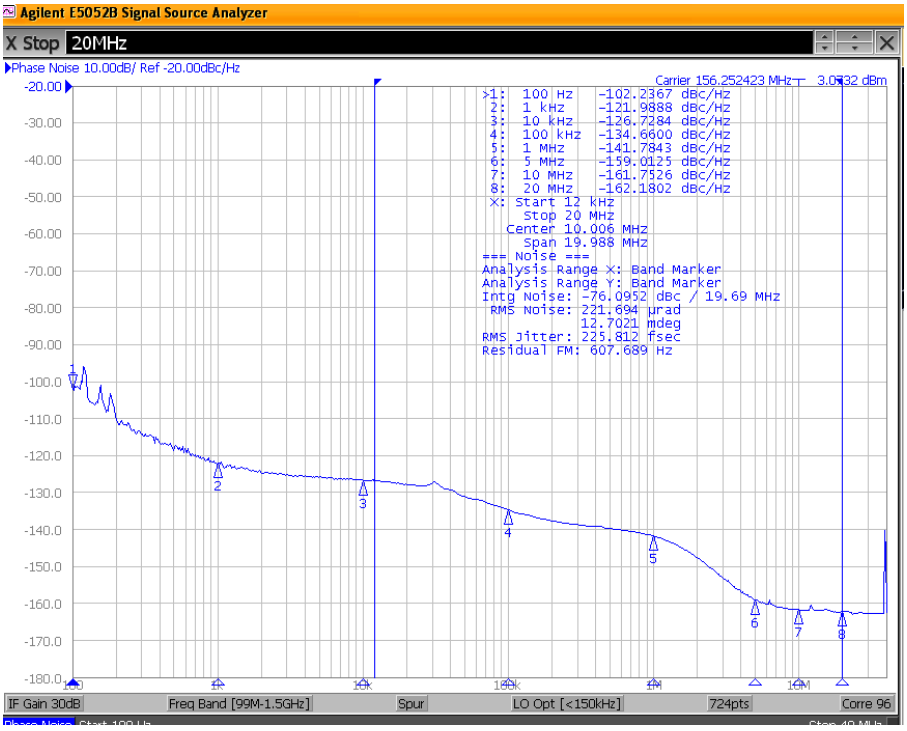
Notes:

4. See Figure 6.
5. Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.
6. Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.
7. All phase noise measurements were taken with an Agilent 5052B phase noise system.
8. Measured using a 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

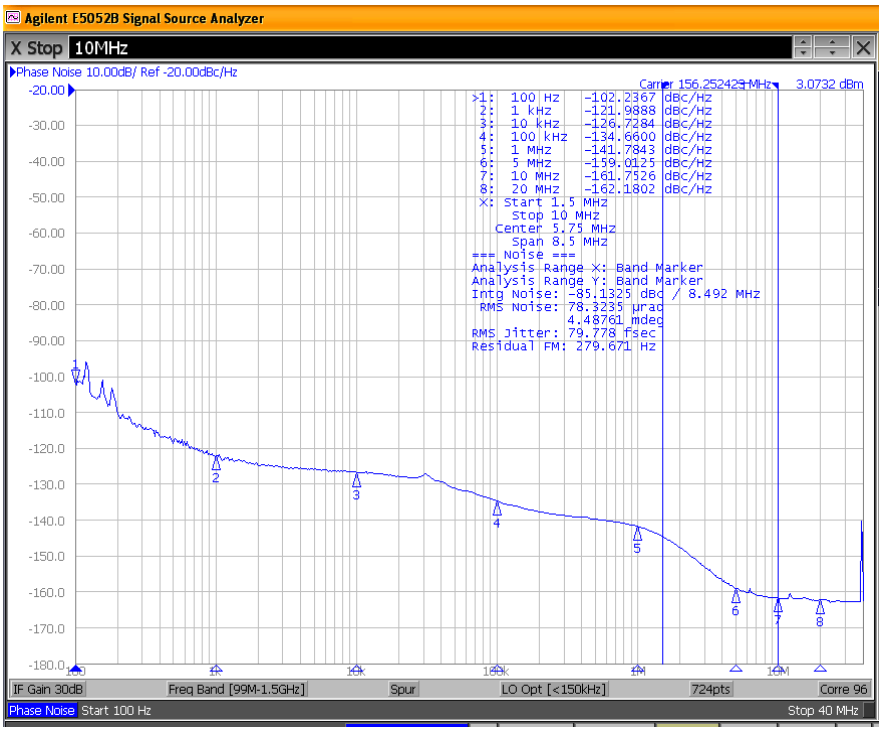
Phase Noise Performance



156.25MHz, Integration Range 1.875MHz to 20MHz: 74.2fs RMS



156.25MHz, Integration Range 12kHz to 20MHz: 182.4fs RMS



156.25MHz, Integration Range 1.5MHz to 10MHz: 79.8fs RMS

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

If you need help selecting a suitable crystal for your application, contact Micrel's HBW applications group at: hbwhelp@micrel.com

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Filtering Recommendations

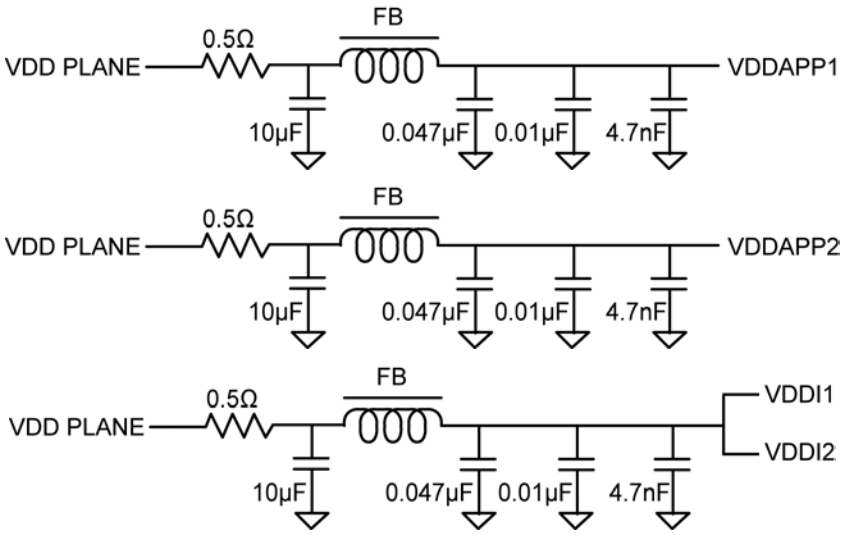


Figure 3. Recommended Power Supply Filtering

- Use the power supply filtering shown in Figure 3 for VDDAP1, VDDAP2, VDDI1 and VDDI2.
- Connect the VDDO and VDD pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 240Ω to 600Ω impedance and >150mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Micrel's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 4 and can be used for any of the above VDD sections.

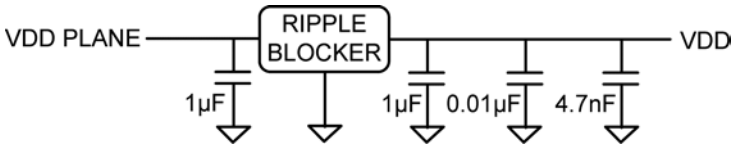


Figure 4. Power Supply Filtering with Ripple Blocker

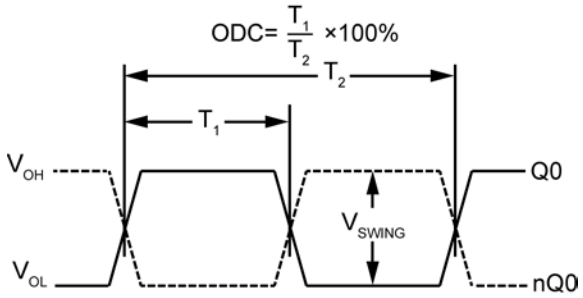


Figure 5. Duty Cycle Timing

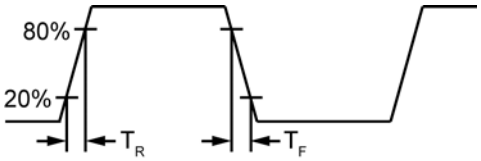


Figure 6. All Outputs Rise/Fall Time

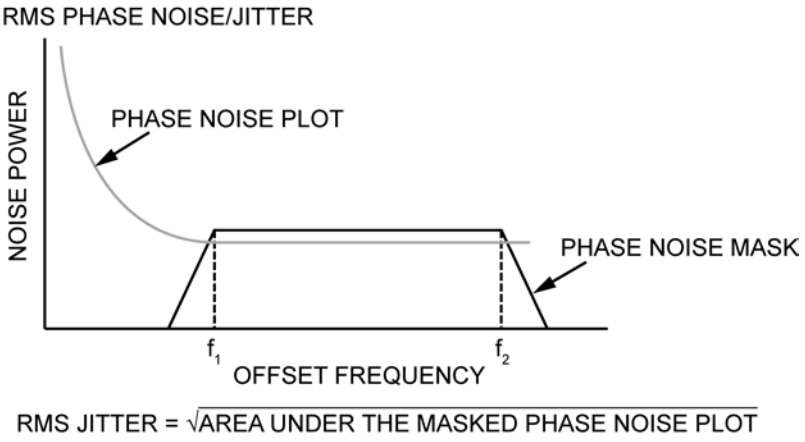


Figure 7. RMS Phase/Noise/Jitter

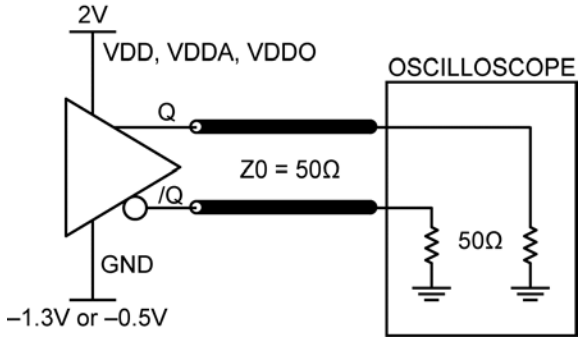


Figure 8. LVPECL Output Load and Test Circuit

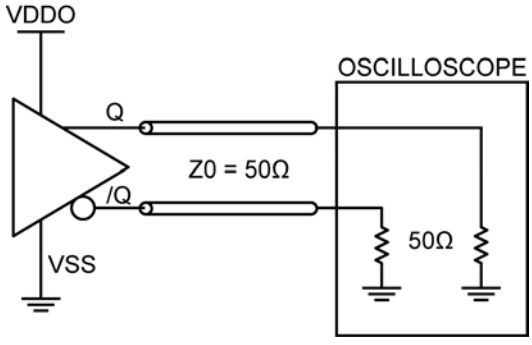


Figure 9. HCSL Output Load and Test Circuit

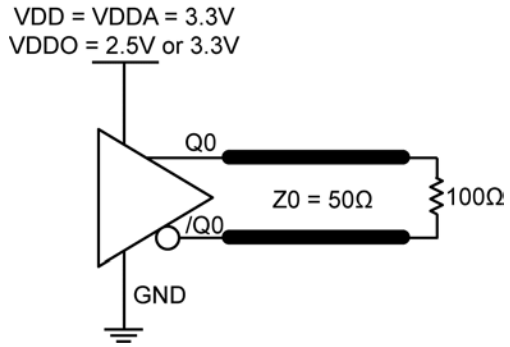


Figure 10. LVDS Output Load and Test Circuit

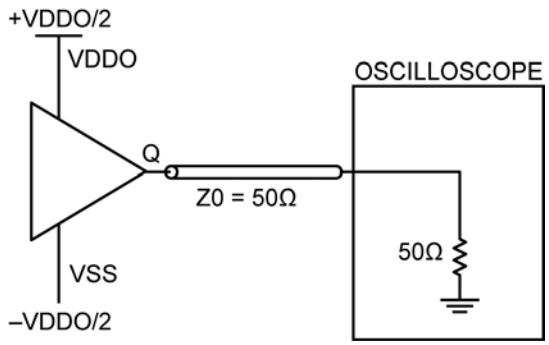


Figure 11. LVCMOS Output Load and Test Circuit

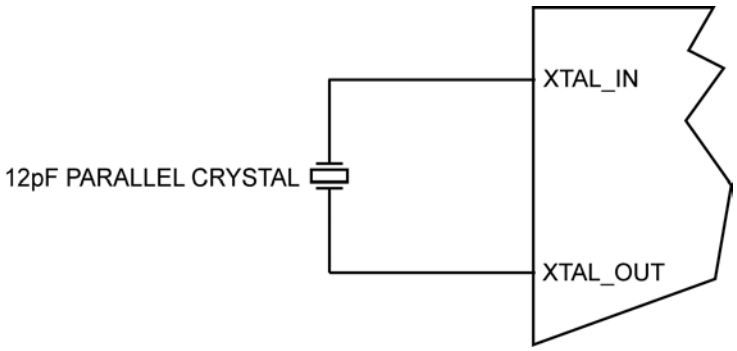
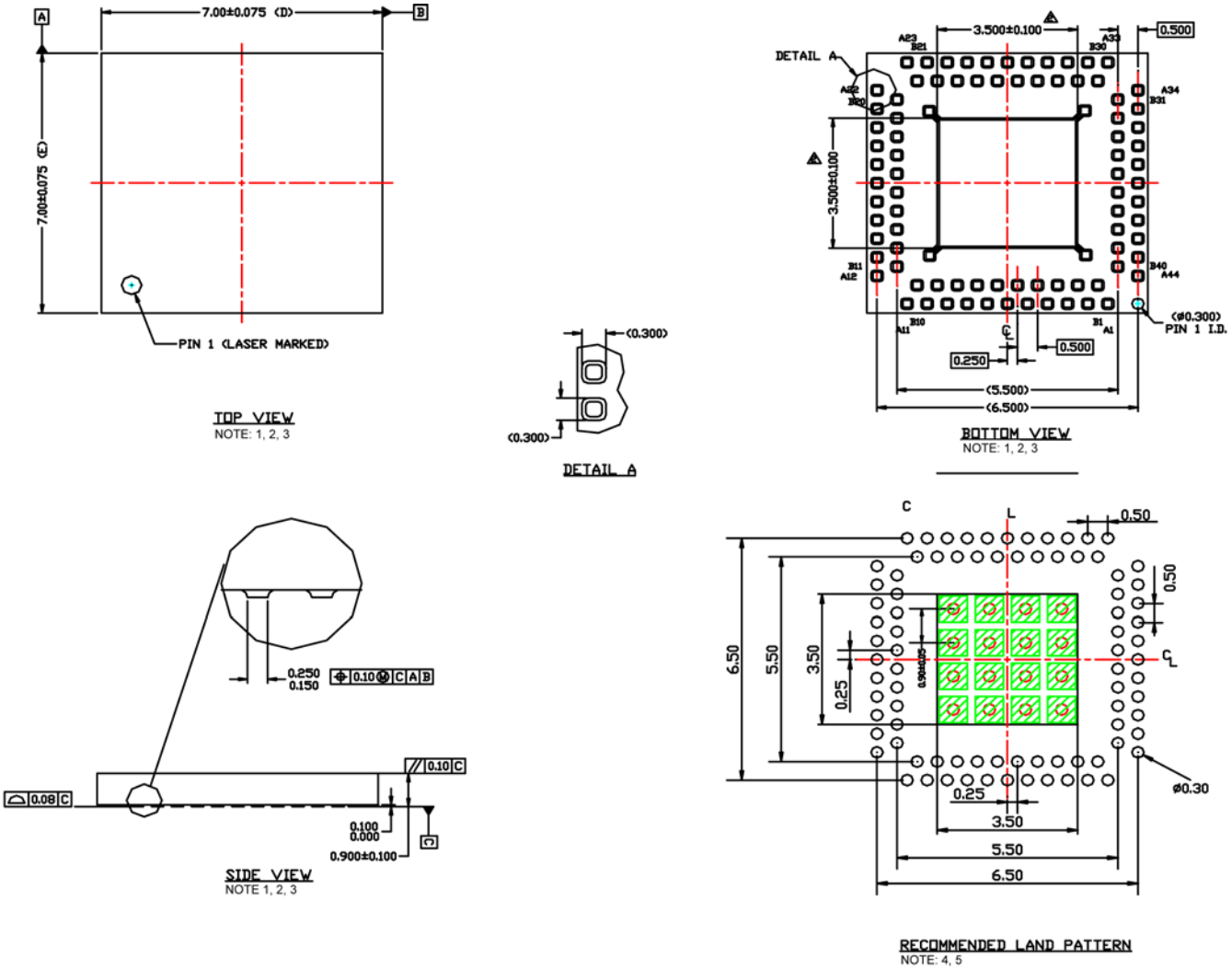


Figure 12. Crystal Input Interface

Package Information and Recommended Land Pattern for 84-Pin QFN[9]



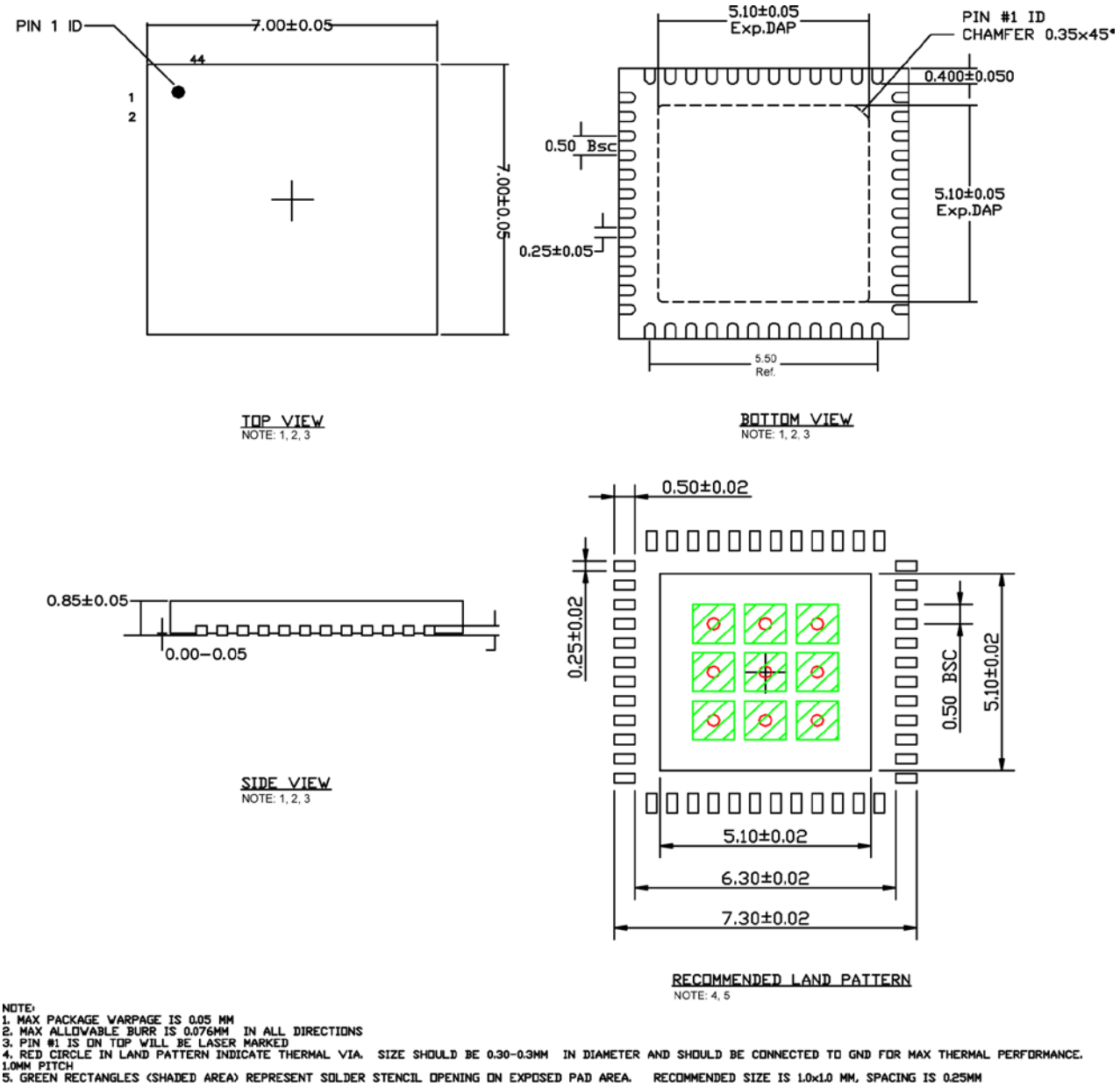
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE. PITCH IS 0.90mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.70x0.70 mm, PITCH IS 0.90 mm.

84-Pin QFN

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Land Pattern for 48-Pin QFN[9]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30~0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.0x1.0 MM, SPACING IS 0.25MM

48-Pin QFN

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