PL902xxx

Revision 1.1

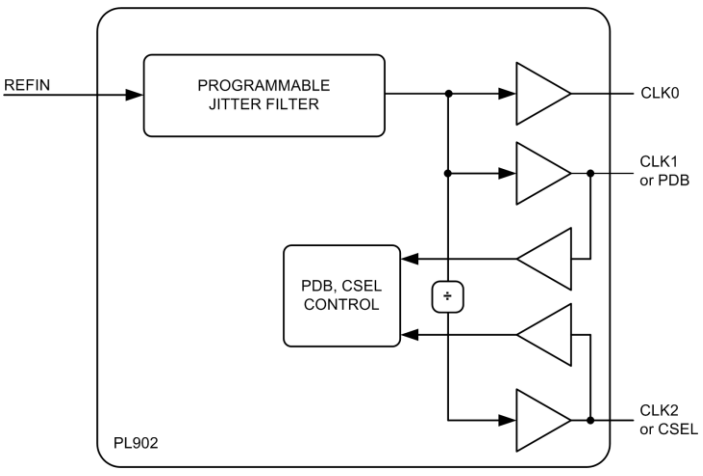
General Description

The PL902xxx series is a low-power, small form-factor, high-performance OTP-based device and a member of Micrel's JitterBlocker, factory programmable jitter attenuators. The JitterBlocker product family cleans any deterministic jitter, thereby improving the peak-to-peak jitter, accumulated jitter, and even the phase noise. The PL902xxx is capable of reducing thousands of picoseconds of period jitter in a clock to a level below 100ps peak-to-peak, making that clock usable for many more applications.

The PL902xxx operates on a single 2.5V or 3.3V supply, consumes little power, and is housed in a small SOT23 package for a broad range of applications. Programmable I/O pins can be configured as output enable (OE), configuration select (CSEL), power down (PDB) input, or CLK1 (2) output. The power down feature of PL902xxx, when activated, allows the IC to consume less than 10µA of power, while its programming flexibility allows filtering of any clock frequency, up to 200MHz.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Lowest power and smallest programmable jitter attenuator
- Input/output frequency up to 200MHz
- I/O pins can be configured as output enable (OE), frequency switching (CSEL), power down (PDB) input, or CLK1(2) output.
- <10µA current consumption with PDB active
- Operating temperature range from –40°C to +85°C
- Available in 6-pin SOT23 GREEN/RoHS-compliant packages.
- Related devices:
  - PL903xxx: Single-ended input, differential output, and phase noise cleaning.
  - PL904xxx: Differential input, two differential outputs, and phase noise cleaning

Applications

- IEEE1588 GPIO clock cleanup
- FPGA-generated clock cleanup
- 1/10/40/100 Gigabit Ethernet (GbE)
- SONET/SDH
- PCI-Express
- CPRI/OBSAI wireless base stations
- Fibre Channel
- SAS/SATA
- DIMM

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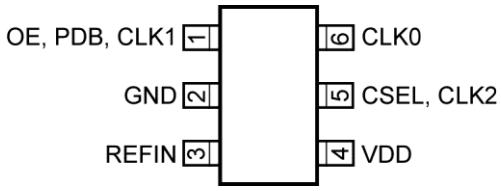
Ordering Information

Part Number	Marking	Shipping	Junction Temp. Range	Package
PL902xxxUSY TR	K2XXX	Tape and Reel	–40° to +85°C	SOT23-6L

Pin Configuration



SOT23-6L (3mm × 3mm × 1.35mm)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	PDB, OE, CLK1	I/O	LVCMOS	Customizable pin: power down or output enable control input with pull-up or clock output.
2	GND	GND		Power supply ground
3	REF_IN	I, (SE)	LVCMOS	Reference clock input
4	VDD	PWR		Power supply
5	CSEL, CLK2	I/O	LVCMOS	Customizable pin: configuration select control input with pull-up or clock output.
6	CLK0	O	LVCMOS	Clock output

Key Programming Parameters

CLK[0:2] Output Frequency	Output Drive Strength	Programmable Input/Output
CLK0 = REFIN CLK1 = CLK0 CLK2 = CLK0, CLK0/2, or CLK0/4 Frequency translation is optional within the specified frequency range.	Three optional drive strengths to choose from: • Low: 4mA • Standard: 8mA (default) • High: 16mA	One output pin can be configured as: • OE – input • PDB – input • CSEL – input • CLK1, 2 – output

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Functional Description

The PL902xxx series is a highly featured, very flexible, advanced programmable jitter filter design for high performance, low-power, small form-factor applications. The PL902xxx accepts a reference clock input between 1MHz and 200MHz and is capable of producing up to three outputs in the 5MHz to 200MHz range. The most common configuration will be comprised of the same input and output frequency, but this flexible design also allows frequency translation from one frequency to another frequency as long as both frequencies are within the specified ranges for input and output.

Jitter Filter Programming

Typically, the jitter filter settings will be optimized for one particular input and output frequency, but the flexible design also allows configurations for a certain frequency range, up to one octave wide.

The typical bandwidth of the jitter filter is 4kHz. This means that jitter frequency components above 4kHz will be attenuated. In case of frequency translation, the bandwidth may be slightly different.

Clock Output (CLK0)

CLK0 is the main clock output. The output drive level can be programmed to low drive (4mA), standard drive (8mA) or high drive (16mA). The maximum output frequency is 200MHz at 3.3V operation and 167MHz at 2.5V operation.

Clock Output (CLK1, CLK2)

The CLK1 and CLK2 feature allows the PL902xxx to have two additional clock outputs programmed to one of the following frequencies:

- CLK1 = CLK0
- CLK2 = CLK0, CLK0/2 or CLK0/4

CLK1 and CLK2 allow the same output drive level programming as CLK0. Because of the extra /2 and /4 settings, CLK2 is capable of going down to 1.25MHz. In case only an output clock of <5MHz is needed, CLK0 and CLK1 can be disabled.

Output Enable (OE)

The output enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60kΩ pull-up resistor, giving a default condition of logic “1”.

Power Down Control (PDB)

The power down (PDB) feature allows the user to put the PL902xxx into sleep mode. When activated (logic “0”), PDB disables the synthesizer circuitry, counters, and all other active circuitry. In power down mode, the IC consumes <10µA of power. The PDB pin incorporates a 60kΩ pull-up resistor giving a default condition of logic “1”.

Configuration Select (CSEL)

The configuration select (CSEL) feature allows the PL902xxx to switch between two pre-programmed configurations allowing the device on-the-fly frequency switching. The CSEL pin incorporates a 60kΩ pull-up resistor giving a default condition of logic “1”.

Examples for this feature are:

- Select between two frequencies or two frequency ranges.
- Select between two frequency translations, like 1:1 and 1:2.

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Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +2.25V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
SOT23 (θ_{JA}), Still-Air ..... 195°C/W

DC Electrical Characteristics

V_{DD} = 3.3V ±10% or 2.5V ±10%; C_L = 15pF; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply current, dynamic	V_{DD} = 3.3V, 30MHz, load = 15pF		12	18	mA
I_{DD}	Supply current, dynamic	When PDB = 0			<10	µA
V_{DD}	Operating voltage		2.25		3.63	V
t_{PU}	Power supply ramp	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.	0.001		100	ms
I_{OLD}	Output current, low drive	V_{OL} = 0.4V, V_{OH} = V_{DD} – 0.9V, V_{DD} = 3.3V	4			mA
I_{OSD}	Output current, standard drive	V_{OL} = 0.4V, V_{OH} = V_{DD} – 0.9V, V_{DD} = 3.3V	8			mA
I_{OHD}	Output current, high drive	V_{OL} = 0.4V, V_{OH} = V_{DD} – 0.9V, V_{DD} = 3.3V	16			mA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.

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AC Electrical Characteristics

V_{DD} = 3.3V ±10% or 2.5V ±10%; C_L = 15pF; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Input (REFIN) frequency	3.3V operation	1		200	MHz
	2.5V operation	1		167	MHz
Input signal amplitude	Internally AC-coupled (high frequency)	0.8		V_{DD}	V_{PP}
Input signal amplitude	Internally AC-coupled (low frequency) 3.3V ≤ 50MHz, 2.5V ≤ 40MHz	0.1		V_{DD}	V_{PP}
Output frequency	CLK0 and CLK1, 3.3V operation	5		200	MHz
	CLK0 and CLK1, 2.5V operation	5		167	MHz
	CLK2, 3.3V operation	1.25		200	MHz
	CLK2, 2.5V operation	1.25		167	MHz
Settling time	At power up (after V_{DD} increases over 2.25V)			1	ms
Output enable time	OE function: T_A = 25ºC, 15pF load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB function: T_A = 25ºC, 15pF load.			1	ms
Output rise time	15pF load, 10/90% V_{DD}, high drive, 3.3V		1.2	1.7	ns
Output fall time	15pF load, 10/90% V_{DD}, high drive, 3.3V		1.2	1.7	ns
Duty Cycle	@ 2.5V and 3.3V over entire frequency range. Threshold = V_{DD}/2	45	50	55	%
Period jitter, peak-to-peak[3] (10,000 samples measured)	With capacitive decoupling between VDD and GND		75		ps
Jitter attenuation bandwidth	CLK0 = REFIN		4		kHz

Notes:

3. Jitter performance can be considered the noise floor of the device. Jitter cannot be attenuated below this value.

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Layout Recommendations

The following guidelines are designed to assist the user to create a performance-optimized PCB design.

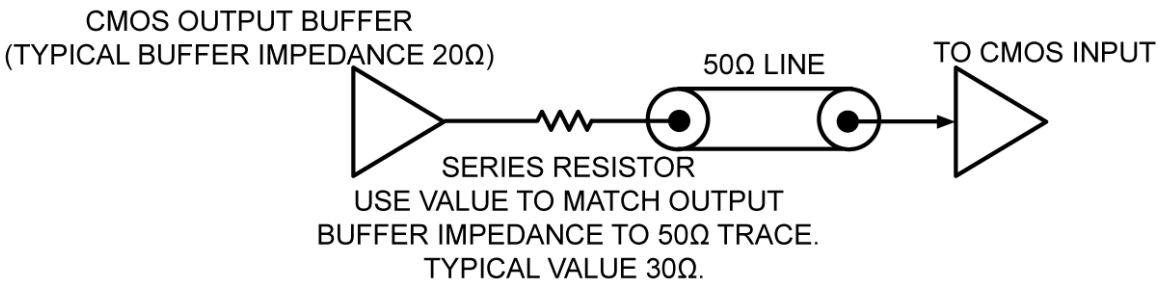
Signal Integrity and Termination Considerations

- Keep traces short for good signal integrity.
- Trace = Inductor. With a capacitive load this causes ringing.
- Long trace = Transmission line. Without proper termination, this will cause reflections that also look like ringing.
- Design long traces (greater than 1 inch) as “striplines” or “microstrips” with defined impedance.
- Match the trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply.
- Multiple VDD pins should be decoupled separately for best performance.
- The addition of a ferrite bead in series with VDD can help prevent noise from other board sources.
- The value of the decoupling capacitor is frequency-dependent. Typical values to use are 0.1µF for designs using frequencies <50MHz and 0.01µF for designs using frequencies >50MHz.

Typical CMOS Termination
Place series resistor as close to CMOS output as possible.



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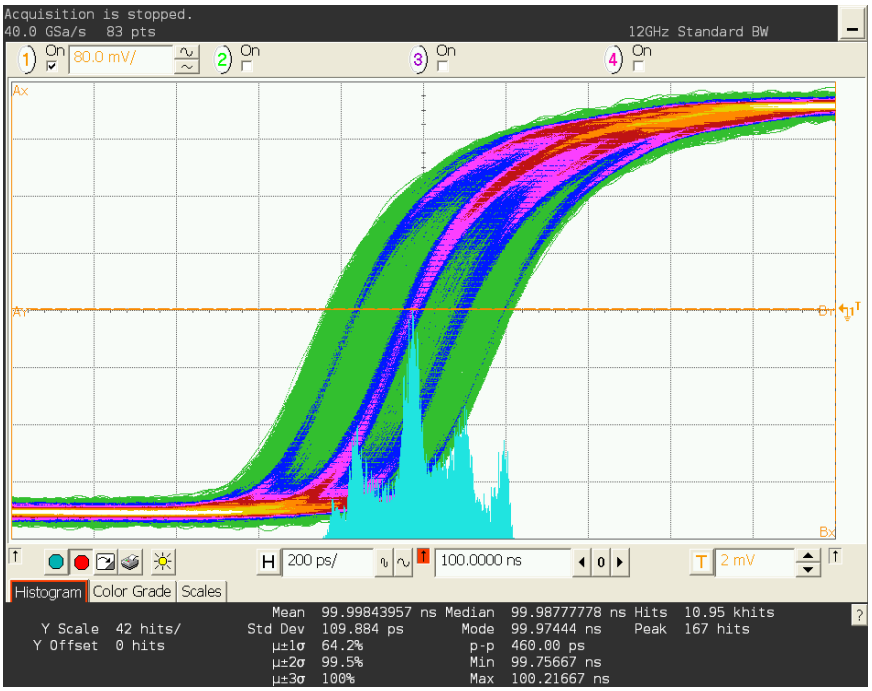
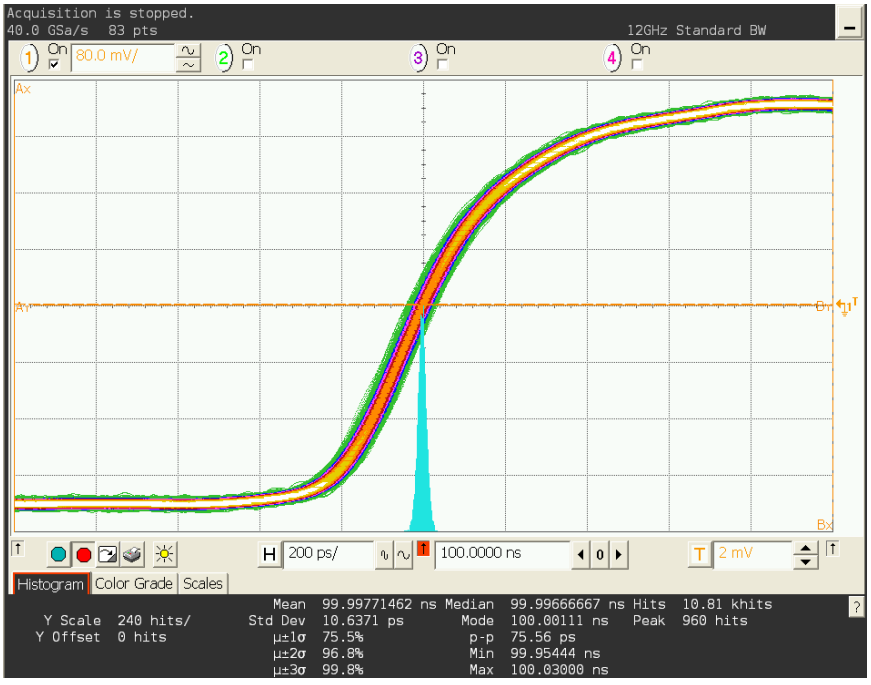
Period Jitter Histogram

10MHz input clock with bad period jitter.



10MHz with 460ps peak-to-peak period jitter

Output clock from JitterBlocker.



10MHz with 75ps peak-to-peak period jitter

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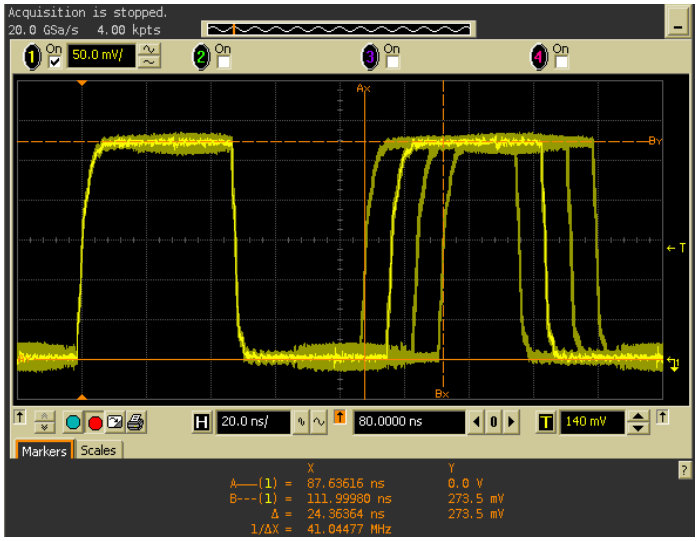
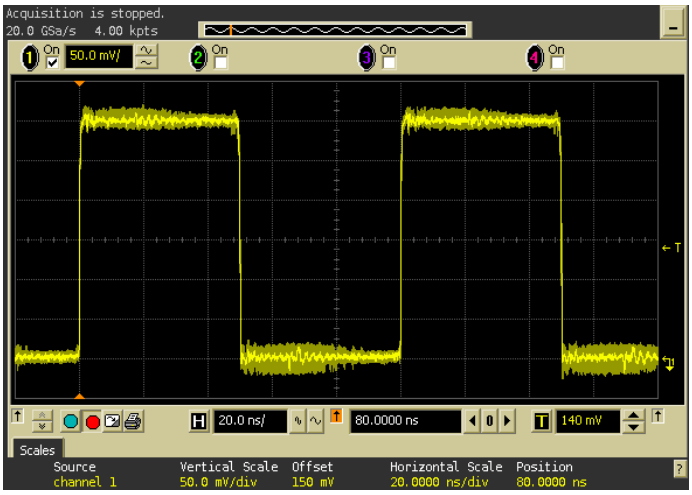
Fixing Extreme Jitter in 10MHz IEEE1588 GPIO Clocks



10MHz clock from IEEE1588



Jitter Blocker output

An IEEE1588 system can manufacture a 10MHz clock from 8ns pulses, but this creates extreme period jitter of about 24ns peak-to-peak in this case. The JitterBlocker cleans that up to 100ps peak-to-peak, allowing the clock to be used in more jitter-sensitive applications.

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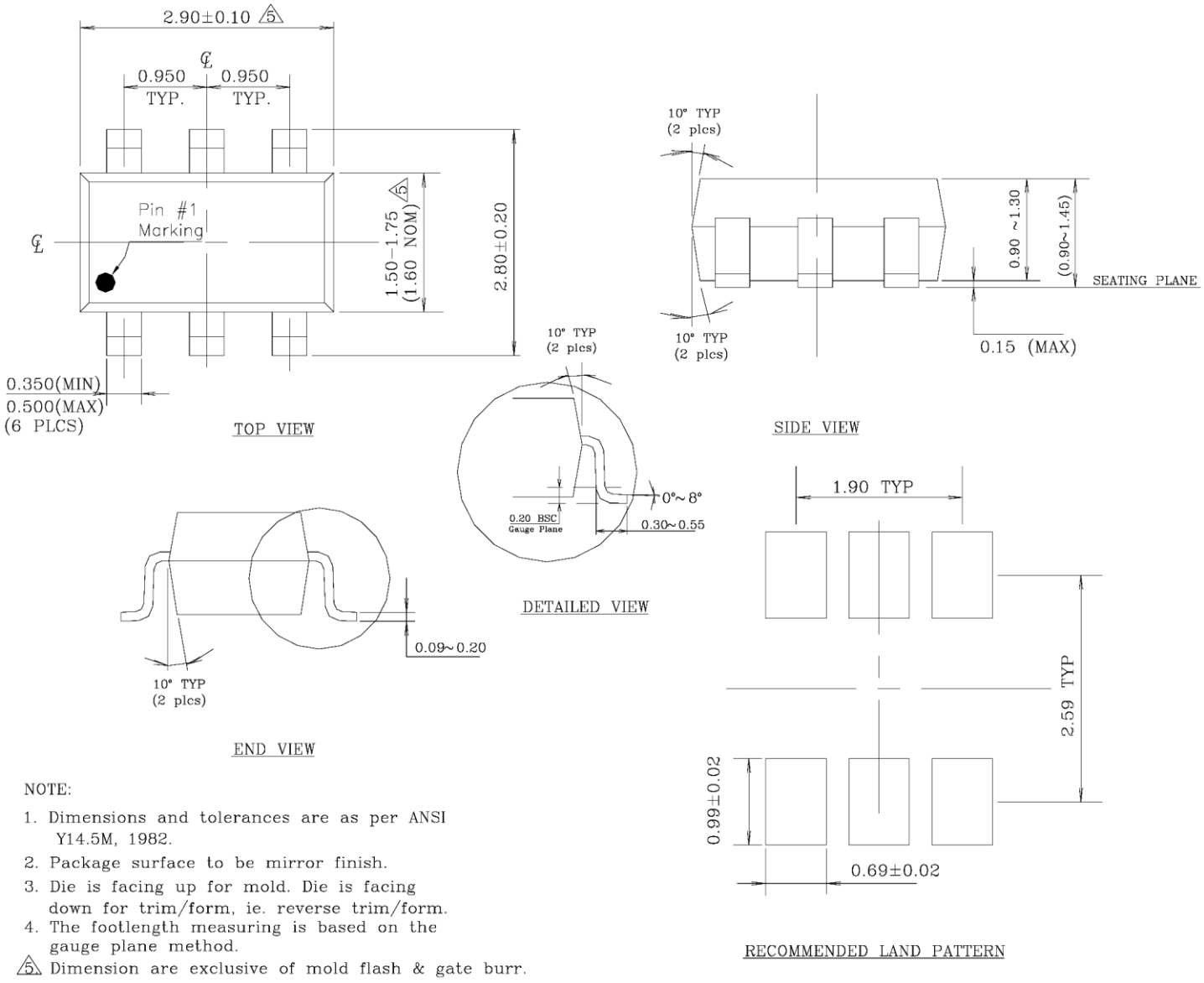
Package Information[4]



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

5 Dimension are exclusive of mold flash & gate burr.

6-Pin SOT23

Note:

4. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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