Features

- **Advanced Processor for Dual-mode Digital Still Cameras and Video Recorders**
- **Supports Personal Video Recording Applications**
- **ARM946E-S™ Core with Enhanced DSP Capability for A/V Processing and System Control Functions, 8 Kbytes Each for Instruction/Data Cache, Runs Up to 96 MHz**
- **Supports Progressive and Interlaced CCD Imagers (Up to 4 Fields)**
- **Image Processing Functions for CCD/CMOS Imagers**
- **Image Scaling and Rotation Hardware**
- **Video Encoder with Two DACs and Line Drivers for Composite or S-Video NTSC/PAL TV**
- **Digital Video Outputs Include: Composite, 16/8-bit YC (CCIR-656), RGB 565, 24-bit RGB, Component (Y/Pr/Pb), VESA Up to XGA Resolutions**
- **Direct Interface to Casio, Epson, AU, and Toppoly LCDs**
- **Encodes/Decodes Images and Video: Baseline JPEG, MPEG-1 at 24 fps VGA, MPEG-4 at 30 fps VGA (Performance Figures are for Half-duplex)**
- **DDR SDRAM Interface Supports from 128 Mbits to 1 Gbit**
- **Unified Memory Architecture (All Program and Data Stored in the DDR SDRAM)**
- **Support for All Flash Card Interfaces (MMC/SD, Memory Stick Pro™, SSFDC/Smartmedia, CompactFlash®)**
- **ATA/IDE Interface**
- **Static Memory Interface (Flash/SRAM) Supports Up to Eight 16 MB Devices**
- **One DAC for Camera Control Functions and Audio Output**
- **Four ADC Channels for Monitoring Camera Analog Inputs, Audio Input, Switch Input**
- **Audio Data Interface for Connection to External Stereo ADC/DAC**
- **USB 2.0 High-speed Slave and Full-speed Host Controllers for PC Camera and Printing Applications**
- **IEEE# 1394 Link Layer Interface**
- **Two USART Interfaces and a Serial Peripheral Interface (SPI) for Loading Boot Code and Controlling Camera Components**
- **Six General-purpose Timers for Waveform Generation (PWM, etc.) and Event Monitoring**
- **Programmable Watchdog Timer and Real-time Clock**
- **Keyboard Interface Supports Up to 25 Buttons**
- **Up to 8 External Interrupts and Up to 130 Pins Configurable as General-purpose I/O**
- **280-ball BGA Package, 1.8V Core, and 1.8 to 3.3V I/O Operation**
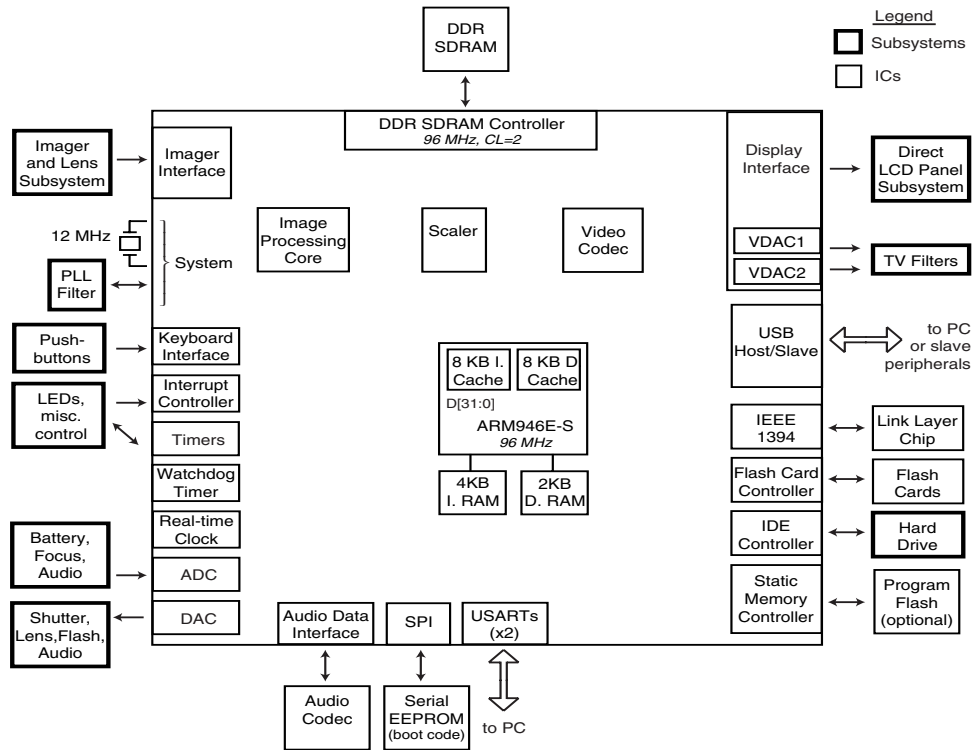
High-Performance Digital/Video Camera Processor

AT76C114 Summary

5674BS–IMAGE–09/04

Figure 1. Typical DSC Application Using the AT76C114

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Description

The AT76C114 is a highly integrated solution for dual-mode digital still-image and video cameras. It combines a number of functions that are required in such devices, including the following:

- The device is based on an ARM946E-S microprocessor whose function is to control the entire system, to capture and play back audio, and to multiplex compressed video and audio into a single bitstream that can be delivered to the main CPU. Most computationally-intensive functions are implemented in hardware which can be programmed according to user specifications, thus allowing the ARM® processor to be free for other user-defined functions such as advanced image and multimedia processing. The processor has 8 KB + 8 KB of internal instruction/data cache which helps it to operate efficiently and use minimal DDR SDRAM bandwidth.

- The device supports imager sizes of up to 16 megapixels. It accepts both Bayer RGB and CCIR-656 interfaces, which cover all possible CCD and CMOS sensors. It supports progressive as well as interlaced (up to 4 fields) imagers, including the special readout modes of progressive VGA CCD imagers. The device also supports a programmable delay on the external imager clock so that the highest quality images can be captured.

- The device has a high-performance still-image and video image processing block that performs all the necessary functions to convert the image/video data to a format that can be compressed in either JPEG or MPEG formats, as well as deliver image data to the LCD controller for live view. This block performs gain control, color recovery, Gamma correction, image enhancement, image correction, scaling, and conversion to YC format. All those functions have been implemented in hardware to achieve the required performance at very low power consumption figures. In addition, there is a hardware block that collects statistics on the imager for auto-exposure (AE) and auto-white balancing (AWB) algorithms. Those AE/AWB algorithms are performed in the embedded ARM9 CPU to allow customization of the application. The current architecture also has the appropriate interfaces as well as sufficient performance to support a strobe-type flash light, as well as dark frame subtraction for low-level light conditions.

- The device has numerous display capabilities. It has an integrated video encoder (double sampling) and two 10-bit video DACs running at up to 27 MHz to support direct display to high-definition TVs and projectors. The device also has a 24-bit RGB output to interface to flat-panel TVs (LCDs and Plasma) at different VESA rates up to XGA (1024 x 768) resolution. It supports both square pixel and CCIR-type formats and can display in NTSC or PAL modes with the same crystal. It also has an integrated LCD controller which can interface directly to various LCDs. It directly supports a variety of LCD panels from Epson, Casio, AU, and Toppoly without the need for external ICs. Finally, it has a digital video output interface which can supply composite, 8-bit YC (CCIR-656), 16-bit YC, RGB 565, or component (Y/Pr/Pb) formats.

- The device has a high-performance image scaler that can do up and down scaling at floating point resolutions. In addition, the device supports hardware rotation, as well as flipping and mirroring in both vertical and horizontal dimensions. It takes approximately 120 ms to rotate a 2M image (1600 pixels) in any direction.

- For video applications, a hardware video codec is included that supports MPEG-4 Simple Profile (encode and decode) and Advanced Simple Profile (encode only) communication at up to 30 fps VGA resolution. The hardware video engine is a pipelined architecture which is also flexible enough to support JPEG compression/decompression, H.263, MPEG-2 encode(I/P frames) at 30 fps VGA, and MPEG-1 encode/decode at 24 fps VGA (I frames only). The video codec can also be used to record and play back video clips including those taken from other

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digital cameras and mobile phones. All performance figures are for half-duplex operation. Full duplex is possible, but the performance has not been characterized.

- The device utilizes a unified memory architecture using the DDR-SDRAM to capture, process, and play back images and video as well as to store program code and variables. It supports SDRAM configurations of up to 1 gigabit.

- The device supports all Flash cards, including Multimedia Card (MMC), Secure Digital (SD), Memory Stick Pro, SSFDC/Smartmedia/NAND Flash, and CompactFlash. The Flash card interfaces can support read/write operations at the maximum speeds specified by the Flash cards.

- The device has an ATA/IDE controller with UDMA capability to stream video directly to hard drives or CompactFlash devices.

- A static memory controller is included that supports up to eight 16 MB devices such as Flash, SRAM, or other memory-mapped peripherals. Both 8-bit and16-bit data buses are supported, with data accesses of up to 32 bits. The number of wait states, and setup, hold, and data float times are programmable on a per device (chip select) basis.

- A general-purpose 10-bit, 96 kHz DAC is available. It can be used to control camera components such as the iris, shutter motor, lens motor, flash bulb, or AGC gain. It can also be used to drive audio output.

- A general-purpose 10-bit, 96 kHz ADC is available. This ADC has four input channels, which can be used for such things as battery level checking, photo detection, focus sensing, or audio capture.

- The I^2S- and AC '97-compatible audio data interface allows the device to connect with an external stereo ADC/DAC to capture or play back voice or audio. The device can encode captured audio in various popular formats, and can package it in the same bitstream as the video or inside compressed JPEG pictures. It can also play back stand-alone audio such as MP3 files, or audio embedded in MPEG bitstreams.

- The USB 2.0 high-speed slave controller can be used to connect to a PC for efficient downloading of captured images to the PC. The USB 2.0 full-speed host controller allows the device to connect directly to printers and other slave devices.

- An IEEE 1394 link layer interface allows the device to stream video (compressed or uncompressed) to other devices.

- Two USART interfaces are included for serial communication. They support standard baud rates of up to 460.8 kbps or non-standard rates of up to 4.875 Mbps in asynchronous mode. They support rates of up to19.5 Mbps in synchronous mode.

- The Serial Peripheral Interface (SPI) is used to boot from an external EEPROM. Once the boot code is loaded inside the program memory, the CPU can download its code from any peripheral supported by the device, including non-volatile storage media. With four chip select pins, the SPI can also be used to control other external devices at speeds of up to 24 Mbps.

- Three 16-bit and three 32-bit general purpose timers are included which can be used to generate interrupts to the internal CPU. The 16-bit timers can also generate waveforms on their associated pins via pulse-width modulation (PWM) or other techniques. They can also monitor and count external events on these pins.

- A dedicated watchdog timer is available which can provide an interrupt, an event on an external pin, or a reset to the internal CPU in the event that software is not responding as expected. Write access to the watchdog is protected by control access keys to prevent corruption of the watchdog should an error condition occur.

- A real-time clock is provided to keep track of the time. It operates on its own power supply, so the clock can keep running with very low power consumption even if the rest of the chip is unpowered. Two pins are provided to control system power switching.

- The device provides a keyboard interface that can monitor up to 25 buttons.

- The device provides up to 8 external interrupt pins, depending on the system configuration, which can be handled by the interrupt controller as either edge or level sensitive.

- Up to 130 pins can also be configured as GPIOs, depending on the system application.

- During normal operation, the power consumption may be minimized by disabling the clock of any internal module that is not in use. In order to further reduce power consumption, the main CPU clock can be divided to run at a slower speed. In order to minimize power consumption when the device is not in use, a "sleep mode" is available that halts the operation of all logic and shuts down the oscillators and PLLs. Recovery from sleep mode occurs via the WKP ("wakeup") pin, at which time the device begins execution from its previous state.

Technology

- The device is fabricated in a 0.18 micron process. It is expected that the device will operate at less than 70 mA when fully active (video compression/decompression).

- The core logic requires a 1.8V power supply. Most I/O pads require 3.3V supplies, a few interfaces use 1.8V supplies, and the DDR interface requires a 2.5V supply.

- The package is a 280-ball BGA.

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