32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

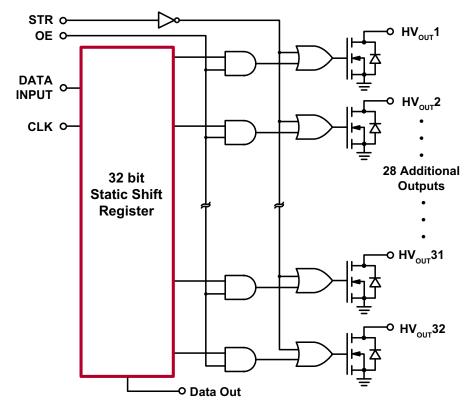
- Processed with HVCMOS[®] technology
- Output voltages to 225V using a ramped supply voltage
- SINK current minimum 100mA
- Shift register speed 8.0MHz
- Strobe and enable inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Hi-Rel processing available

General Description

The HV5122 is a low voltage serial to high voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register and control logic to perform the Output Enable and all-on functions. Data is shifted through the shift register on the high to low transition of the clock. The HV5122 shifts in the counter-clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE(Output Enable) or the STR(Strobe) inputs.

The HV5122 has been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.



Functional Block Diagram

Ordering Information

Part Number	Package	Packing
HV5122DJ-G*	44-Lead Quad Cerpac	27/Tube
HV5122PG-G	44-Lead PQFP	96/Tray
HV5122PG-G M919	44-Lead PQFP	500/Reel
HV5122PJ-G	44-Lead PLCC	27/Tube
HV5122PJ-G M903	44-Lead PLCC	500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package * Hi-Rel processing available

Hi-Rel processing available

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V _{DD}	-0.5V to +15V
Supply voltage, V _{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current ¹	1.5A
Continuous total power dissipation ² Plastic Ceramic	1200W 1500W
Operating temperature range Plastic Ceramic	-40°C to +85°C -55°C to +125°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

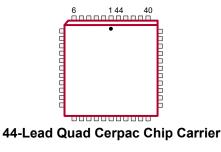
- 1. Duty cycle is limited by the total power dissipated in the package.
- 2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

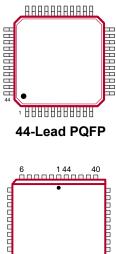
Product Marking



44-Lead Quad Cerpac Chip Carrier

Pin Configuration





44-Lead PLCC

Typical Thermal Resistance

Package	$oldsymbol{ heta}_{ja}$
44-Lead Quad Cerpac	
44-Lead PQFP	51°C/W
44-Lead PLCC	37°C/W



Packages may or may not include the following marks: Si or G

Doc.# DSFP-HV5122 B072213

Recommended Operating Conditions

Sym	Parameter		Min	Тур	Max	Units
V _{DD}	Logic voltage supply		10.8	12	13.2	V
HV _{out}	High voltage output		-0.3	-	225	V
V _{IH}	High-level input voltage		V _{DD} -2.0	-	V _{DD}	V
V _{IL}	Low-level input voltage		0	-	2.0	V
f _{ськ}	Clock frequency	Clock frequency			8.0	MHz
–	Operating free air temperature	Plastic	-40	-	+85	00
T _A	Operating free-air temperature	Ceramic	-55	-	+125	°C

Power-Up Sequence

Power-up sequence should be the following:

- 1. Connect ground
- 2. Apply V_{DD} 3. Set all inputs to a known state

Power-down sequence should be the reverse of the above.

Electrical Characteristics (Over recommended operating conditions unless otherwise specified) **DC Characteristics**

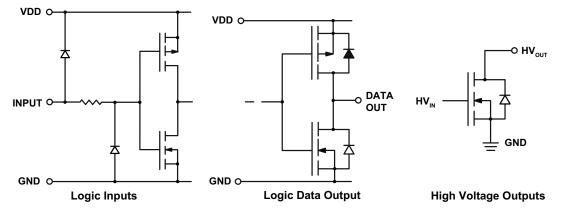
Sym	Parameter	Min	Max	Units	Conditions	
I _{DD}	V _{DD} supply current	V _{DD} supply current			mA	f _{CLK} = 8.0MHz, F _{DATA} = 4.0MHz
I _{DDQ}	Quiescent V _{DD} supply curr	-	100	μA	All $V_{IN} = 0V$	
I _{O(OFF)}	Off-state output current	-	10	μA	All outputs high, all SWS parallel	
I _{IH}	High level logic input curre	-	1.0	μA	V _{IH} = 12V	
I _{IL}	Low level logic input curre	Low level logic input current			μA	V _{IL} = 0
V _{OH}	High level output data out	High level output data out			V	Ι _{DOUT} = -100μΑ
V	нV _{оит}		-	15	V	I _{HVOUT} = +100mA
V _{OL}	Low level output voltage	Data out	-	1.0		Ι _{DOUT} = +100μΑ
V _{oc}	HV _{out} clamp voltage		-	-1.5	V	I _{oL} = -100mA

AC Characteristics ($V_{DD} = 12V$, $T_{A} = 25^{\circ}C$)

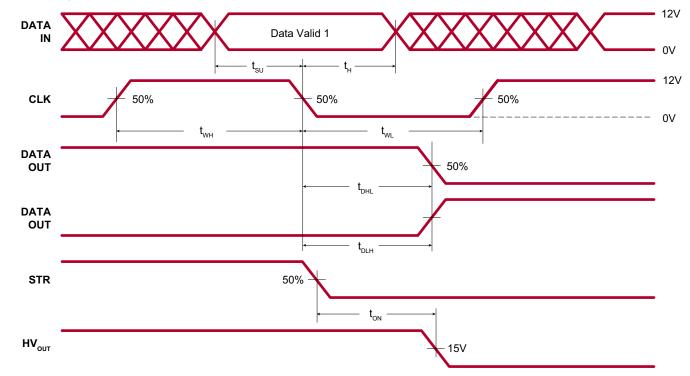
Sym	Parameter	Min	Мах	Units	Conditions
f _{clk}	Clock frequency	-	8.0	MHz	
t _w	Clock width, high or low	62	-	ns	
t _{su}	Data setup time before CLK falls	25	-	ns	
t _H	Data hold time after CLK falls	10	-	ns	
t _{on}	Turn-on time, HV_{OUT} from strobe	-	500	ns	$R_{L} = 2.0 K\Omega$ to 200V
t _{DHL}	Data output delay after H to L CLK	-	100	ns	C _L = 15pF
t _{DLH}	Data output delay after L to H CLK	-	100	ns	C _L = 15pF

HV5122

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

		Inp	uts		Outputs					
	Data	.			Shift	Reg	HV Ou	Data		
			OE STR		1	232	1	232	Out	
All on	Х	Х	Х	L	•	••	ON	ONON	•	
All off	Х	Х	L	Н	•	●●	OFF	OFFOFF	•	
Load S/R	H OR L	\downarrow	L	н	H or L	●●	OFF	OFFOFF	-	
Output Enable	Х	H OR L	Н	Н	H or L	••	ON or OFF	●●	•	

Notes:

 $H = high \ level, \ L = low \ level, \ X = irrelevant, \ \downarrow = high-to-low \ transition$

• = dependent on previous stage's state before the last CLK: High-to-low transition

Doc.# DSFP-HV5122 B072213

HV5122

44-Lead PQFP Pin description

PinFunctionDescription1 HV_{our11} 2 HV_{our11} 3 HV_{aur13} 4 HV_{our14} 5 HV_{our15} 6 HV_{our17} 8 HV_{our17} 9 HV_{our17} 10 HV_{our17} 11 HV_{our17} 12 HV_{our22} 13 HV_{our24} 15 HV_{our25} 16 HV_{our27} 17 HV_{our28} 20 HV_{our30} 21 HV_{our31} 22 HV_{our33} 23DATA OUT242525N/C26 NC 27Output enable input.28 OE 29 CLK Data full register clock. Input are forced into a LOW state, regardless of data in each channel. When OE is HUGH, all HV outputs reflect data latched.29 CLK Data high register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.32STRStrobe.												
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Pin	Function	Description									
3 HV _{cur} 13 4 HV _{cur} 14 5 HV _{cur} 14 5 HV _{cur} 17 6 HV _{cur} 17 8 HV _{cur} 19 10 HV _{cur} 21 11 HV _{cur} 22 13 HV _{cur} 23 14 HV _{cur} 26 15 HV _{cur} 27 18 HV _{cur} 28 19 HV _{cur} 28 19 HV _{cur} 32 22 HV _{cur} 31 22 HV _{cur} 32 23 DATA OUT 24 25 26 N/C 27 No connect. 28 OE Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. 29 CLK Data shift register clock. Input are shifted into the shift register on the positive edge of the clock. 30 GND Logic and high voltage ground. 31 VDD Low voltage logic power rail.		HV _{out} 11										
4 HV _{our} 14 5 HV _{our} 15 6 HV _{our} 17 8 HV _{our} 19 10 HV _{our} 20 11 HV _{our} 21 12 HV _{our} 22 13 HV _{our} 23 14 HV _{our} 24 15 HV _{our} 26 17 HV _{our} 28 18 HV _{our} 29 20 HV _{our} 30 21 HV _{our} 32 23 DATA OUT 24 N/C 25 N/C 26 N/C 27 Output enable input. 28 OE 29 CLK 29 CLK 30 GND 31 VDD 131 VDD		HV _{out} 12										
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$ \begin{array}{ c c c c } \hline 6 & HV_{our} 16 \\ \hline 7 & HV_{our} 17 \\ \hline 8 & HV_{our} 18 \\ \hline 9 & HV_{our} 19 \\ \hline 10 & HV_{our} 20 \\ \hline 11 & HV_{our} 21 \\ \hline 12 & HV_{our} 22 \\ \hline 13 & HV_{our} 23 \\ \hline 14 & HV_{our} 24 \\ \hline 15 & HV_{our} 25 \\ \hline 16 & HV_{our} 26 \\ \hline 17 & HV_{our} 28 \\ \hline 19 & HV_{our} 28 \\ \hline 19 & HV_{our} 28 \\ \hline 20 & HV_{our} 30 \\ \hline 21 & HV_{our} 30 \\ \hline 22 & HV_{our} 32 \\ \hline 23 & DATA OUT \\ \hline 24 & Data output for cascading to the data input of the next device. \\ \hline 24 & \\ \hline 25 & \\ \hline 26 & \\ \hline 7 & \\ \hline 28 & OE \\ \hline OE & \\ \hline OE & \\ \hline Output enable input. \\ \hline When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. \\ \hline 29 & CLK \\ \hline 30 & GND \\ \hline Logic and high voltage ground. \\ \hline WDD & Low voltage logic power rail. \\ \hline \end{array}$	4	HV _{out} 14										
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$\begin{array}{ c c c }\hline 9 & HV_{our}19 \\ \hline 10 & HV_{our}20 \\ \hline 11 & HV_{our}21 \\ \hline 12 & HV_{our}22 \\ \hline 13 & HV_{our}23 \\ \hline 14 & HV_{our}23 \\ \hline 14 & HV_{our}24 \\ \hline 15 & HV_{our}26 \\ \hline 17 & HV_{our}26 \\ \hline 17 & HV_{our}28 \\ \hline 19 & HV_{our}28 \\ \hline 19 & HV_{our}30 \\ \hline 21 & HV_{our}31 \\ \hline 22 & HV_{our}32 \\ \hline 23 & DATA OUT \\ \hline 24 & \\ \hline 25 & \\ \hline 26 & \\ \hline 27 & \\ \hline \\ 28 & OE & \\ \hline OE & \\ \hline Output enable input. \\ \hline When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. \\ \hline 29 & CLK & \\ \hline 30 & GND & Logic and high voltage ground. \\ \hline 10 & Low voltage logic power rail. \\ \hline \end{array}$	7	HV _{out} 17										
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$ \begin{array}{ c c c c } \hline 11 & HV_{our}^{OU}21 \\ \hline 12 & HV_{our}^{OU}22 \\ \hline 13 & HV_{our}^{OU}23 \\ \hline 14 & HV_{our}^{OU}24 \\ \hline 15 & HV_{our}^{OU}25 \\ \hline 16 & HV_{our}^{OU}28 \\ \hline 17 & HV_{our}^{OU}28 \\ \hline 19 & HV_{our}^{OU}28 \\ \hline 20 & HV_{our}^{OU}30 \\ \hline 21 & HV_{our}^{OU}31 \\ \hline 22 & HV_{our}^{OU}32 \\ \hline 23 & DATA OUT \\ \hline 24 & & & \\ \hline 25 & & & \\ \hline 26 & & & \\ \hline 27 & & & \\ \hline 28 & OE & & \\ \hline 0E & & & \\ \hline 29 & CLK & & \\ \hline 29 & CLK & \\ \hline 30 & GND & Logic and high voltage ground. \\ \hline 31 & VDD & Low voltage logic power rail. \\ \hline \end{array} \right. $	9	HV _{out} 19										
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19HV _{our} 2920HV _{our} 3021HV _{our} 3122HV _{our} 3223DATA OUT24	17	HV _{out} 27										
20 HV _{out} 30 21 HV _{out} 31 22 HV _{out} 32 23 DATA OUT Data output for cascading to the data input of the next device. 24	18	HV _{out} 28										
21 HV _{our} 31 22 HV _{our} 32 23 DATA OUT Data output for cascading to the data input of the next device. 24	19	HV _{out} 29										
22 HV _{our} 32 23 DATA OUT Data output for cascading to the data input of the next device. 24	20	HV _{out} 30										
23 DATA OUT Data output for cascading to the data input of the next device. 24	21	HV _{out} 31										
24 25 N/C No connect. 26 27 Output enable input. 28 OE Output enable input. 29 CLK Data shift register clock. Input are shifted into the shift register on the positive edge of the clock. 30 GND Logic and high voltage ground. 31 VDD Low voltage logic power rail.	22	HV _{out} 32										
25 26N/CNo connect.2727Output enable input.28OEOutput enable input.28OEWhen OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.29CLKData shift register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.	23		Data output for cascading to the data input of the next device.									
26N/CNo connect.2727Output enable input.28OEOutput enable input.28OEWhen OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.29CLKData shift register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.	24											
262728OE0Output enable input.28OEUpper or the positive of the clock.29CLK29CLK30GND21Logic and high voltage ground.31VDDLow voltage logic power rail.	25											
28OEOutput enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.29CLKData shift register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.	26	N/C	NO CONNECT.									
28OEWhen OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.29CLKData shift register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.	27											
When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.29CLKData shift register clock. Input are shifted into the shift register on the positive edge of the clock.30GNDLogic and high voltage ground.31VDDLow voltage logic power rail.			Output enable input.									
29 CLK the clock. 30 GND Logic and high voltage ground. 31 VDD Low voltage logic power rail.	28	OE										
31 VDD Low voltage logic power rail.	29	CLK										
	30	GND	Logic and high voltage ground.									
32 STR Strobe.	31	VDD	Low voltage logic power rail.									
	32	STR	Strobe.									

Pin	Function	Description						
33	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.						
34	N/C	No connect.						
35	HV _{out} 1							
36	HV _{OUT} 2							
37	HV _{OUT} 3							
38	HV _{OUT} 4							
39	HV _{OUT} 5							
40	HV _{OUT} 6	High voltage outputs.						
41	HV _{out} 7							
42	HV _{OUT} 8							
43	HV _{out} 9							
44	HV _{out} 10							

44-Lead PQFP Pin description (cont.)

44-Lead PLCC Pin description

Pin	Function	Function
1	HV _{out} 16	
2	HV _{out} 17	
3	HV _{out} 18	
4	HV _{out} 19	
5	HV _{OUT} 20	
6	HV _{OUT} 21	
7	HV _{OUT} 22	
8	HV _{OUT} 23	
9	HV _{OUT} 24	High voltage outputs
10	HV _{OUT} 25	
11	HV _{OUT} 26	
12	HV _{OUT} 27	
13	HV _{OUT} 28	
14	HV _{OUT} 29	
15	HV _{OUT} 30	
16	HV _{OUT} 31	
17	HV _{OUT} 32	

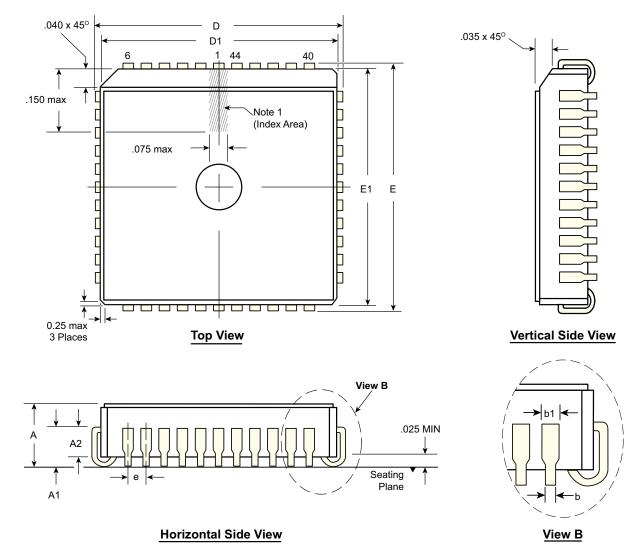
HV5122

44-Lead PLCC Pin description (cont.)

Pin	Function	Function						
18	DATA OUT	Data output for cascading to the data input of the next device.						
19								
20								
21	N/C	No connect.						
22								
23	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.						
24	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.						
25	GND	Logic and high voltage ground.						
26	VDD	Low voltage logic power rail.						
27	STR	Strobe.						
28	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.						
29	N/C	No connect.						
30	HV _{out} 1							
31	HV _{out} 2							
32	HV _{OUT} 3							
33	HV _{out} 4							
34	HV _{out} 5							
35	HV _{out} 6							
36	HV _{out} 7							
37	HV _{out} 8	High voltage outputs.						
38	HV _{out} 9							
39	HV _{out} 10							
40	HV _{OUT} 11							
41	HV _{out} 12							
42	HV _{out} 13							
43	HV _{out} 14							
44	HV _{out} 15							

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44-Lead Quad Cerpac Package Outline (DJ) .650x.650in body, .190in height (max), .050in pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symb	ol	Α	A1	A2	b	b1	D	D1	E	E1	е
Dimension	MIN	.155	.090	000	.017	.026	.685	.630	.685	.630	050
Dimension (inches)	NOM	.172	.100	.060 REF	.019	.029	.690	.650	.690	.650	.050 BSC
(incres)	MAX	.190	.120		.021	.032	.695	.665	.695	.665	DOO

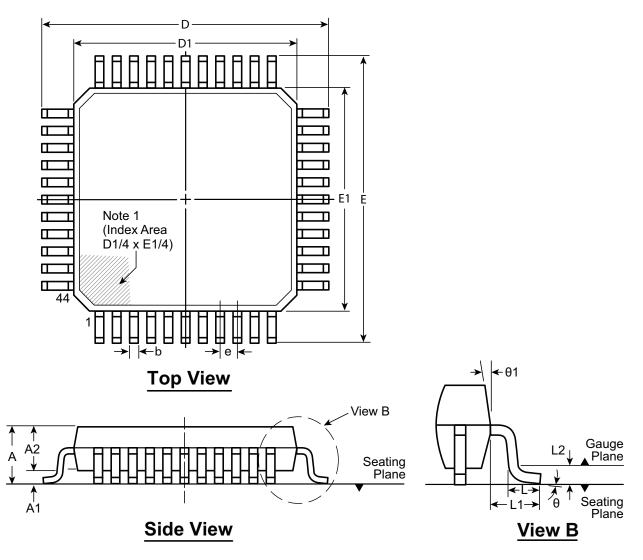
JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.

Drawings not to scale.

Supertex Doc. #: DSPD-44CERPACDJ, Version D090808.

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44-Lead PQFP Package Outline (PG) 10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		Α	A1	A2	b	D	D1	E	E1	е	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0 0
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5 ⁰
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7 °

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep. 1995.

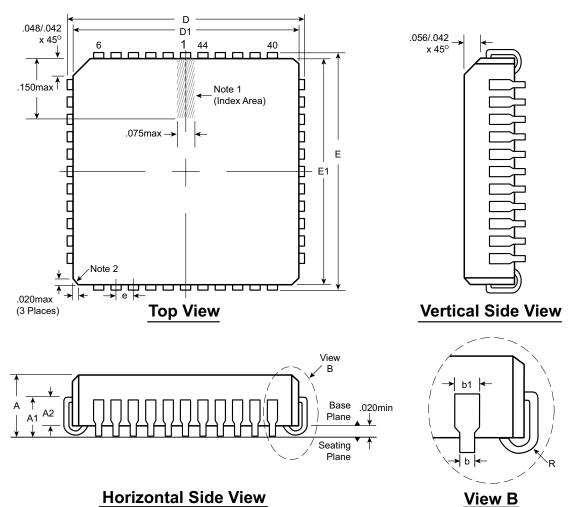
* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PQFPPG, Version C041309.

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44-Lead PLCC Package Outline (PJ) .653x.653in body, .180in height (max), .050in pitch



Notes:

2. Actual shape of this feature may vary.

Symbol		Α	A1	A2	b	b1	D	D1	E	E1	е	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to: <u>http://www.supertex.com/packaging.html</u>.)

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^{1.} A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.