Atmel ATA6829

Dual Triple DMOS Output Driver with Serial Input Control

DATASHEET

Features

- Supply voltage up to 40V
- R_{DSon} typically 0.5Ω at 25°C, maximum 1.1Ω at 150°C
- Up to 1.5A output current
- Three high-side and three low-side drivers usable as single outputs or half bridges
- Capable to switch all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors
- PWM capability for each output controlled by external PWM signal
- No shoot-through current
- Very low quiescent current I_S < 5µA in Standby Mode over total temperature range
- Outputs short-circuit protected
- Selective overtemperature protection for each switch and overtemperature prewarning
- Undervoltage protection
- Various diagnostic functions such as shorted output, open load, overtemperature and power-supply fail detection
- Serial data interface, Daisy Chain capable, up to 2MHz clock frequency
- SO16 power package

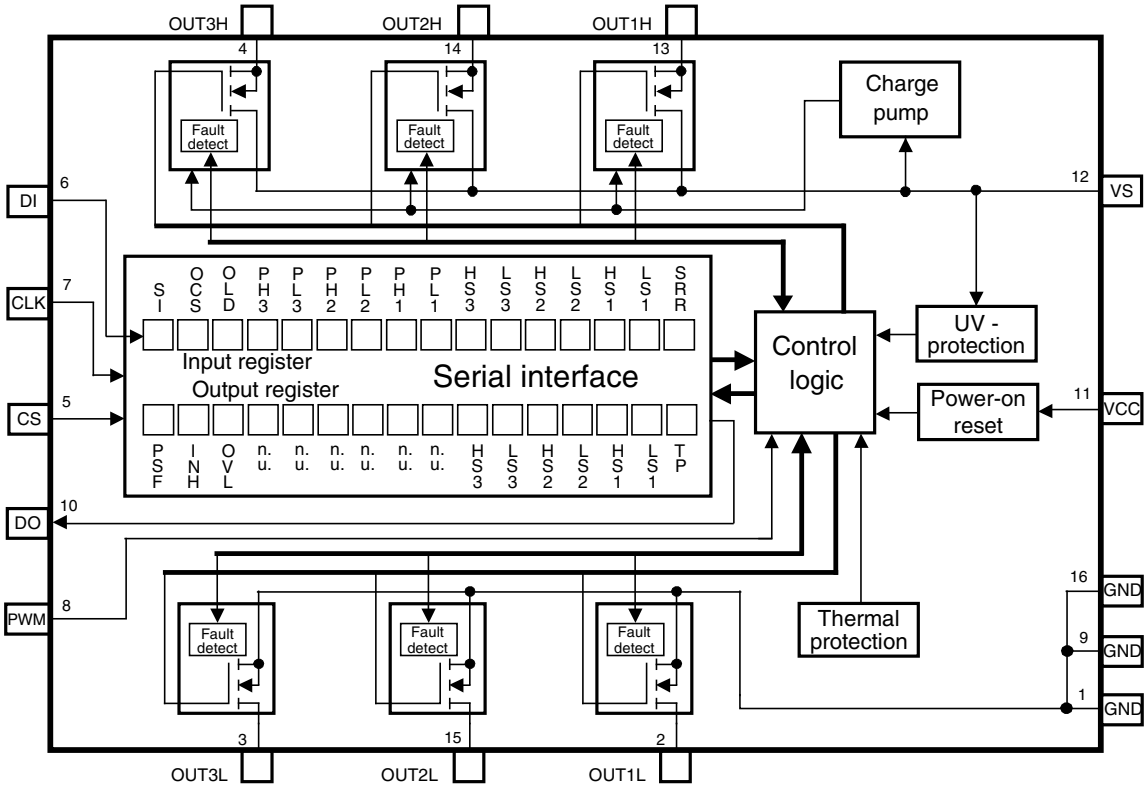
1. Description

The Atmel® ATA6829 is a fully protected driver interface designed in 0.8-µm BCDMOS technology. It is used to control up to six different loads by a microcontroller in automotive and industrial applications.

Each of the three high-side and three low-side drivers is capable to drive currents up to 1.5A. Each driver is freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the applications of H-bridges to drive DC motors. The capability to control each output with an external PWM signal opens additional applications.

Protection is guaranteed regarding short-circuit conditions, overtemperature and undervoltage. Various diagnostic functions and a very low quiescent current in stand-by mode opens a wide range of applications. Automotive qualification (protection against conducted interferences, EMC protection and 2-kV ESD protection) gives added value and enhanced quality for exacting requirements of automotive applications.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning PSO16

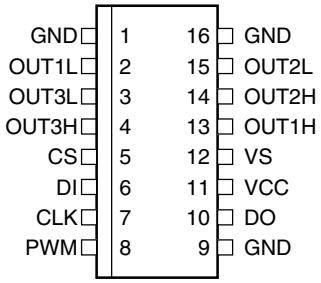


Table 2-1. Pin Description

Pin	Symbol	Function
1	GND	Ground; reference potential; internal connection to pin 9 and pin 16; connection to heat slug
2	OUT1L	Low-side driver output 1; power MOS open drain with internal reverse diode; short-circuit protection; overtemperature protection; diagnosis for short and open load; PWM ability
3	OUT3L	Low-side driver output 3; see pin 2
4	OUT3H	High-side driver output 3; power MOS open source with internal reverse diode; short-circuit protection; overtemperature protection; diagnosis for short and open load; PWM ability
5	CS	Chip select input; 5-V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
6	DI	Serial data input; 5-V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
7	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2MHz)
8	PWM	PWM input; 5-V CMOS logic level input with internal pull down; receives PWM signal to control outputs which are selected for PWM mode by the serial data interface, high = outputs on, low = outputs off
9	GND	Ground; see pin 1
10	DO	Serial data output; 5-V CMOS logic-level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first); output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on one data-output line only.
11	VCC	Logic supply voltage (5V)
12	VS	Power supply for high-side output stages OUT1H, OUT2H, OUT3H, internal supply
13	OUT1H	High-side driver output 1; see pin 4
14	OUT2H	High-side driver output 2; see pin 4
15	OUT2L	Low-side driver output 2; see pin 2
16	GND	Ground; see pin 1

3. Functional Description

3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer

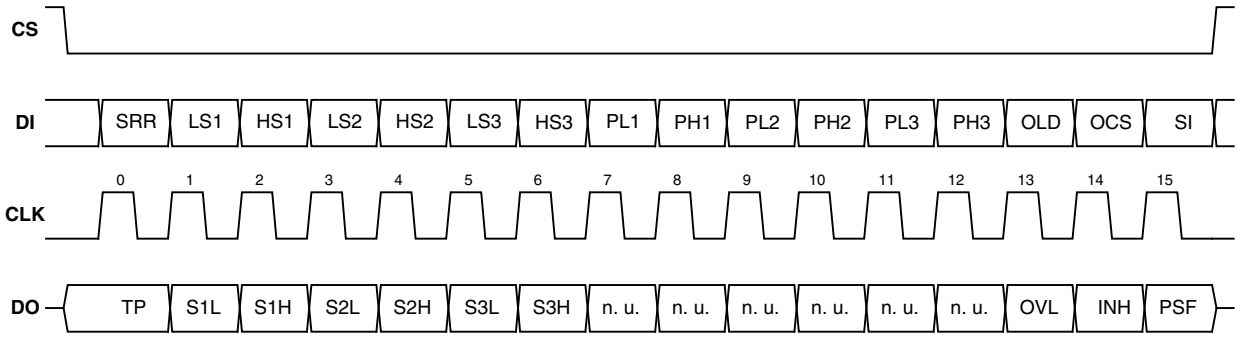


Table 3-1. Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF and OVL in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	PL1	Output LS1 additionally controlled by PWM Input
8	PH1	Output HS1 additionally controlled by PWM Input
9	PL2	See PL1
10	PH2	See PH1
11	PL3	See PL1
12	PH3	See PH1
13	OLD	Open load detection (low = on)
14	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered)

Table 3-2. Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OVL	Over-load detected: set high, when at least one output is switched off by a short-circuit condition or an overtemperature event. Bits 1 to 6 can be used to detect the affected switch. (open-load detection bit OLD = high)
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) High = standby, low = normal operation
15	PSF	Power-supply fail: undervoltage at pin VS detected

After power-on reset, the input register has the following status:

Bit 15 SI	Bit 14 OCS	Bit 13 OLD	Bit 12 PH3	Bit 11 PL3	Bit 10 PH2	Bit 9 PL2	Bit 8 PH1	Bit 7 PL1	Bit 6 HS3	Bit 5 LS3	Bit 4 HS2	Bit 3 LS2	Bit 2 HS1	Bit 1 LS1	Bit 0 SRR
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

The following patterns are used to enable internal test modes of the IC. It is not recommended to use these patterns during normal operation.

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	H	H	L	L	L	L	L	L	L

3.2 Power-supply Fail

In case of undervoltage at pin VS, the Power-Supply Fail bit (PSF) in the output register is set and all outputs are disabled. To detect an undervoltage, its duration has to last longer than the undervoltage detection delay time t_{dUV}. The outputs are enabled immediately when supply voltage recovers normal operation value. The PSF bit stays high until it is reset by the SRR bit in the input register.

3.3 Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{OUT1-3}). If the current through the external load does not reach the open-load detection current, the corresponding bit of the output in the output register is set to high.

Switching on an output stage with OLD bit set to low disables the open-load function for this output.

3.4 Overtemperature Protection

If the junction temperature of one ore more output stages exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word. The status of TP is available at pin DO with the falling edge of CS. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the status of input and output registers.

If the junction temperature of an output stage exceeds the thermal shutdown threshold, $T_{j\ switch\ off}$, the affected output is disabled and the corresponding bit in the output register is set to low. Additional the overload detection bit (OVL) in the output register is set. The output can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{jswitch\ on}$ and the SRR bit in the input register is set to high. Hysteresis of thermal prewarning and shutdown threshold avoids oscillations.

3.5 Short-circuit Protection

The output currents are limited by a current regulator. Overcurrent detection is activated by writing a high to the OCS bit in the input register. When the current in an output stage exceeds the overcurrent limitation and shut-down threshold, it is switched off after a delay time (t_{dSd}). The over-load detection bit (OVL) is set and the corresponding status bit in the output register is set to low. For OCS = low the overcurrent shutdown is inactive and the OVL bit is not set by an overcurrent. By writing a high to the SRR bit in the input register the OVL bit is reset and the disabled outputs are enabled.

3.6 Inhibit

The SI bit in the input register has to be set to zero to inhibit the Atmel ATA6829.

All output stages are then turned off but the serial interface stays active. The current consumption is reduced to less than 5 µA at pin VS and less than 100 µA at pin VCC. The output stages can be activated again by bit SI = 1.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

Parameters	Pin	Symbol	Value	Unit
Supply voltage	12	V_{VS}	–0.3 to +40	V
Supply voltage t < 0.5s; I_S > –2A	12	V_{VS}	–1	V
Logic supply voltage	11	V_{VCC}	–0.3 to +7	V
Logic input voltage	5 to 8	V_{CS}, V_{DI}, V_{CLK}, V_{PWM}	–0.3 to V_{VCC} + 0.3	V
Logic output voltage	10	V_{DO}	–0.3 to V_{VCC} + 0.3	V
Input current	5 to 8	I_{CS}, I_{DI}, I_{CLK}, I_{PWM}	–10 to +10	mA
Output current	10	I_{DO}	–10 to +10	mA
Output current	2 to 4 13 to 15	I_{Out3H}, I_{Out2H}, I_{Out1H} I_{Out3L}, I_{Out2L}, I_{Out1L}	Internally limited, see output specification	
Output voltage	2 to 4 13 to 15	I_{Out3H}, I_{Out2H}, I_{Out1H} I_{Out3L}, I_{Out2L}, I_{Out1L}	–0.3 to +40	V
Reverse conducting current (t_{pulse} = 150 µs)	2 to 4 13 to 15 towards pin 12	I_{Out3H}, I_{Out2H}, I_{Out1H} I_{Out3L}, I_{Out2L}, I_{Out1L}	17	A
Junction temperature range		T_J	–40 to +150	°C
Storage temperature range		T_{STG}	–55 to +150	°C

5. Thermal Resistance

Parameters	Test Conditions	Symbol	Value	Unit
Junction pin	Measured to heat slug GND pins 1, 9 and 16	R_{thJP}	5	K/W
Junction ambient		R_{thJA}	30	K/W

6. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_{VS}	V_{UV}[1] to 40	V
Logic supply voltage	V_{VCC}	4.75 to 5.25	V
Logic input voltage	V_{CS},V_{DI}, V_{CLK}, V_{PWM}	–0.3 to V_{VCC}	V
Serial interface clock frequency	f_{CLK}	2	MHz
PWM input frequency	f_{PWM}	1	kHz
Junction temperature range	T_j	–40 to +150	°C

Note: 1. Threshold for undervoltage detection.

7. Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Interference suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model)	ESD S 5.1	2 kV
ESD (Machine Model)	JEDEC A115A	200 V

Note: 1. Test pulse 5: V_{smax} = 40V.

8. Electrical Characteristics

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40° C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Current Consumption								
1.1	Quiescent current VS	V_{VS} < 20V, SI = low	12	I_{VS}		1	5	µA	A
1.2	Quiescent current VCC	4.75V < V_{VCC} < 5.25V, SI = low	11	I_{VCC}		60	100	µA	A
1.3	Supply current VS	V_{VS} < 20V normal operating, all outputs off, input register bit 13 (OLD) = high	12	I_{VS}		4	6	mA	A
1.4	Supply current VCC	4.75V < V_{VCC} < 5.25V, normal operating	11	I_{VCC}		350	650	µA	A
1.5	Discharge current VS	V_{VS} = 32.5V, INH = low	12	I_{VS}	0.5		5.5	mA	A
1.6	Discharge current VS	V_{VS} = 40V, INH = low	12	I_{VS}	2.5		10	mA	A
2	Undervoltage Detection, Power-on Reset								
2.1	Power-on reset threshold		11	V_{VCC}	3.2	3.9	4.4	V	A
2.2	Power-on reset delay time	After switching on V_{CC}		t_{dPor}	30	95	190	µs	A
2.3	Undervoltage-detection threshold	V_{CC} = 5V	12	V_{Uv}	5.6		7.0	V	A
2.4	Undervoltage-detection hysteresis	V_{CC} = 5V	12	ΔV_{Uv}		0.6		V	A
2.5	Undervoltage-detection delay time			t_{dUV}	10		40	µs	A
3	Thermal Prewarning and Shutdown								
3.1	Thermal prewarning set			$T_{jPW\ set}$	120	145	170	°C	B
3.2	Thermal prewarning reset			$T_{jPW\ reset}$	105	130	155	°C	B
3.3	Thermal prewarning hysteresis			ΔT_{jPW}		15		K	B
3.4	Thermal shutdown off			$T_{j\ switch\ off}$	150	175	200	°C	B

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1 ms.
2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40° C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Thermal shutdown on			$T_{j\ switch\ on}$	135	160	185	°C	B
3.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		15		K	B
3.7	Ratio thermal shutdown off/thermal prewarning set			$T_{j\ switch\ off}$/ $T_{jPW\ set}$	1.05	1.2			B
3.8	Ratio thermal shutdown on/thermal prewarning reset			$T_{j\ switch\ on}$/ $T_{jPW\ reset}$	1.05	1.2			B
4	Output Specification (OUT1-OUT3)								
4.1	On resistance	$I_{Out\ 1\text{-}3\ H}$ = –1.3A	4, 13, 14	$R_{DSOn1\text{-}3H}$			1.1	Ω	A
4.2		$I_{Out\ 1\text{-}3\ L}$ = 1.3A	2, 3, 15	$R_{DSOn1\text{-}3L}$			1.1	Ω	A
4.3	High-side output leakage current	$V_{Out\ 1\text{-}3\ H}$ = 0V, output stages off	4, 13, 14	$I_{Out1\text{-}3H}$	–5			µA	A
4.4	Low-side output leakage current	$V_{Out\ 1\text{-}3\ L}$ = V_{VS}, output stages off	2, 3, 15	$I_{Out1\text{-}3L}$			5	µA	A
4.5	High-side switch reverse diode forward voltage	I_{Out} = 1.5A	4, 13, 14	$V_{Out1\text{-}3}$ – V_{VS}			1.5	V	A
4.6	Low-side switch reverse diode forward voltage	$I_{Out\ 1\text{-}3\ L}$ = –1.5A	2, 3, 15	$V_{Out1\text{-}3L}$	–1.5			V	A
4.7	High-side overcurrent limitation and shutdown threshold		4, 13, 14	$I_{Out1\text{-}3H}$	–2.5	–2	–1.5	A	A
4.8	Low-side overcurrent limitation and shutdown threshold		2, 3, 15	$I_{Out1\text{-}3L}$	1.5	2	2.5	A	A
4.9	Overcurrent shutdown delay time			t_{dSd}	10		40	µs	A
4.10	High-side open load detection current	Input register bit 13 (OLD) = low, output off	4, 13, 14	$I_{Out1\text{-}3H}$	–2.5		–0.2	mA	A
4.11	Low-side open load detection current	Input register bit 13 (OLD) = low, output off	2, 3, 15	$I_{Out1\text{-}3L}$	0.2		2.5	mA	A
4.12	High-side output switch on delay(1),(2)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.13	Low-side output switch on delay(1),(2)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.14	High-side output switch off delay(1),(2)	V_{VS} =13V R_{Load} = 30Ω		t_{doff}			20	µs	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1 ms.
2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40° C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.15	Low-side output switch off delay(1),(2)	V_{VS} =13V R_{Load} = 30Ω		t_{doff}			3	µs	A
4.16	Dead time between corresponding high- and low-side switches	V_{VS} =13V R_{Load} = 30Ω		$t_{don} - t_{doff}$	1			µs	A
4.17	Δt_{dPWM} low-side switch(3)	V_{VS} = 13V R_{Load} = 30Ω		$\Delta t_{dPWM} = t_{don} - t_{doff}$			20	µs	A
4.18	Δt_{dPWM} high-side switch(3)	V_{VS} = 13V R_{Load} = 30Ω		$\Delta t_{dPWM} = t_{don} - t_{doff}$	3		7	µs	A
5	Logic Inputs DI, CLK, CS, PWM								
5.1	Input voltage low-level threshold		5-8	V_{IL}	0.3 × V_{VCC}			V	A
5.2	Input voltage high-level threshold		5-8	V_{IH}			0.7 × V_{VCC}	V	A
5.3	Hysteresis of input voltage		5-8	ΔV_I	50		700	mV	A
5.4	Pull-down current Pins DI, CLK, PWM	V_{DI}, V_{CLK}, V_{PWM} = V_{CC}	6, 7, 8	I_{PD}	10		65	µA	A
5.5	Pull-up current Pin CS	V_{CS} = 0V	5	I_{PU}	–65		–10	µA	A
6	Serial Interface – Logic Output DO								
6.1	Output-voltage low level	I_{DOL} = 2mA	10	V_{DOL}			0.4	V	A
6.2	Output-voltage high level	I_{DOL} = –2mA	10	V_{DOH}	V_{VCC} – 0.7 V			V	A
6.3	Leakage current (tri-state)	V_{CS} = V_{CC} 0V < V_{DO} < V_{VCC}	10	I_{DO}	–10		10	µA	A
7	Inhibit Input – Timing								
7.1	Delay time from standby to normal operation			t_{dINH}			100	µs	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1 ms.
2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

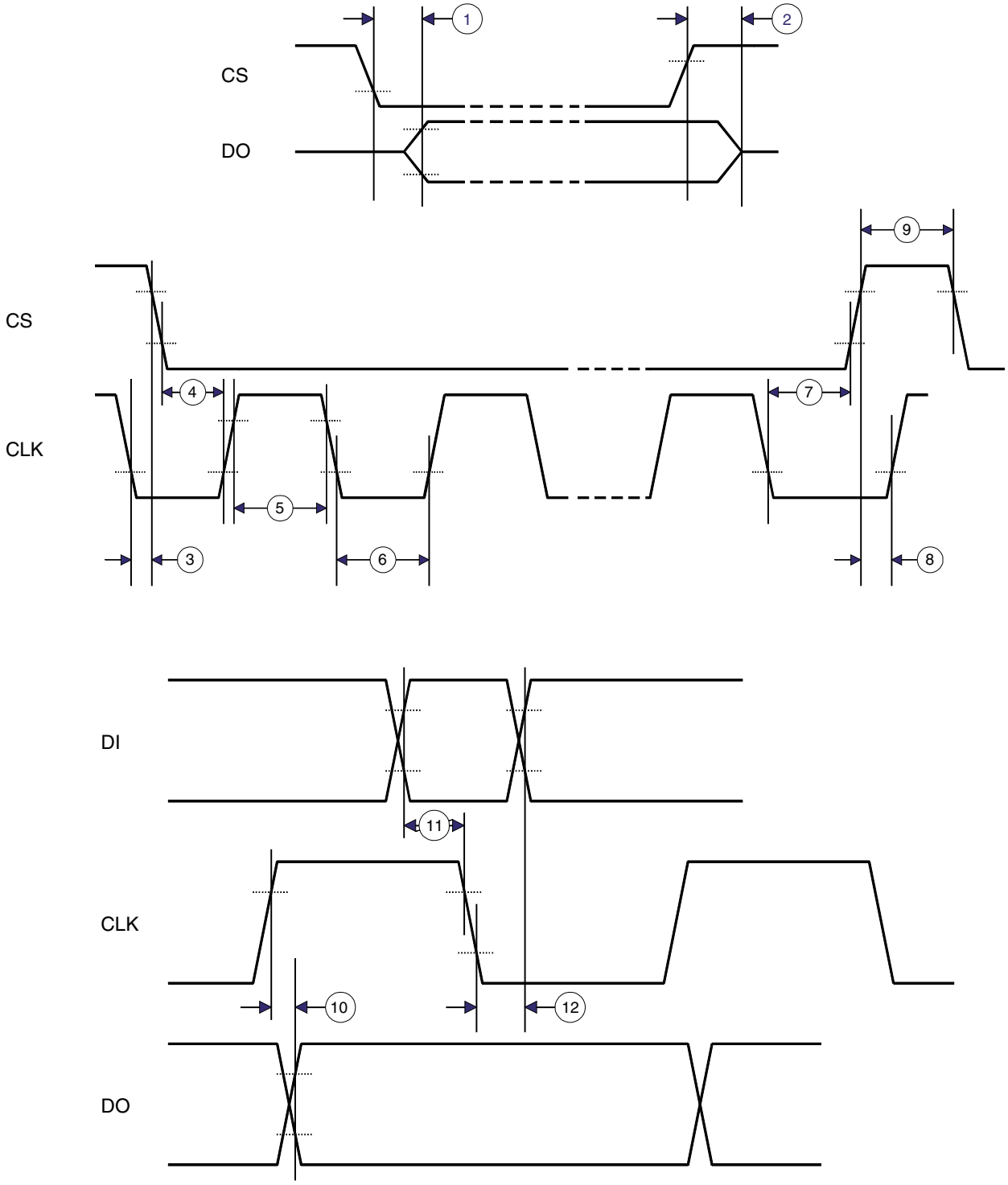
9. Serial Interface – Timing

No.	Parameters	Test Conditions	Pin	Timing Chart No.(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
8.1	DO enable after CS falling edge	C_{DO} = 100 pF	10	1	t_{ENDO}			200	ns	D
8.2	DO disable after CS rising edge	C_{DO} = 100 pF	10	2	t_{DISDO}			200	ns	D
8.3	DO fall time	C_{DO} = 100 pF	10	-	t_{DOf}			100	ns	D
8.4	DO rise time	C_{DO} = 100 pF	10	-	t_{DOr}			100	ns	D
8.5	DO valid time	C_{DO} = 100 pF	10	10	t_{DOVal}			200	ns	D
8.6	CS setup time		5	4	$t_{CSSethl}$	225			ns	D
8.7	CS setup time		5	8	$t_{CSSetlh}$	225			ns	D
8.8	CS high time		5	9	t_{CSh}	500			ns	D
8.9	CLK high time		7	5	t_{CLKh}	225			ns	D
8.10	CLK low time		7	6	t_{CLKl}	225			ns	D
8.11	CLK period time		7	-	t_{CLKp}	500			ns	D
8.12	CLK setup time		7	7	$t_{CLKSethl}$	225			ns	D
8.13	CLK setup time		7	3	$t_{CLKSetlh}$	225			ns	D
8.14	DI setup time		6	11	t_{DIset}	40			ns	D
8.15	DI hold time		6	12	t_{DIHold}	40			ns	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. See Figure 9-1 on page 12

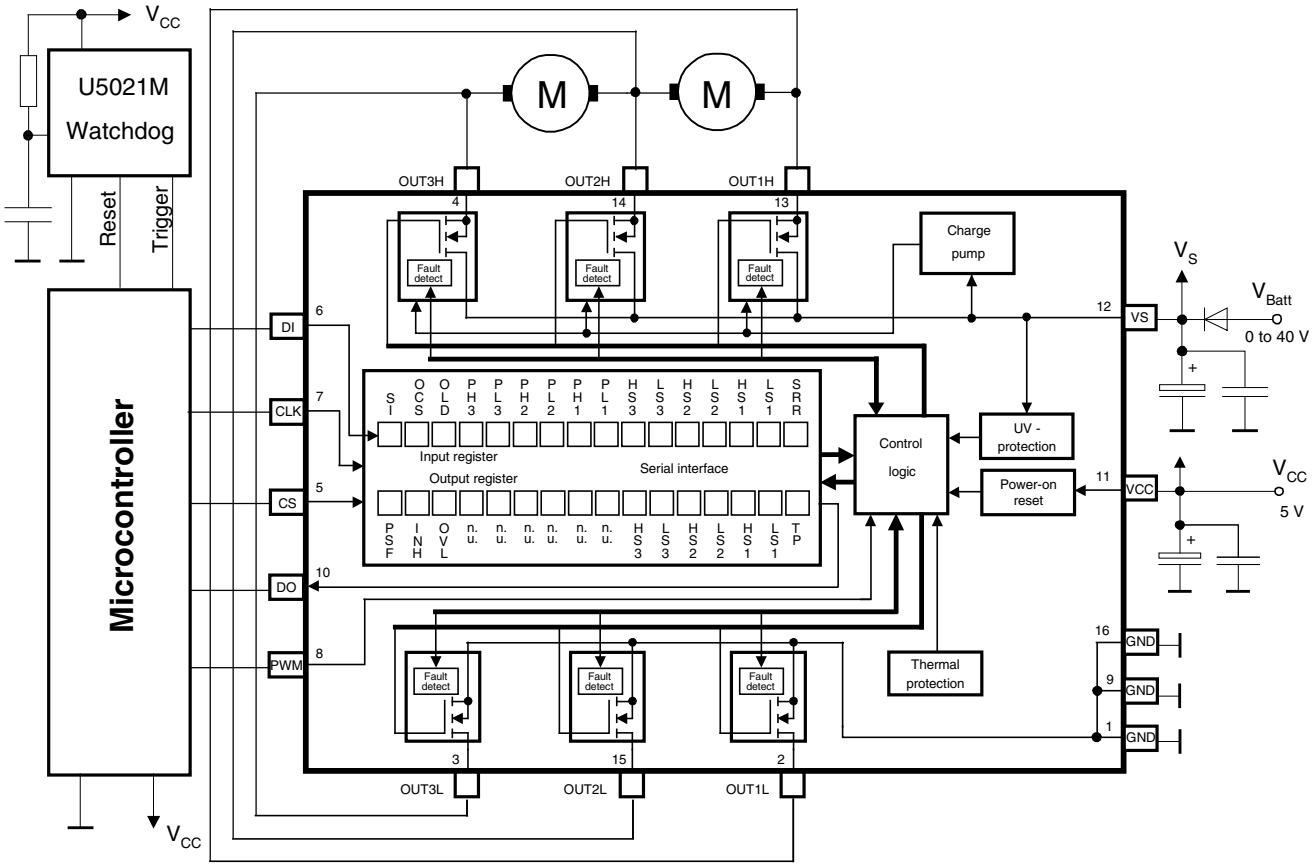
Figure 9-1. Serial Interface Timing with Chart Number



Inputs DI, CLK, CS: High level = 0.7 x V_{CC}, low level = 0.3 x V_{CC}
Output DO: High level = 0.8 x V_{CC}, low level = 0.2 x V_{CC}

10. Application Circuit

Figure 10-1. Application Circuit



10.1 Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:

Electrolytic capacitor C > 22µF in parallel with a ceramic capacitor C = 100nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current $I_{Out1,2,3}$ (see “Absolute Maximum Ratings” on page 7).

Recommended value for capacitors at V_{CC}:

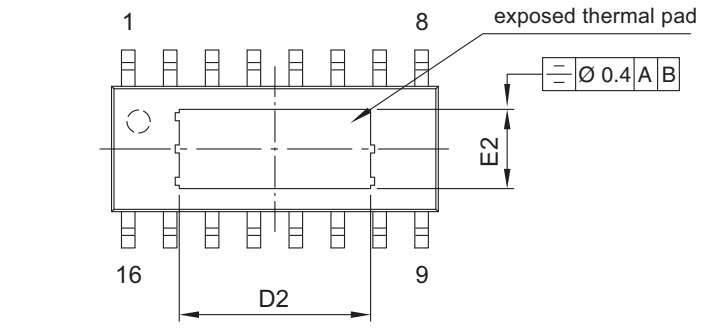
Electrolytic capacitor C > 10µF in parallel with a ceramic capacitor C = 100nF.

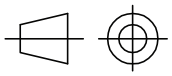
To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to the GND pins. Negative spikes at the output pins (e.g. negative spikes caused by an inductive load switched off with a high side driver) may activate the overtemperature protection function of the Atmel ATA6829. In this condition, the affected output will be switched off. If this behavior is not acceptable or compatible with the specific application functionally, it is necessary, that for switching on required outputs again, the SRR bit (**S**tatus **R**egister **R**eset) is set, to ensure a reset of the overtemperature function.

11. Ordering Information

Extended Type Number	Package	Remarks
ATA6829-T3QY	PSO16	Power package with heat slug, taped and reeled, lead-free

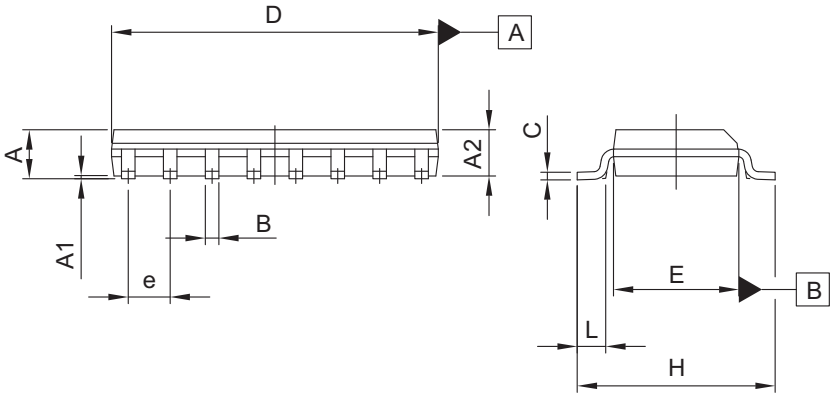
12. Package Information





technical drawings
according to DIN
specifications

Dimensions in mm



Note[1]: Dimensions “D” and “E” do not include Moldflash or protrusion.
(MAX. 0.15mm per side)

Bemerkung: AMKOR

COMMON DIMENSIONS (Unit of Measure = mm)			
Symbol	**MIN**	**NOM**	**MAX**
A	1.43	1.55	1.68
A1	0.00	0.05	0.10
A2	0.43	1.50	1.58
B	0.35	0.41	0.49
C	0.19	0.22	0.25
D[1)]	9.80	9.90	10.00
D2	5.70	5.80	5.90
E[1)]	3.80	3.90	4.00
E2	2.30	2.40	2.50
e		1.27 BSC	
H	5.80	6.00	6.20
L	0.40	0.65	0.90

03/27/12

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Package: ePAD SOIC**		6.541-5052.01-4	1

13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4531H-BCD-04/12	• Package drawing on page 14 updated
4531G-BCD-07/09	• Complete datasheet: T6819 deleted
4531F-BCD-09/05	• Complete datasheet: T6829 changed in ATA6829 • Ordering Information on page 14 changed • Package drawing on page 15 changed

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