NX2601

DUAL SYNCHRONOUS PWM CONTROLLER WITH NMOS LDO CONTROLLER & 5V BIAS REGULATOR

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2601 controller IC is a triple controller with a dual channel synchronous Buck controller IC and an LDO controller designed for multiple converters such as PCIe graphic card applications .The two synchronous PWM controllers are 180 degree out of phase which reduces the input ripple current, allowing to reduce the # of input capacitors.Another main feature of the part is that it can operate from single 12V supply while maintaining a regulated 5V supply for the biasing and the internal drivers. Other features of NX2601 are: programmable frequency from 200kHz to 1MHz, independent digital soft start and enable pins for each controller which allows for different power sequencing, Adaptive driver provides optimized efficiency while maintain sufficient deadband, Vcc undervoltage lock out and current limiting using an Rds-on of the external MOSFET with HICCUP feature.

FEATURES

- Two channel PWM with out of phase operation
- Individual digital soft start for two PWM output and LDO controller
- Bus voltage operation from 2V to 25V
- Hiccup Current limit by sensing Rdson of MOSFET
- Adjustable frequency up to 1Mhz per channel
- Adaptive deadband time
- Three enable pin available allows for independent power sequencing
- MLPQ-32L package offers small size
- Pb-free and RoHS compliant

APPLICATIONS

- PCI Graphic Card on board converters
- Vddq Supply in mother board applications
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- FPGA and Set Top Box Applications

TYPICAL APPLICATION

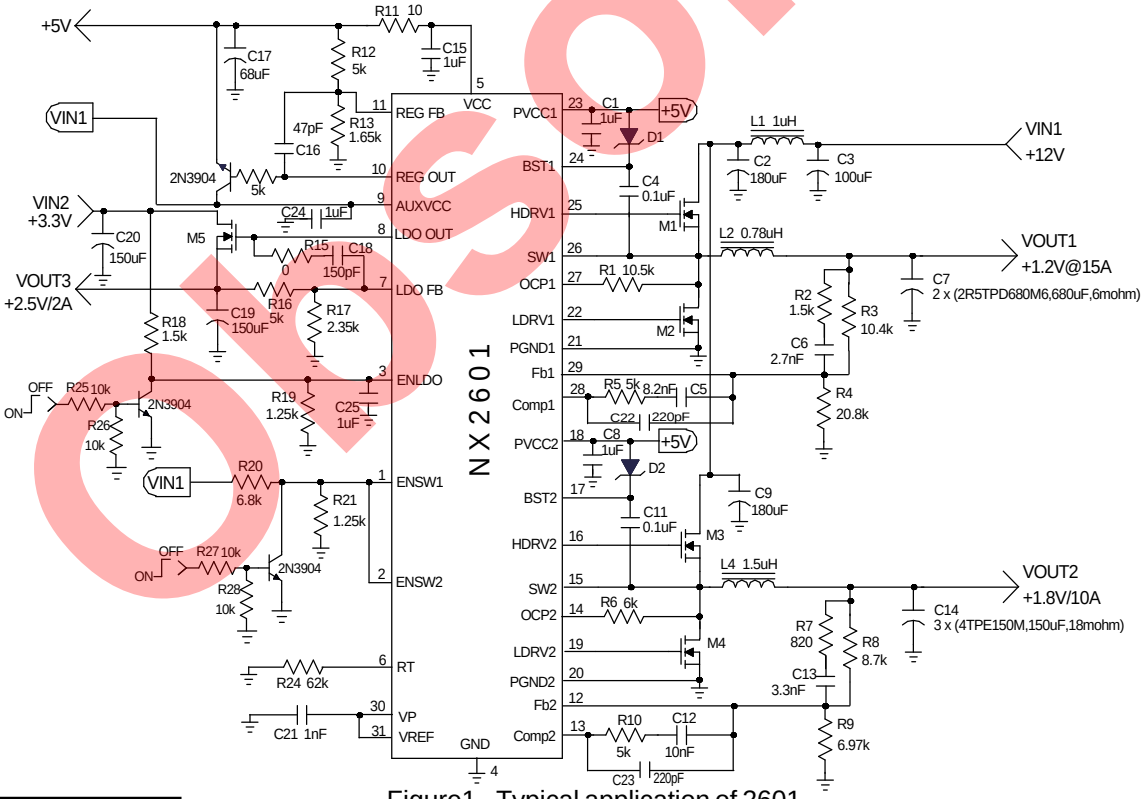

Figure1 - Typical application of 2601

PATENT PENDING

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2601CMTR	0 to 70°C	MLPQ-32L	200kHz to 1MHz	Yes

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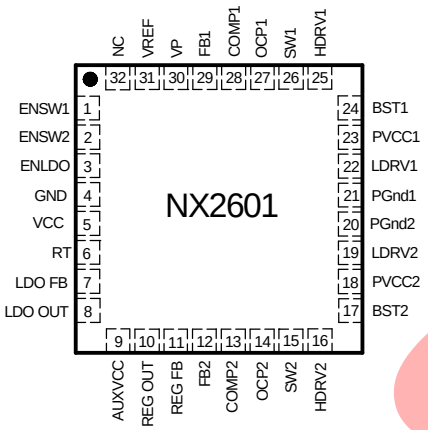
ABSOLUTE MAXIMUM RATINGS

Vcc,PVcc & BST to SW voltage 6.5V
BST Voltage 35V
SW ..... -5V(Note1) to 35V
AUXVCC 35V
All other pins ..... GND to Vcc+0.3V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

32-LEAD 5x5 PLASTIC MLPQ



$\theta_{JA} \approx 35^{o}C/W$

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, V_{BST}-V_{SW}=5V, ENSW1=HIGH, ENSW2=HIGH, ENLDO=HIGH, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
FB Voltage	V_{REF}	4.5 < Vcc < 5.5		0.800		V
FB Voltage Line Regulation				0.4		%
Vcc Supply Voltage						
Vcc Voltage Range	V_{CC}		4.5	5.0	5.5	V
Vcc Static Supply Current	I_{CC_STA}	Outputs not switching		2.0		mA
Vcc Dynamic Supply Current	I_{CC_DYN}	Freq=600kHz, C_{LOAD} = 3300pF		8		mA
V_{BST} Voltage Range	V_{BST}		4.5	5.0	5.5	V
V_{BST} Static Supply Current	I_{BST_STA}	Outputs not switching		2.0		mA
V_{BST} Dynamic Supply Current	I_{BST_DYN}	Freq = 600KHz, C_{LOAD} = 3300pF		TBD		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Under Voltage Lockout						
UVLO Threshold - Vcc	V_{CC_UVLO}	Supply Ramping Up		4		V
UVLO Hysteresis - Vcc	V_{CC_HYST}	Supply Ramping Down		0.2		V
UVLO Threshold - V_{AUXVcc}	V_{AUX_UVLO}	Supply Ramping Up		7		V
UVLO Hysteresis - V_{AUXVcc}	V_{AUX_HYST}	Supply Ramping Down		0.7		V
Error Amplifiers						
Open Loop Gain				65		dB
Input Bias Current				0.3		uA
Input Offset Voltage				0		mV
Oscillator						
Frequency	F_S	Rt=30k,measured at the output drive		600		KHz
Ramp Amplitude	V_{RAMP}			1		V
EN & SS						
Soft Start Time	T_{SS}	Fs=600KHz		3.41		mS
Enable Threshold Voltage				1.25		V
Enable Hysterises		Enable ramp up		100		mV
LDO Controller						
LDO FB Voltage		LDOOUT=LDOFB		0.8		V
FB Pin Bias Current			-0.2	0		µA
LDO_out Output Voltage High		AUXVCC=24V,LDO FB=0.7V I_{O_SOURCE}=1.4mA	22	23.5		V
LDO_out Output Voltage Low		AUXVCC=24V,LDO FB=0.9V I_{O_SINK}=1.4mA		0.2		V
Open Loop Gain		GBNT(Note2)	50			dB
5V AUX REG						
REG FB Voltage		REGOUT=REGFB		1.25		V
FB Pin Bias Current			-0.2	0		µA
REG_out Output Voltage High		AUXVCC=24V,REG FB=1.1V I_{O_SOURCE}=1.4mA	22	23.5		V
REG_out Output Voltage Low		AUXVCC=24V,REG FB=1.4V I_{O_SINK}=1.4mA		0.2		V
Open Loop Gain		GBNT(Note2)	50			dB
High Side driver (CL=3300pF)						
Output Impedance, Sourcing Current	$R_{source—H}$			0.85		ohm
Output Impedance , Sinking Current	$R_{sink—H}$			0.65		ohm
Rise Time	T_{HDRV_RISE}	10% to 90%		25		ns
Fall Time	T_{HDRV_FALL}	90% to 10%		20		ns
Deadband Time	T_{DEAD_LH}	LDRV going Low to HDRV going High, 10% to 10%		30		ns

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PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Low Side driver (CL=3300pF) Output Impedance, Sourcing Current	R_{source_L}			0.85		ohm
Output Impedance , Sinking Current	R_{sink_L}			0.5		ohm
Rise Time	T_{LDRV_RISE}	10% to 90%		25		ns
Fall Time	T_{LDRV_FALL}	90% to 10%		20		ns
Deadband Time	T_{DEAD_HL}	SW going Low to LDRV going High, 10% to 10%		20		ns

Note 1: 500ns transient. This pin can withstand -2V DC.
Note 2: This parameter is guaranteed by design but not tested in production(GBNT).

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	ENSW1	A resistor divider is connected from the respective switcher BUS voltages to these pins that holds off the controllers soft start until this threshold is reached. An external low cost MOSFET or NPN transisitor can be connected to this pin for external enable control.
2	ENSW2	
3	ENLDO	A resistor divider is connected from the LDO bus voltage to this pin that holds off the LDO soft start until this threshold is reached. An external low cost MOSFET can be connected to this pin for external enable control.
4	GND	Analog ground.
5	VCC	IC's supply voltage. This pin biases the internal logic circuits. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin.
6	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND. This frequency is the master clock frequency which is internally divided by two to set each controller frequency.
7	LDO FB	LDO controller feedback input. If the LDOFB pin is pulled below 0.5*Vref, an internal comparator after certain delay and pulls down LDOOUT pin and initiates the HICCUP circuitry. During the startup this latch is not activated, allowing the LDOFB pin to come up and follow the Soft started Vref voltage.
8	LDO OUT	LDO controller output. This pin is controlling the gate of an external NCH MOSFET. The maximum rating of this pin is 16V.
9	AUXVCC	This pin is the supply voltage for the LDO controller as well as the 5V regulator controller that regulates the voltage at Vcc derived from the BUS voltage. The maximum voltage applied to this pin is 30V.
10	REGOUT	The output of the 5V regulator controller that drives a low current low cost external BIPOLAR transistor or an external MOSFET to regulate the voltage at Vcc pin derived from BUS voltage. This eliminates an otherwise external regulator needed in applications where 5V is not available.
11	REGFB	Feedback pin of the 5V regulator controller. A resistor divider is connected from the output of the 5V regulator to this pin to complete the loop.
12	FB2	This pin is the error amplifiers inverting input. These pins are connected via resistor dividers to the output of the switching regulators to set the output DC voltage.
29	FB1	
13	COMP2	These pins are the outputs of error amplifiers and are used to compensate the respective voltage control feedback loops.
28	COMP1	

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
14	OCP2	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source which equals 1.25V divided by Rt resistor is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on. Once this threshold is reached the Hdrv and Ldrv pins are switched low and an internal hiccup circuit is set that recycles the soft start circuit after 2048 switching cycles.
27	OCP1	
15	SW2	These pins are connected to source of high side FETs and provide return path for the high side drivers. They are also used to hold the low side drivers low until this pin is brought low by the action of high side turning off. LDRVs can only go high if SW is below 1V threshold.
26	SW1	
16	HDRV2	High side gate driver outputs.
25	HDRV1	
17	BST2	This pin supplies voltage to high side FET driver. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to these pins and respected SW pins.
24	BST1	
18	PVCC2	Supply voltage for the low side fet drivers. A high frequency 1uF ceramic cap must be connected from this pin to the PGND1 and PGND2 pin as close as possible to the pins.
23	PVCC1	
19	LDRV2	Low side gate driver outputs.
22	LDRV1	
20	PGND2	Power ground pin for low side drivers.
21	PGND1	
30	VP	This pin is the first error amplifier non-inverting input. This pin should be connected either to an external reference voltage (tracking application) or to the internal reference voltage provided by this device.
31	VREF	Reference voltage available. A 100pF capacitor can be connected from this pin to GND. This pin is held low until internal Vcc UVLO and the ENSW 1 pin are good, allowing it to soft start.
32	NC	

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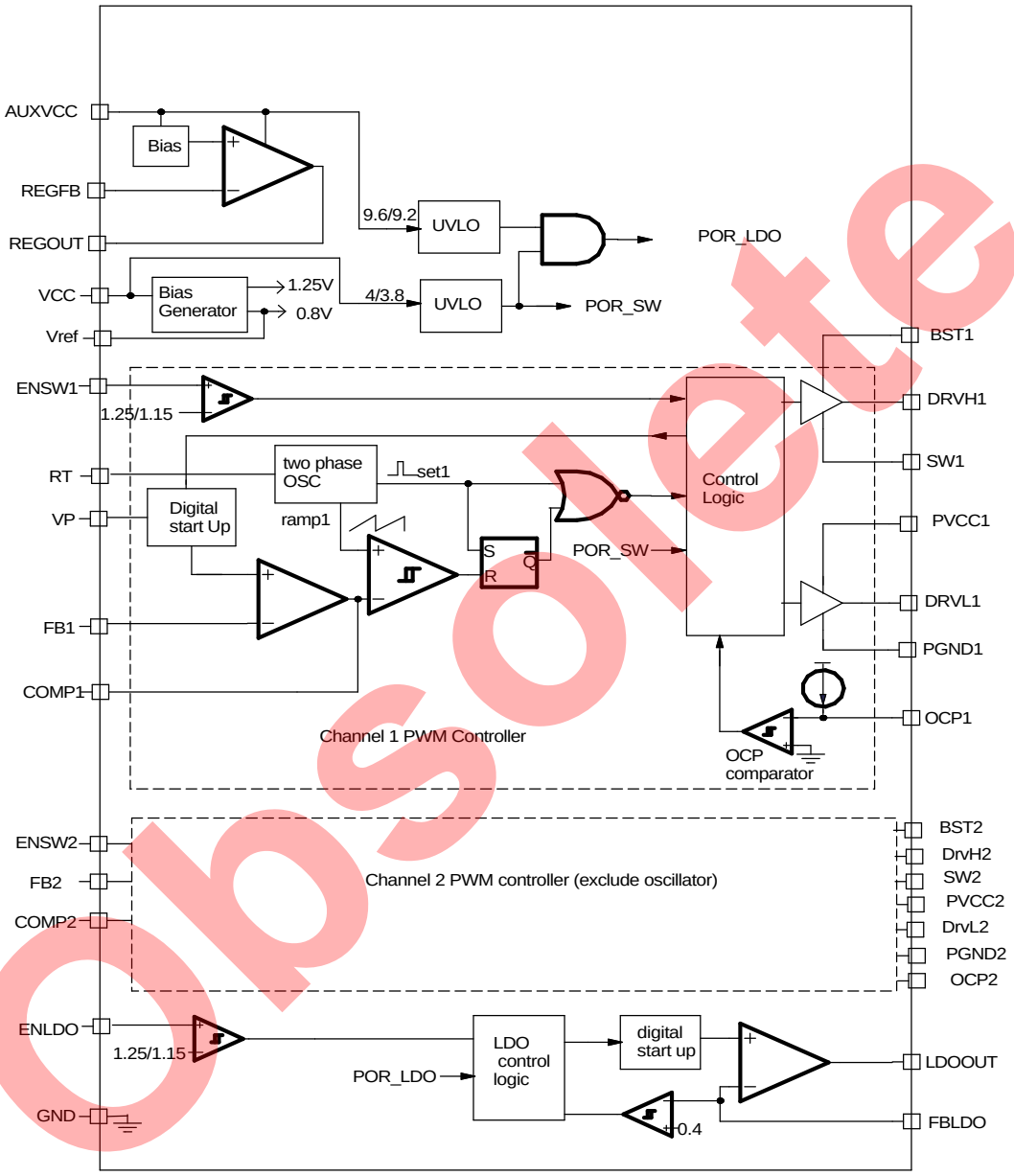
BLOCK DIAGRAM



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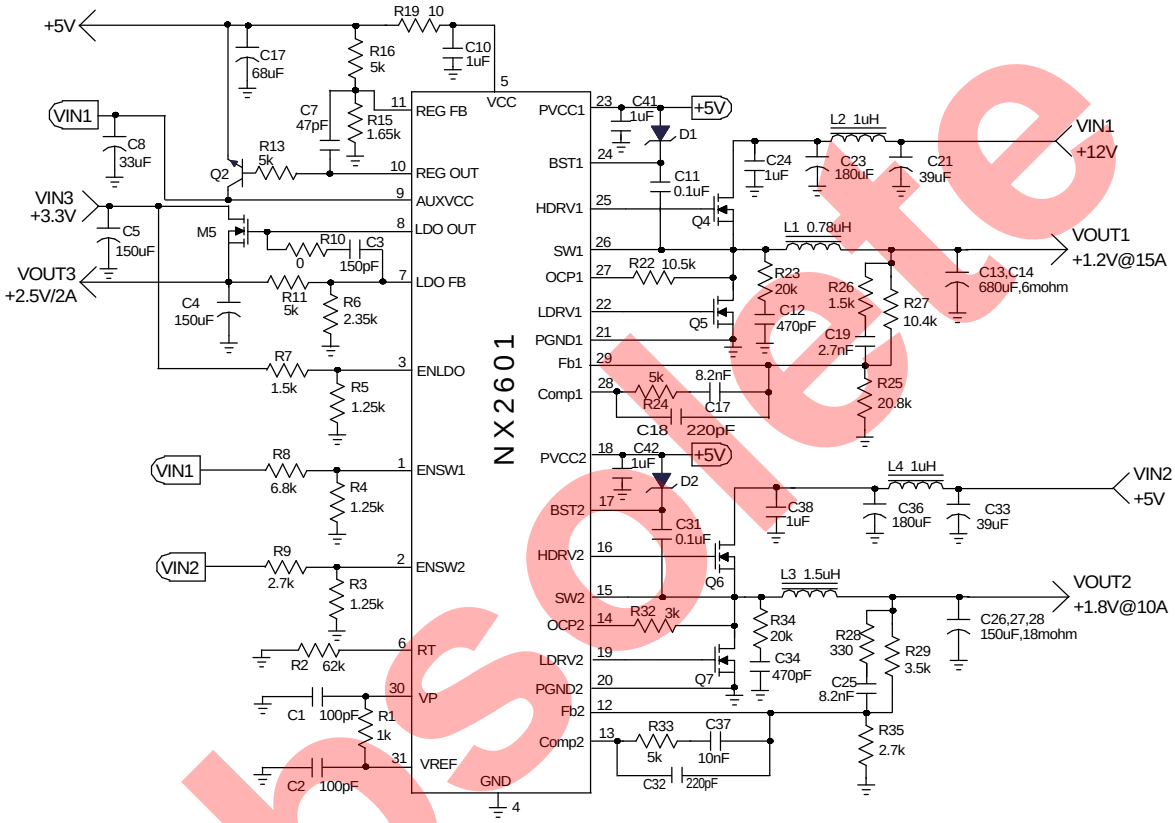

Simplified Demo board schematic

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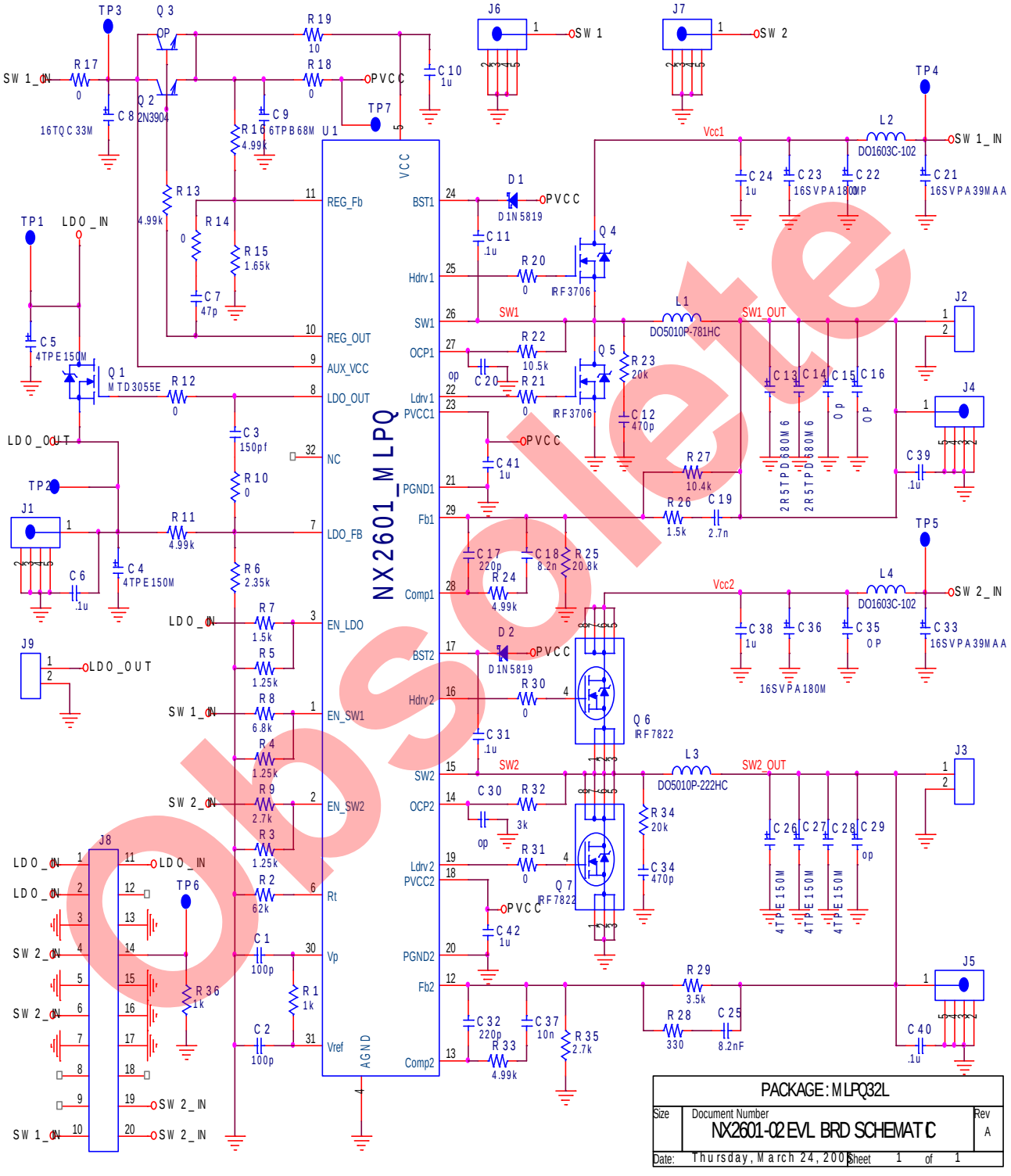

Figure 2 - Demo board schematic based on ORCAD

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Bill of Materials

Item numb	Quantity		Value	Manufacture
1	2	C2,C1	100p	
2	1	C3	150pf	
3	5	C4,C5,C26,C27,C28	4TPE150M	SANYO
4	5	C6,C11,C31,C39,C40	.1u	
5	1	C7	47p	
6	1	C8	16TQC33M	SANYO
7	1	C9	6TPB68M	SANYO
8	5	C10,C24,C38,C41,C42	1u	
9	2	C12,C34	470p	
10	2	C14,C13	2R5TPD680M6	SANYO
11	9	Q3,R14,C15,C16,C20,C22,	OP	
		C29,C30,C35		
12	2	C17,C32	220p	
13	1	C18	8.2n	
14	1	C19	2.7n	
15	2	C21,C33	16SVPA39MAA	SANYO
16	2	C36,C23	16SVPA180M	SANYO
17	1	C25	8.2nF	
18	1	C37	10n	
19	2	D1,D2	D1N5819	
20	5	J1,J4,J5,J6,J7	SCOPE TP	Tektronics
21	3	J2,J3,J9	CON2	
22	1	J8	CON20B	
23	1	L1	DO5010P-781HC	Coilcraft
24	2	L2,L4	DO1603C-102	
25	1	L3	DO5010P-222HC	
26	1	Q1	MTD3055E	
27	1	Q2	2N3904	
28	2	Q4,Q5	IRF3706	International Rectifier
29	2	Q7,Q6	IRF7822	International Rectifier
30	1	R1	1k	
31	1	R2	62k	
32	3	R3,R4,R5	1.25k	
33	1	R6	2.35k	
34	2	R7,R26	1.5k	
35	1	R8	6.8k	
36	2	R35,R9	2.7k	
37	8	R10,R12,R17,R18,R20,R21,	0	
		R30,R31		
38	5	R11,R13,R16,R24,R33	4.99k	
39	1	R15	1.65k	
40	1	R19	10	
41	1	R22	10.5k	
42	2	R34,R23	20k	
43	1	R25	20.8k	
44	1	R27	10.4k	
45	1	R28	330	
46	1	R29	3.5k	
47	1	R32	3k	
48	1	R36	10k	
49	7	TP1,TP2,TP3,TP4,TP5,TP6,	TP	
		TP7		
50	1	U1	NX2601_MLPQ	NEXSEM INC.

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Demoboard waveforms

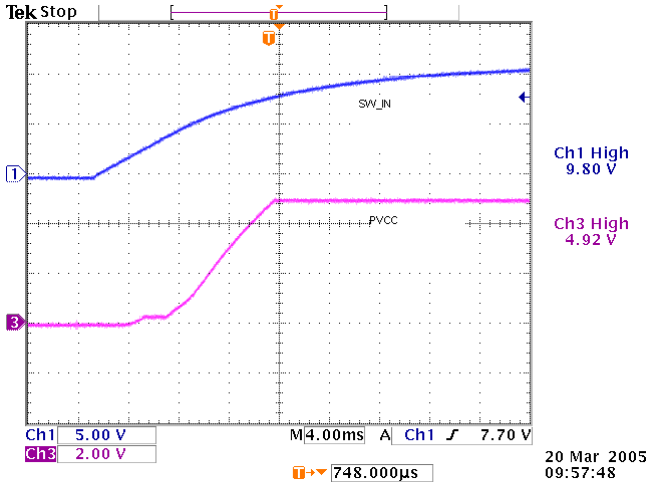

Figure 3 - Start up waveform of VCC by internal regulator. Ch1(AUXVCC), Ch3(VCC&PVCC)

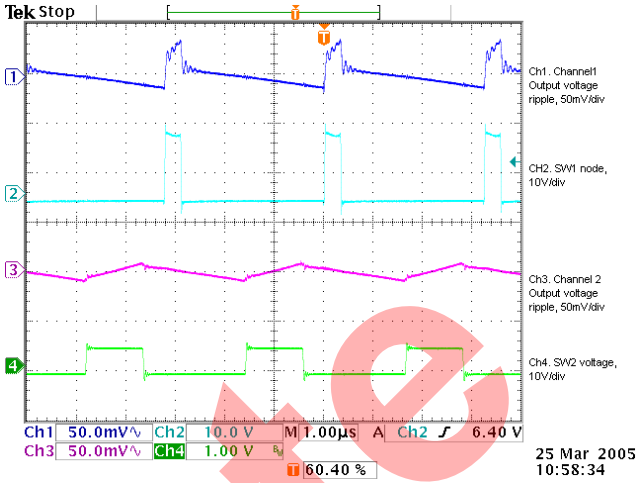

Figure 6 - Output ripple for power output CH1 and CH2

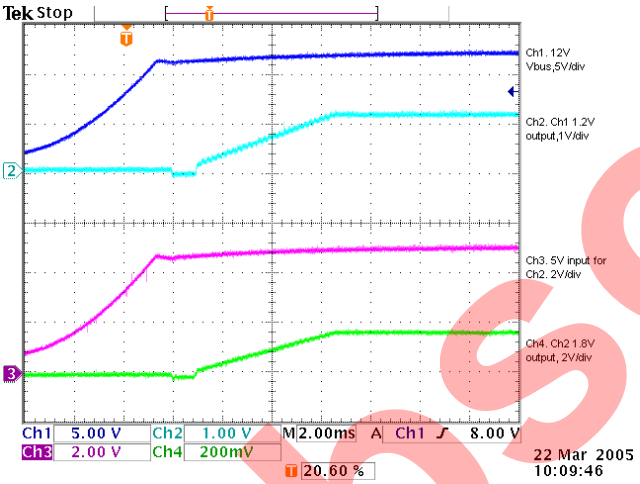

Figure 4 - Soft start for Channel 1 1.2V and chanel 2 1.8V output

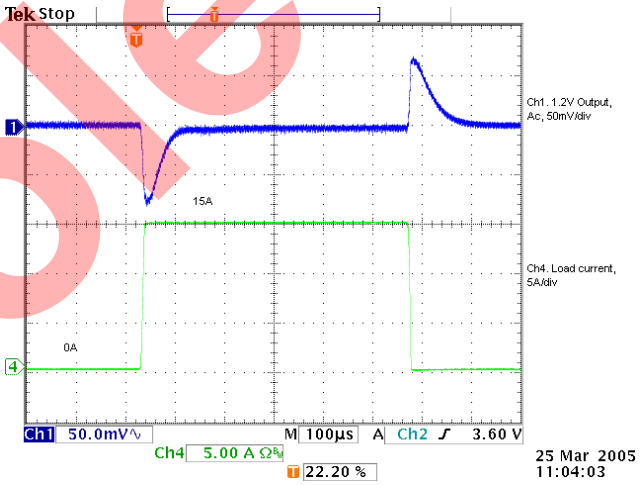

Figure 7-Transient response for first channel 1.2V output

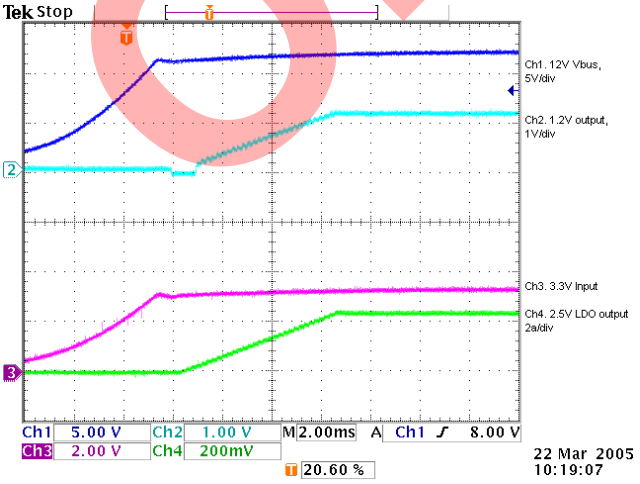

Figure 5 - Soft start for Channel 1 1.2V and LDO output

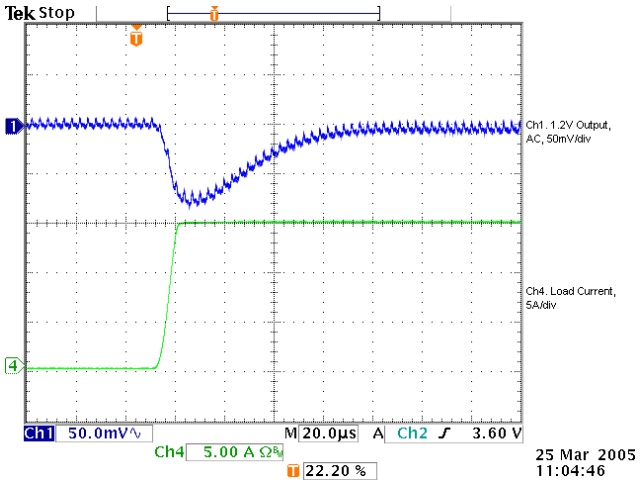

Figure 8 -Transient reponse for Channel 1. (zoomed)

Demo Board Waveforms (Cont')

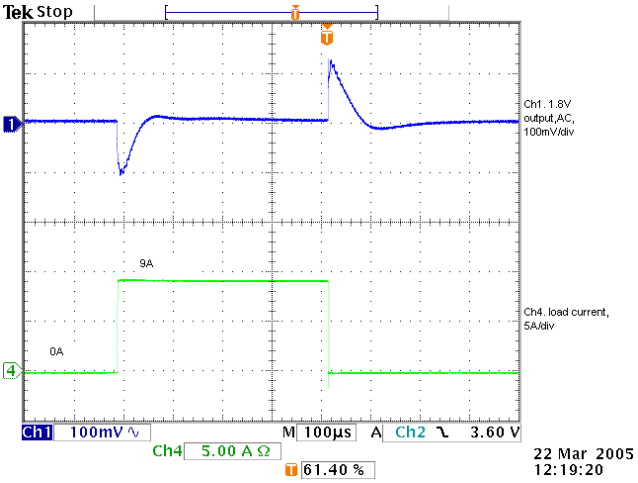

Figure 9 - Ch2 1.8V output transient 0 to 9A.

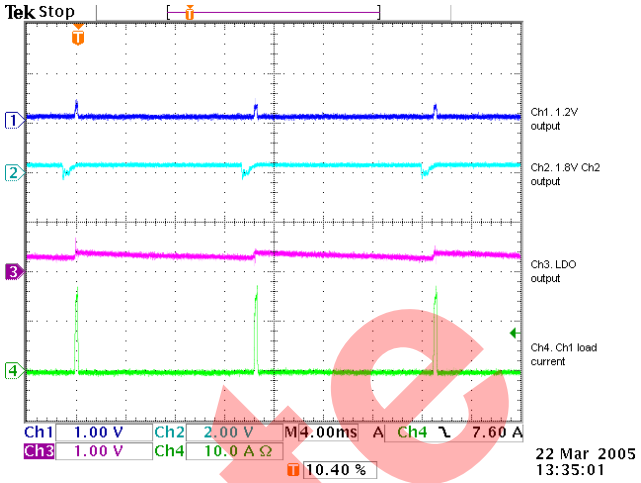

Figure 12 - Ch1 is short. All channels go into hiccup.

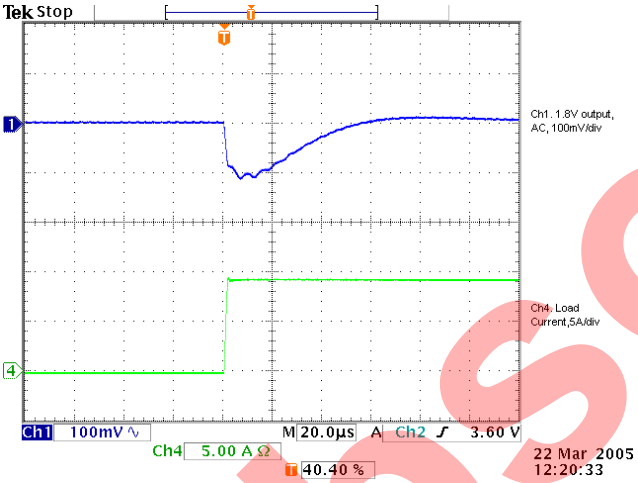

Figure 10 - Ch2 1.8V transient (zoomed)

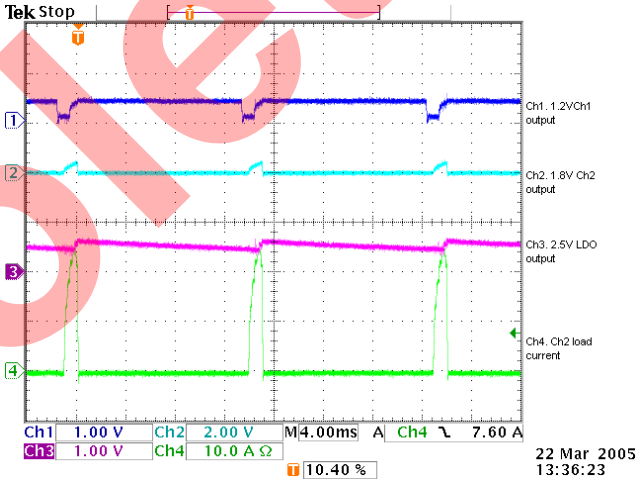

Figure 13 - Ch2 is in short. All channels are in hiccup.

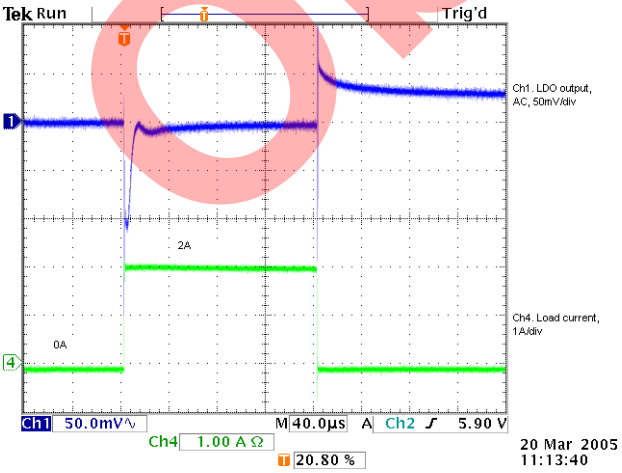

Figure 11 - Transient response for 2.5V LDO output

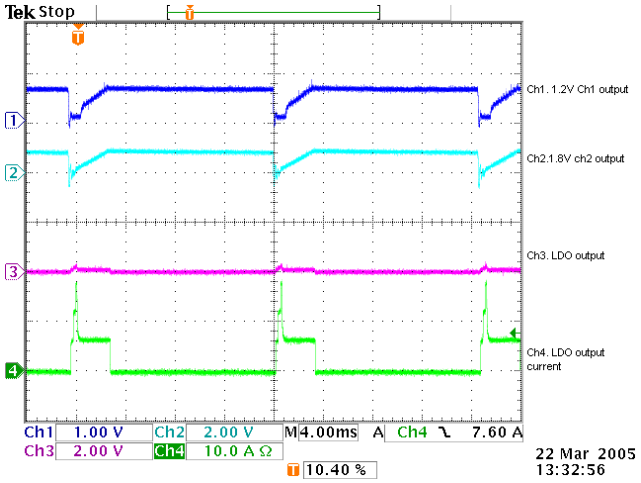

Figure 14 - LDO in short. All channels go into hiccup.

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Switching frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

Power stage design requirements:
V_{IN}=12V
V_{OUT}=1.2V
I_{OUT}=15A
ΔV_{RIPPLE}<=20mV
ΔV_{TRAN}<=100mV @ 15A step
F_S=300kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and higher cost. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.3, then

$$L_{OUT}=\frac{12V-1.2V}{0.3\times 15A}\times\frac{1.2V}{12V}\times\frac{1}{300kHz}$$

L_{OUT}=0.8uH

Choose L_{OUT}=0.78uH, then coilcraft inductor DO5010P-781HC is a good choice.

Current Ripple is calculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$
$$=\frac{12V-1.2V}{0.78uH}\times\frac{1.2V}{12V}\times\frac{1}{300kHz}=4.6A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{20mV}{4.6A}=4.3m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 20mV output ripple, POSCAP 2R5TPD680M6 with 6mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{6m\Omega\times 4.6A}{20mV}$$

N =1.38

The number of capacitor has to be round up to a integer. Choose N =2.

If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is likely to dependent on the ESR of capacitor.

For most cases, the output capacitors are multiple capacitor in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 15A load step.

If the POSCAP 2R5TPD680M6 (680uF, 6mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{6m\Omega \times 680\mu F \times 1.2V}{15A} = 0.33\mu H$$

The selected inductor is 0.78uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E = \frac{0.78\mu H \times 15A}{1.2V} - 6m\Omega \times 680\mu F = 5.67us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 = \frac{6m\Omega \times 15A}{100mV} + \frac{1.2V}{2 \times 0.78\mu H \times 680\mu F \times 100mV} \times (5.67us)^2 = 1.3$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to choose after the test. Typically, for high

frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% up 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitics can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0db with -20db/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo OSCON and POSCAP, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by voltage mode amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

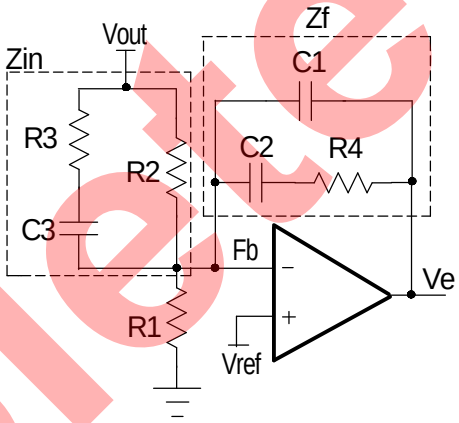
$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 15.

The transfer function of type III compensator is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1}{sR_2\times(C_2+C_1)}\times\frac{(1+sR_4\times C_2)\times[1+s(R_2+R_3)\times C_3]}{(1+sR_4\times\frac{C_2\times C_1}{C_2+C_1})\times(1+sR_3\times C_3)}$$



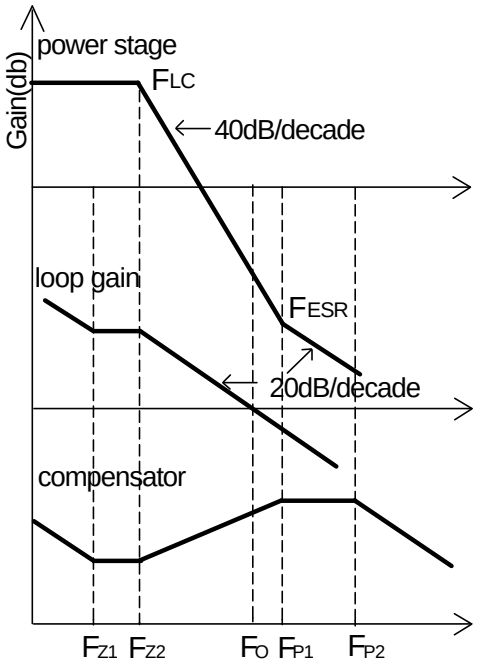


Figure 15 - Type III compensator and its bode plot

The crossover frequency usually is selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10\sim1/5F_s$ for type III compensator .

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR} .

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{0.78uH\times1320uF}}$$
$$=4.89kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times3m\Omega\times1360uF}$$
$$=39kHz$$

2.Set R_2 equal to10.4kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{10.4k\Omega\times0.8V}{1.2V-0.8V}=20.8k\Omega$$

Choose R_1= 20.8kΩ.

3. Set zero F_{Z2} = F_{LC} and F_{p1} =F_{ESR} .

4. Calculate R_4 and C_3 with the crossover frequency smaller than 1/10~ 1/5 of the swithing frequency. Set F_O=25kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times(\frac{1}{F_{z2}}-\frac{1}{F_{p1}})$$
$$=\frac{1}{2\times\pi\times10.4k\Omega}\times(\frac{1}{4.89kHz}-\frac{1}{39kHz})$$
$$=2.8nF$$

Choose C_3=2.7nF.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}$$
$$=\frac{1V}{12V}\times\frac{2\times\pi\times25kHz\times0.8uH}{2.7nF}\times1360uF$$
$$=5.3k\Omega$$

Choose R_4=5k

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}$$
$$=\frac{1}{2\times\pi\times0.75\times4.89kHz\times5k\Omega}$$
$$=8.8nF$$

Choose C_2=8.2nF

6. Calculate C_1 by equation (14) with pole F_{p2} at half the swithing frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}$$
$$=\frac{1}{2\times\pi\times5k\Omega\times150kHz}$$
$$=212pF$$

Choose C_1=220pF

7. Calculate R_3 by equation (13).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}$$
$$=\frac{1}{2\times\pi\times39kHz\times2.7nF}$$
$$=1.5k\Omega$$

Choose R_3= 1.5kΩ.

B. Type II compensator design

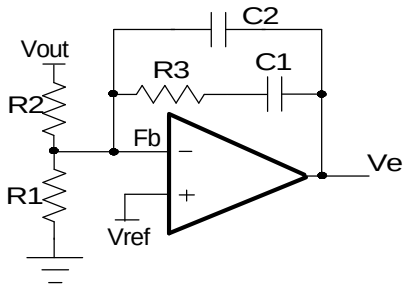
If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit as shown in figure 16.R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=\frac{R_3}{R_2} \quad \text{... (15)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p=\frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$



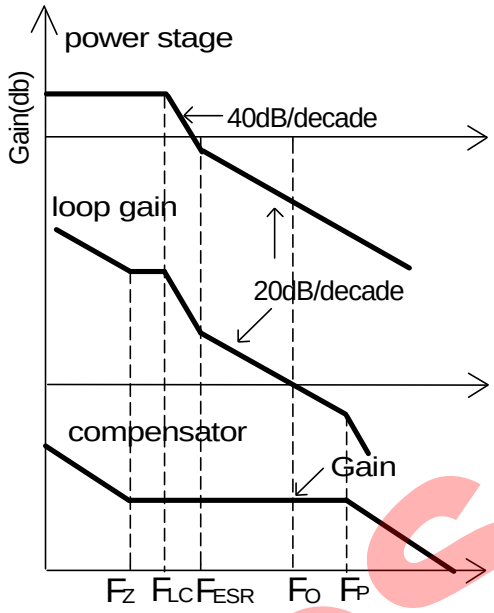


Figure 16 - Type II compensator and its bode plot

For type II compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

The following parameters are used as an example for type II compensator design, three 1500uF with 19mohm Sanyo electrolytic CAP 6MV1500WGL are used as output capacitors. Coilcraft DO5010P-152HC 1.5uH is used as output inductor. The other power stage information is that:

V_{IN}=12V, V_{OUT}=1.2V, I_{OUT} =15A, F_S=200kHz.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{1.5uH\times 4500uF}}$$
$$=1.94kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 6.33m\Omega\times 4500uF}$$
$$=5.6kHz$$

2.Set crossover frequency F_O=20kHz>>F_{ESR}.

3. Set R_2 equal to10kΩ. Based on output voltage, using equation 18, the final selection of R_1 is 20kΩ.

4.Calculate R_3 value by the following equation.

$$R_3=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times R_2$$
$$=\frac{1V}{12V}\times\frac{2\times\pi\times 20kHz\times 1.5uH}{6.33m\Omega}\times 10k\Omega$$
$$=24.8k\Omega$$

Choose R_3 =24.8kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1=\frac{1}{2\times\pi\times R_3\times F_z}$$
$$=\frac{1}{2\times\pi\times 24.8k\Omega\times 0.75\times 1.94kHz}$$
$$=4.4nF$$

Choose C_1=4.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2=\frac{1}{\pi\times R_3\times F_s}$$
$$=\frac{1}{\pi\times 24.8k\Omega\times 200kHz}$$
$$=64pF$$

Choose C_2=68pF

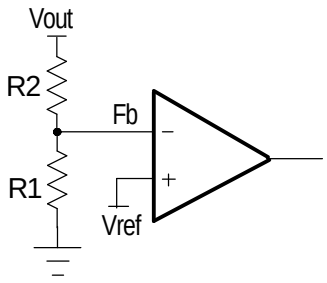
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Choose R_2=10kΩ, to set the output voltage at 1.8V, the result of R_1 is 8kΩ.



Voltage divider

Figure 17 - Voltage divider

In general, the minimum output load impedance including the resistor divider should be less than 5kΩ to prevent overcharge the output voltage by leakage current (e.g. Error Amplifier feedback pin bias current). A minimum load for 5kΩ less (<1/16w for most of application) is recommended to put at the output. For example, in this application,

Vout=1.6V

The power loss is 1/16W less

$$R_{LOAD} = 1.6V \times 1.6V / (1/16W) = 40\Omega$$

Select minimum load is 1kΩ should be good enough.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitor can be calculated

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$

$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(19)$$

V_{IN} = 12V, V_{OUT}=1.2V, I_{OUT}=15A, using equation (19), the result of input RMS current is 4.5A.

For higher efficiency, low ESR capacitors are recommended.

Two Sanyo OS-CON SVPA180M 16V 180uF 29mΩ with 3.4A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The NX2601 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two IRFR3706 are used. They have the following parameters: V_{DS}=30V, I_D =75A,R_{DSON} =9mΩ,Q_{GATE} =23nC.

There are three factors causing the MOSFET power loss:conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(20)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

According to equation (3), P_{GATE} =0.07W. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1-D) \times R_{DS(ON)} \times K \quad ...(21)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K equals to 1.4 at 125°C according to IRFR3706 datasheet. Using equation (4), the result of P_{TOTAL} is 0.54W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(22)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. The result of P_{SW} is 1.5W. Swithing loss P_{SW} is frequency dependent.

Soft Start and Enable

NX2601 has two switching controller and one LDO controller. Each of them has individual digital soft start. Each channel has one enable pin for start up. When the Power Ready (POR) signal is high and the voltage at enable pin is above 1.25V, the internal digital counter starts to operate and the voltage at positive input of Error amplifier starts to increase, the feedback network will force the output voltage follows the reference and starts the output slowly. After 2048 cycles, the soft start is complete and the output voltage is regulated to the desired voltage decided by the feedback resistor divider

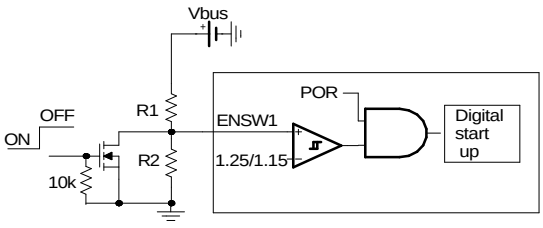


Figure 18 - Enable and Shut down the NX2601 with Enable pin.

The start up of NX2601 can be programmed through resistor divider at Enable pin. For example, for channel 1, if the input bus voltage is 12V and we want NX2601 starts when Vbus is above 8V. We can select

R2=1.24k

$$R_1 = \frac{(8V - 1.25V) \times R_2}{1.25V} = 6.8k\Omega$$

The NX2601 can be turned off by pulling down the ENable pin by extra signal MOSFET as shown in the above Figure. When Enable pin (ENSW1) is below 1.15V, the digital soft start is reset to zero. In addition, all the high side is off and output voltage is turned off.

Frequency Selection

The frequency can be set by external Rt resistor. The relationship between frequency and RT pin is shown as follows.

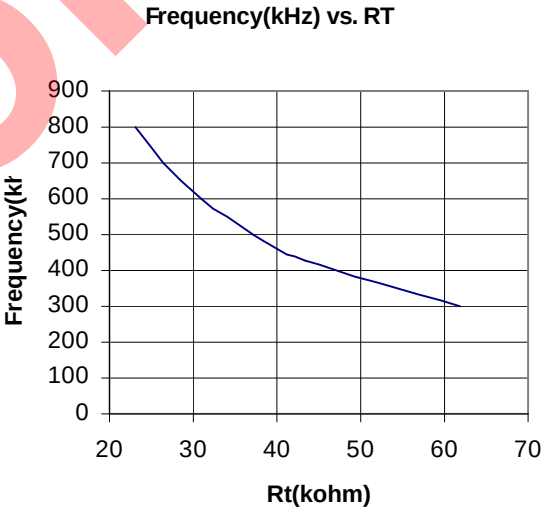


Figure 19 - Frequency versus Rt resistor

For example, for 300kHz operation, Rt is about 62kohm.

Over Current Limit Protection

Over current limit for step down converter is achieved by sensing current through the low side

MOSFET. Inside NX2601, the current through Rt pin is mirrored and injecting to the pin OCP. Since the current through Rt pin is decided as

$$I_{RT} = \frac{1.25}{R_t}$$

This current is very accurate and does not change with silicon process and temperature, the over current limit tripping point can be set more accurate than traditional current source. This scheme is the property of Nexsem. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs. The over current limit can be set by the following equation

$$I_{SET} = I_{RT} \times R_{OCP} / R_{DSON}$$

For example, For 20A current limit and 9mohm Rdson for IRFR3706, the OCP set resistor is calculated as

$$I_{RT} = \frac{1.25V}{62k} = 20uA$$

$$R_{OCP} = \frac{I_{SET}}{I_{RT}} \times R_{DSON} = \frac{20A}{20uA} \times 9mohm = 9kohm$$

Select OCP set resistor R=10.5k.

For NX2601, if one channel goes to hiccup current limit, the other channels include LDO will go to hiccup too.

LDO Selection Guide

NX2601 offers a LDO controller. The selection of MOSFET to meet LDO is more straight forward. The selection is that the Rdson of MOSFET should meet the dropout requirement. For example.

V_{LDOIN} =3.3V

V_{LDOOUT} =2.5V

I_{Load} =2A

The maximum Rdson of MOSFET should be

$$R_{RDSON} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) / 2A = 0.4\Omega$$

Most of MOSFETs can meet the requirement. More important is that MOSFET has to be selected right package to handle the thermal capability. For LDO, maximum power dissipation is given as

$$P_{LOSS} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) \times 2A = 1.6W$$

Select IR MOSFET IRFR3706 with 9mΩ R_{DSON} is sufficient.

LDO Compensation

The diagram of LDO controller including VCC regulator is shown in above figure 20. For low frequency capacitor such as electrolytic, POSCAP, OSCON, etc, The compensation parameter can be calculated as follows.

$$C_C = \frac{1}{2 \times \pi \times F_O \times R_{f1}} \times \frac{g_m \times ESR}{1 + g_m \times ESR}$$

where F_O is the desired loop gain.

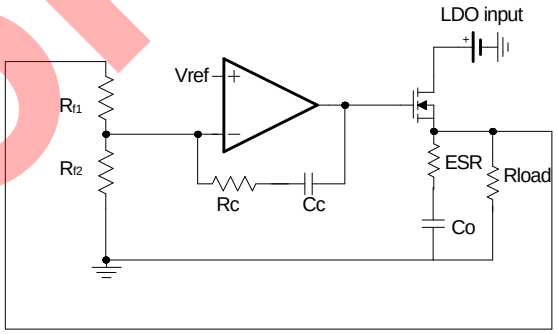


Figure 20 - NX2601 LDO controller.

Typically, F_O has to be higher than zero caused by ESR. F_O is typically around several tens kHz to a few hundred kHz. For this example, we select Fo=100kHz. g_m is the forward trans-conductance of MOSFET.

For IRFR3706, g_m=53.

Select R_{f1}=5kohm.

Output capacitor is Sanyo POSCAP 4TPE150MI with 150uF, ESR=18mohm.

$$C_C = \frac{1}{2 \times \pi \times 100kHz \times 5k\Omega} \times \frac{53 \times 18m\Omega}{1 + 53 \times 18m\Omega} = 155pF$$

Choose C_C=150pF.

For electrolytic or POSCAP, R_C is typically selected to be zero.

R_{f2} is determined by the desired output voltage

$$R_{f2} = R_{f1} \times V_{REF} / (V_{LDOOUT} - V_{REF})$$
$$= 5k\Omega \times 0.8V / (2.5V - 0.8) = 2.35k\Omega$$

Choose R_{f2}=2.34kΩ.

Current Limit for LDO

Current limit of LDO is achieved by sensing the LDO feedback voltage. When LDO_FB pin is below 0.4V, the IC goes into hiccup mode. The IC will turn off all the channel (Channel 1 and Channel 2) for 2096 cycles and start to restart system again.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

TYPICAL APPLICATIONS

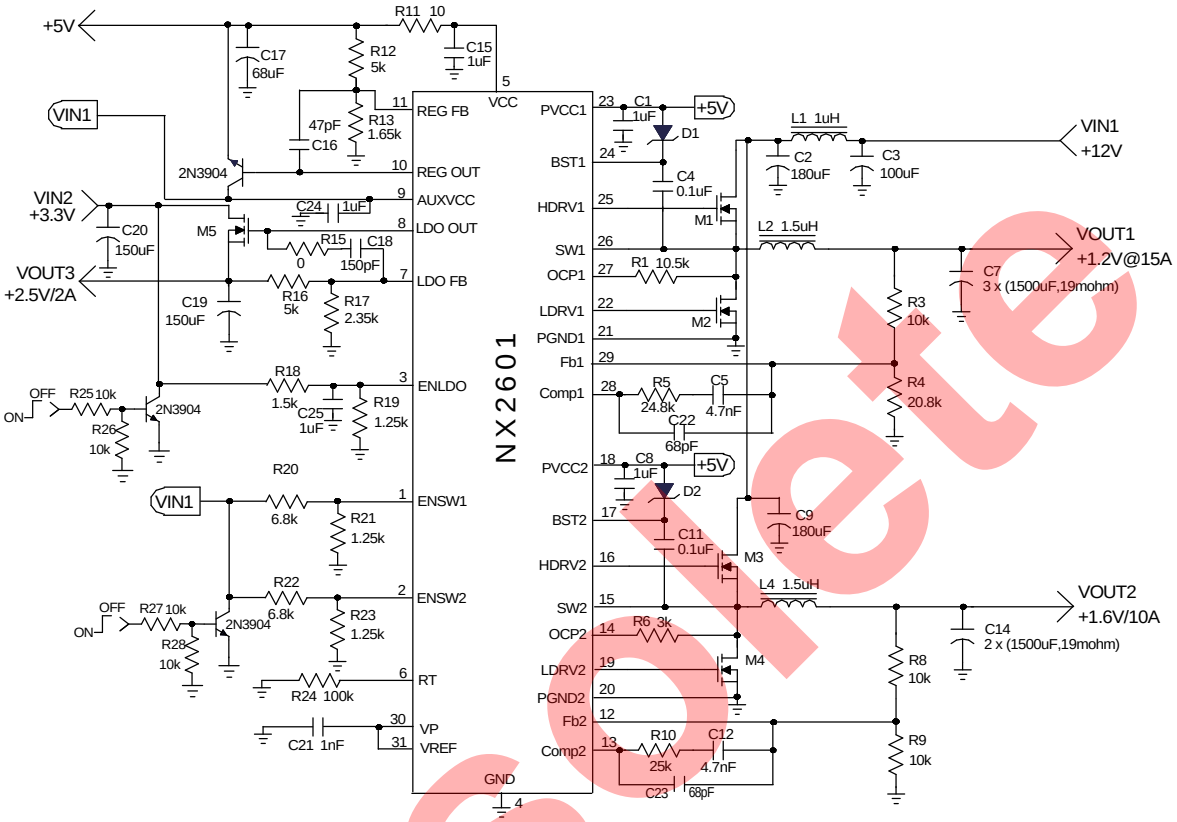


Figure 21 - NX2601 application with electrolytic capacitors as output capacitors

Microsemi
Analog Mixed Signal Group
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TYPICAL APPLICATIONS(cont')

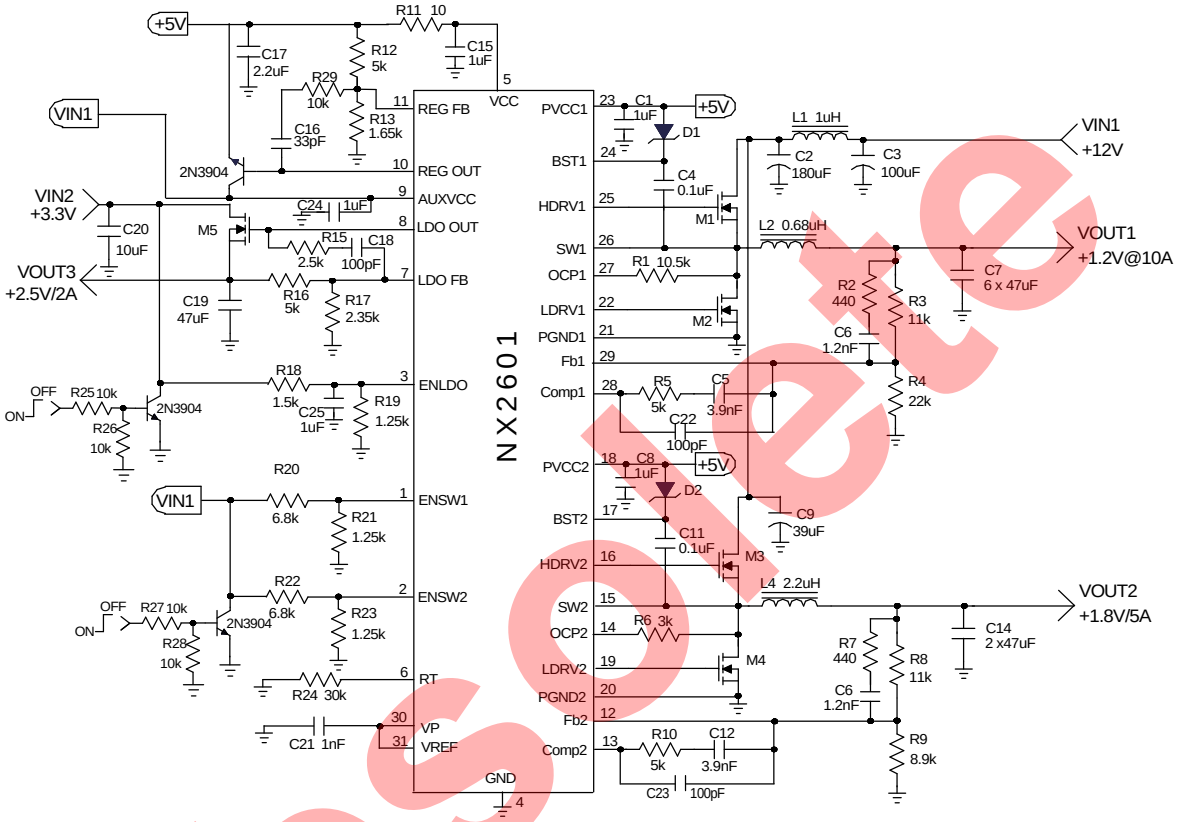

Figure 22 - NX2601 application with ceramic capacitors as output capacitors

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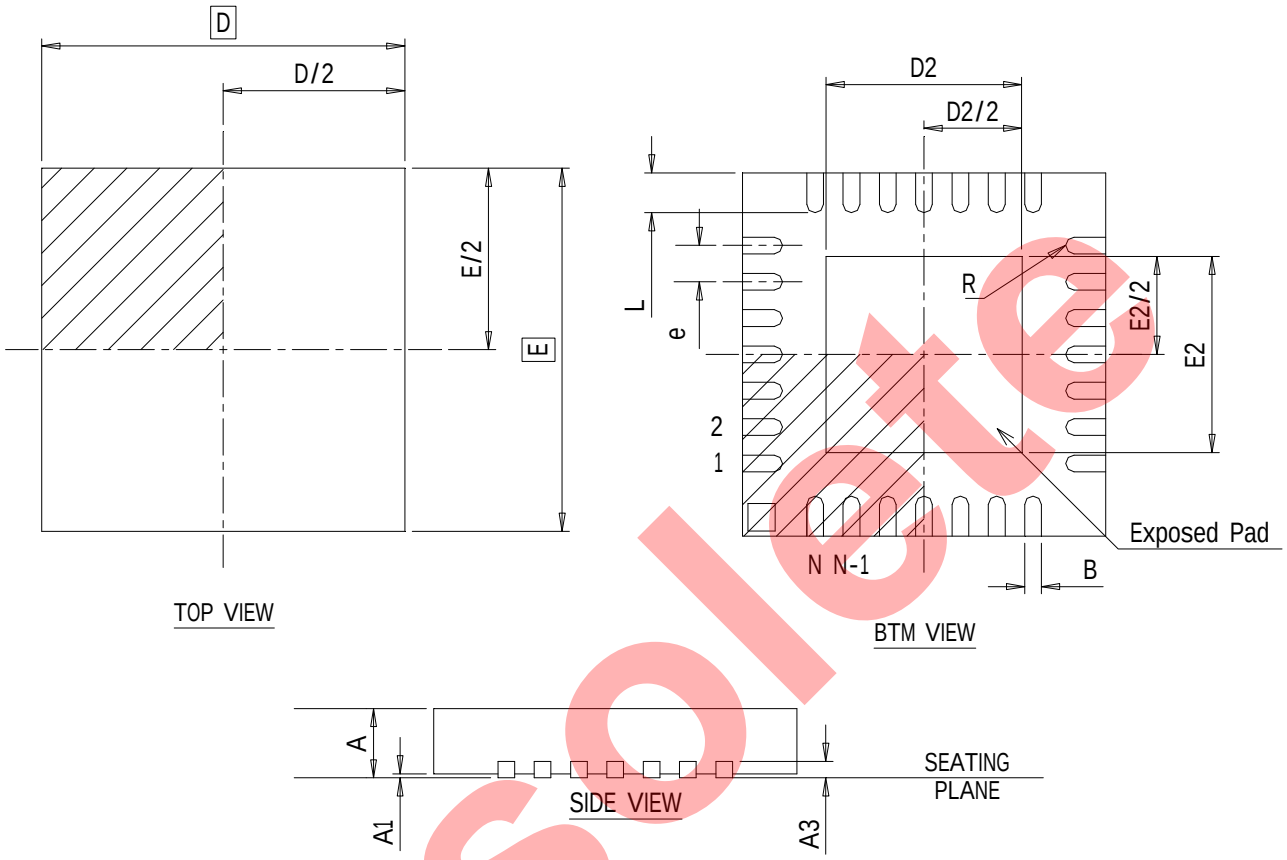
MLPQ 32 PIN 5 x 5 PACKAGE OUTLINE DIMENSIONS



SYMBOL NAME	32 PIN 5 x 5		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20REF	
B	0.18	0.25	0.30
D		5.00BSC	
D2	3.30	3.45	3.55
E		5.00BSC	
E2	3.30	3.45	3.55
e		0.50BSC	
L	0.30	0.40	0.50
R	0.09	---	---
ND		6	
NE		6	

NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.
ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

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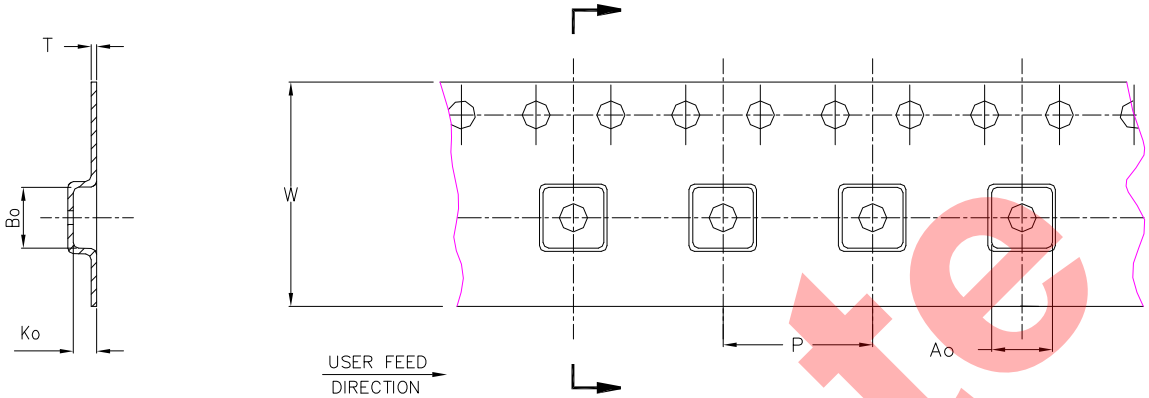
MLPQ 32 PIN 5 x 5 TAPE AND REEL INFORMATION



Dimension	MLPQ 05X05
Ao	5.30 +/− 0.1
Bo	6.30 +/− 0.1
Ko	1.2 +/− 0.1
P	8 +/− 0.1
W	12 +/− 0.3
T	0.3 +/− 0.05
R7/Quantity	1000
R13/Quantity	3000

NOTE:
1. R7 = 7 INCH LOCK REEL, R13 = 13 INCH LOCK REEL.
2. ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.

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