PD69012

12 Ports Power Over Ethernet Manager

DATASHEET

DESCRIPTION

Microsemi's PD69012 Power over Ethernet (PoE) Manager chip integrates power, analog and State of the art Embedded Core Logic into a single 80-pin, plastic QFP package. The device is used in Ethernet switches and Midspans to allow network devices to share power and data over the same cable.

PD69012 device is a 12-port, mixed-signal, high-voltage Power over Ethernet driver. It allows detection of IEEE802.3af-2003 compliant PDs (Powered Devices) and IEEE802.3AT High Power Devices, thus, ensuring safe power feeding and disconnection of ports. With full digital control via a serial communication interface and a minimum of external components, the device integrates into multi-port and highly populated Ethernet switches and routers.

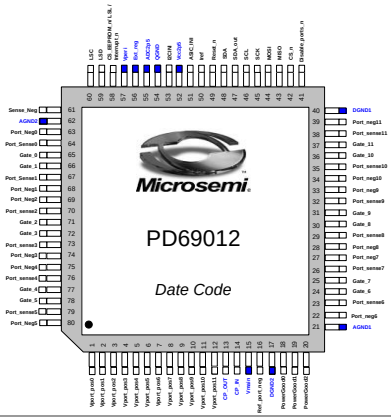
The PD69012 executes all real time functions as specified in the IEEE802.3af-2003 ("AF") standard and IEEE802.3at High Power ("AT") functionality, including: Load detection, "AF" and "AT" classification and port status monitoring, as well as system level activities such as: power management and MIB support for system management. The PoE device is designed to detect and disable disconnected ports, utilizing both DC and AC disconnection methods, as specified in the IEEE 802.3af-2003 standard.

The PD69012 is designed to support 2 main configurations:

- Auto mode: For Basic "AF" and "AT" PSE equipment
- Enhanced mode: For High End, Extended features set of AF and AT PSE equipment.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

PACKAGE PIN OUT



KEY FEATURES

PD69012 Auto Mode features:

- Fully IEEE802.3af-2003 compliant
- Designed to support IEEE802.3at including two-event classification
- Supports pre-standard PD detection
- Supports Cisco devices detection
- IETF Power Ethernet MIB (RFC 3621) compliant
- Single DC voltage input (44v-57v)
- Wide temperature range: -40° C to +85° C
- Low thermal dissipation (0.5Ω sense resistor)
- Drives 12 independent two-pairs power ports or 6 independent 4-pairs ports
- Can cascade up to 8 PoE devices (96 ports)
- EEPROM interface for software patching and parameter configuration
- I^2C Host interface
- Supports Interrupt out pin
- Dynamic power management
- Emergency power management supporting three configurable Power Bank I/Os
- Direct register communication
- Direct LED drive
- Continuous monitoring per port and system data
- Parameter setting per port and per system
- Power soft start algorithm
- Thermal monitoring/protection
- Voltage monitoring/protection
- H/W disable ports input
- Built in 3.3 V regulator
- Internal power on reset
- Enhanced SPI bus for internal communication
- External EEPROM for system parameters update
- SW ROM patch option
- RoHS compliant

Enhanced Modes Additional Features:

- I^2C or UART host interface
- Serial Communication Protocol backwards compatible with PD63000 and PDIC66000
- Additional monitoring
- Extended parameter setting
- Port matrix for flexible PCB layout
- Field upgradeable software
- Emergency Power Management with four power supplies

PACKAGE ORDER INFO

T_A (°C)		
	LF	**Plastic 12x12x1.4 mm LQFP 80 pin**
	RoHS Compliant / Pb-free / MSL3	
-40 to 85	**PD69012**	

Note: This datasheet refers to ICs with date code "XAA0843" or later.

Date code: See the bottom line (XAA0843) in the Pin Configuration drawing. Where "*0843*" is the date code, "*08*"IS the year (2008), and "*43*" is the week

THERMAL DATA

θ_{JA} = 25 °C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PD69012

Microsemi
CPG – PoE BU
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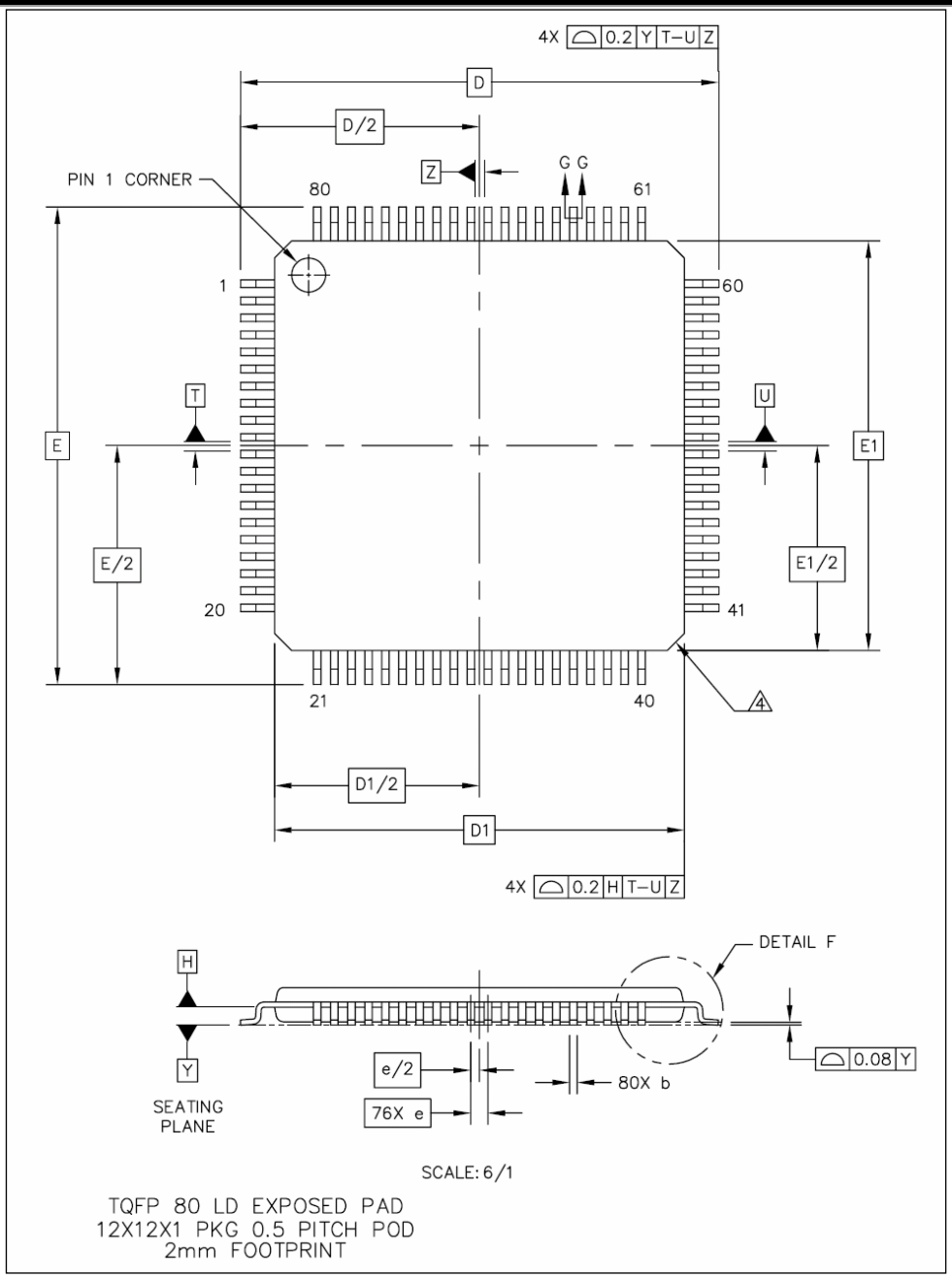
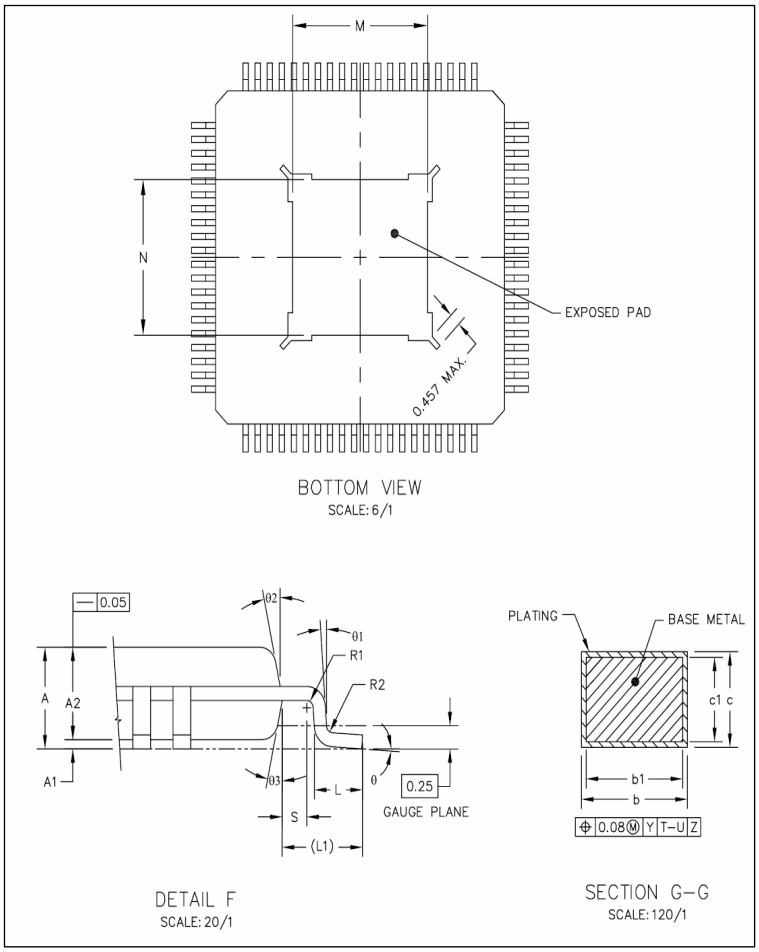
PACKAGE INFORMATION



TQFP 80 LD EXPOSED PAD
12X12X1 PKG 0.5 PITCH POD
2mm FOOTPRINT

PD69012



NOTES:

1. DATUMS T, U AND Z TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
2. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D AND E ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAM BAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

⚠ EXACT SHAPE OF EACH CORNER IS OPTION.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.2	L1		1 REF	
A1	0.05		0.15	R1	0.08		---
A2	0.95	1	1.05	R2	0.08		0.2
b	0.17	0.22	0.27	S	0.2		---
b1	0.17	0.2	0.23	θ	0°		7°
c	0.09		0.2	θ1	0°		---
c1	0.09		0.16	θ2	11°		13°
D		14 BSC		θ3	11°		13°
D1		12 BSC		M	5.5	5.6	5.7
e		0.5 BSC		N	5.5	5.6	5.7
E		14 BSC					
E1		12 BSC					
L	0.45	0.6	0.75				

UNIT	DIMENSION AND TOLERANCES
MM	ASME Y14.5M

Figure 1: PD69012 Package Description

MAIN FEATURES DESCRIPTION	
Feature	**Description**
PD69012 Auto Mode Features	
IEEE802.3af-2003 and IEEE802.3at Compliant	The PD69012 meets all IEEE-802.3AF-2003 standard requirements and all IEEE802.3at draft requirements, such as: • Multi – point resistor detection • AF and AT PD classification function including 2-events • AC disconnect and DC disconnect functions • Supports Back-off feature for Midspan implementation
IETF Power Ethernet MIB (RFC 3621) Compliant	The PD69012 meets all IETF power Ethernet MIB (RFC 3621) requirements such as: port enable/disable, port priority, classification, error counters and system/port power consumption.
Single DC Voltage Input	The PD69012 requires a single DC voltage source: 44V to 57V. No additional voltage sources (e.g. 3.3V/5V) are required for the PoE system's operation.
Wide temperature range: -40°c to +85°c	The PD69012 can operate in a very wide temperature range: -40°c to +85°c. This wide temperature range enables to integrate the PD69012 into small unventilated boxes and be used in harsh environments.
Low power dissipation (0.5Ω sense resistor and <0.2Ω FET)	The PD69012 has an exposed pad which keeps the device in low temperatures. The Rsense in PD69012 applications is only 0.5Ω, and the external FET can be selected to be less than 0.2Ω reducing power dissipation and allowing for fan-less operation
Drives 12 Independent Power Ports	The PD69012 has high port density (12 ports), integrated into a single device, thus saving PCB space, reducing PoE system cost and simplifying the circuit design.
External Power FET Per Port	The PD69012 is designed to drive 12 external Power FET in order to implement flexible power solution and simplify circuit design, allowing the customer to fit the FET to the temperature and current requirements of the application
Can be Cascaded for up to 8 PoE Devices	PD69012 PoE devices can be cascaded for up to 96 ports PoE system, utilizing 8 PoE devices that fit into an Auto Mode Master/Slave configuration.
I^2C Communication for Internal Interface	Allows communication between the Host CPU and the PoE devices for monitoring and setting.
Power Management	When working in either Auto Mode or Enhanced Mode the system supports the following power management modes: Class mode, Allocation mode, Dynamic and Auto-PM mode that combines all modes. The power management feature is a continuous real-time algorithm utilized to protect against over-power consumption. Disconnection and connection of ports is performed as specified in the power management mode.
Emergency Power Management	Three power supply indication inputs for quick shut down of ports according to pre-defined priority table in cases where power supply failure occurs. Four power supplies are supported in Enhanced Mode
Direct Register Communication	The Host CPU communicates with the PoE devices by writing and reading to/from their registers.
Continuous Monitoring per Port	The Host CPU can receive on-line information per port such as: • Port current and power measurement • Port class • Port Status (on, off, overload, short and more)

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Continuous System data	On-line system telemetries for the Host CPU, such as: • Voltage measurement • Total system and per port power consumption • System and ICs status
Parameter Setting per Port and Per System	Configurable parameters via the Host CPU, such as: • Port priority • Power management parameters (power limit, PM mode) • Forced power and disable power per port • AC/DC disconnect method
Thermal Monitoring/Protection	The PD69012 comprises internal thermal protection, to protect against junction overheating; two temperature sensors are integrated into the device, and are utilized for protection and for temperature monitoring.
H/W Disable Ports	The PD69012 utilizes a dedicated pin (#41), enabling an immediate disconnection of all ports. This disable-ports pin can be controlled via the Host CPU. All ports are disconnected when voltage level on this pin drops. This is the quickest way to turn-off all ports.
Built-In 3.3V Regulator	The PD69012 combined with a few additional components can provide 3.3V up to 30mA for other components, such as PoE Controller and optical devices.
Internal Power on Reset	The Power On Reset circuitry monitors the internal voltage regulators (2.5v, Vperi 3.3v and 10v). If one of these voltages drops below a pre-defined level, the PoE devices reset, until all voltages are functional again.
ESPI Bus for Internal PoE Communication	The Internal PoE Communication between the Master PoE device and the Slave PoE devices is performed via an SPI bus comprising the MOSI, MISO, SCK and a single CS line, with multiplexed address and data.
Pre-Standard PD Detection	Enables detection and powering of pre-standard devices (PDs).
Detection of Cisco Devices	Enables detection and powering of all Cisco devices including pre-standard terminals.
Interrupt - Out	Enables the Host-CPU to reduce communication volume. Whenever a PoE event (masked by the CPU) occurs, the PoE Controller sends an interrupt to the Host for notification. Events are port-based, chip-based, or system-based(1).
LED Support	Direct SPI interface to an external LED Stream circuitry. It enables the designer to implement a simple LED circuit without any software code (1)
Code Patching	SW code updates and configuration using external EEPROM or Downloaded by the HOST CPU (1)

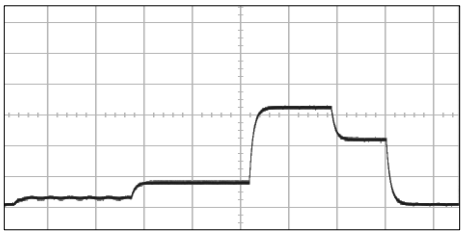
(1) When using Interrupt_n pin - LED stream and external EEPROM support are not available. For more information refer to Microsemi's PoE Application Notes

Feature	Description
Enhanced Modes – Additional Features	
I²C / UART Host interface	Allows I²C communication or UART communication between the Host CPU and the PoE controller for continuous monitoring and for port parameter setting using the Serial Communication Protocol backwards compatible with the PD63000 and the PDIC66000.
Additional Continuous Monitoring per Port and Per System	The Host-CPU can receive additional information from the PoE controller such as: Additional port statuses, port matrix, PoE interrupt events, etc.
Additional parameters setting per Port and Per System	The Host-CPU can configure additional parameters such as: LEDs parameters, port matrix, PoE Controller interrupt-out masks, flags, etc.
Port Matrix	Allows the layout designer to connect the physical ports to the logical ports whenever needed.
Software Download for Program Upgrading	Allows upgrading of the PoE mode software via download procedure in the field.

MAIN FUNCTIONAL SIGNALS DEXCRIPTION

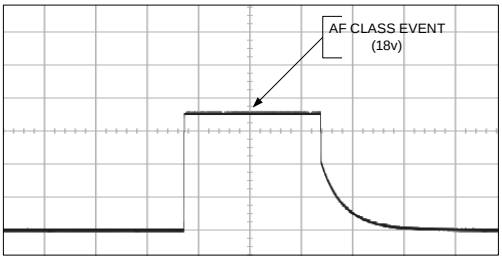
Detection Signal

Waveform of the PSE output when performing line detection procedure is shown below. The PoE device utilizes 4 voltage levels over the output port.



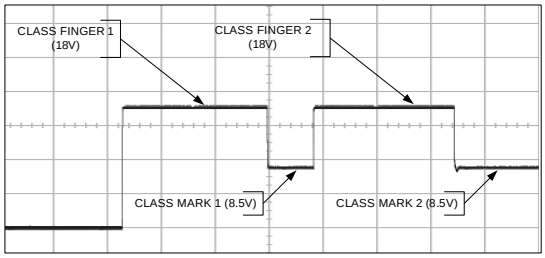
AF Class Signal

Waveform of the PSE output AF classification is shown below; Once the PD is recognized as a valid PoE PD, the classification voltage is applied, followed by full operating power.



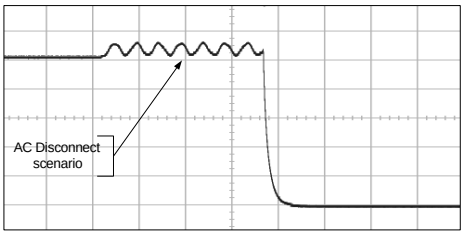
MCA Class Signal

Waveform of the PSE output MCA classification is shown below; Once the PD is recognized as a valid Type 2 PoE PD (high power PD), the classification event 1 voltage is applied (18v), followed by a mark 1 event voltage followed again by classification event and mark event.



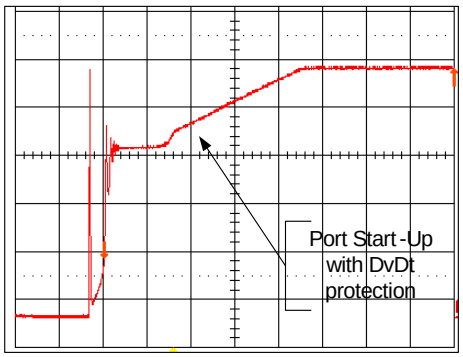
AC Disconnect

When a valid PD is connected to the port terminals, the AC signal amplitude sensed is as low as ~10 mVp-p. When the PD disconnects from the PSE terminals, the AC signal amplitude sensed rises. After several high pulses (300-400 ms), the port power shuts down.



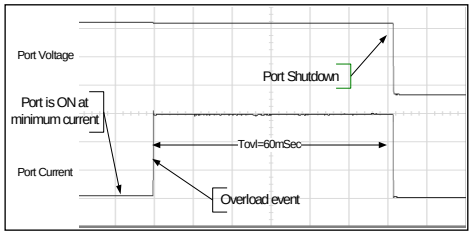
Start Up Event

After the detection and classification phases end, the PSE will apply the full operation voltage.



Overload Event

If port current in exceeds ICUT threshold for longer than Tovl, the PSE removes power from the PI as shown in the figure below.



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ABSOLUTE MAXIMUM RATINGS

V_{main} ..... -0.3 to 80 V(1)
DGND, AGND, QGND, SENSE_NEG ..... -0.3 to 0.3 V(2)

V_{PORT_POSx} ..... -0.3 to 80 V(1)
V_{PORT_NEGx}, REF_PORT_NEG ..... -8.4 to 80V(1)
V_{PORT_POSx} - V_{PORT_NEGx} ..... -0.3 to 80 V(1)

PORT_SENSEx ..... 7.2 to 25 V (1)
Gate_x ..... 0.3 to 18 V

VCC_{2p5}, ADC_{2p5} ..... 0.3 to 3 V
V_{PERI} ..... 4 V
EXT_REG ..... -0.3 to 6 V
I2CINI, ASICINI ..... -0.3 to 3 V
MISO, MOSI, SCK, SCL, SDA, CLK, RESETN, CS_N, INTERRUPT, POWER_BANK[2..0], LSD, LSC, LSL, SDA_OUT -0.3 to (V_{PERI} + 0.3) V

ESD (Human Body Model ..... -2 to 2 kV(3)
Max junction temperature (T_{junc}) ..... +150 °C
Junction-ambient thermal resistance (θ_{JA}) ..... 30 °C/W(4)

Junction-case thermal resistance (θ_{JC}) ..... 10° C/W
Lead temperature (soldering, 10 s) ..... 260° C
Storage temperature ..... -40 to +125 °C

Notes: "x" defines port numbers, 0 thru 3, inclusive.
(1) 80 V is the transient voltage that can be applied for 1 min max.
(2) Maximum value between grounds.
(3) ESD testing is performed in accordance with the Human Body Model (CZap = 100 pF, RZap = 1500 Ω).
(4) with 4ML PCB – no air flow

Stresses beyond those listed above, may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods, may affect device reliability.

OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating temperature At full load ambient	-40		+85	° C
Operational limitations (1)	15 to 44	44 to 55	55 to 57	V

(1) Operating functions depend on the input voltage, as shown in Figure 2.

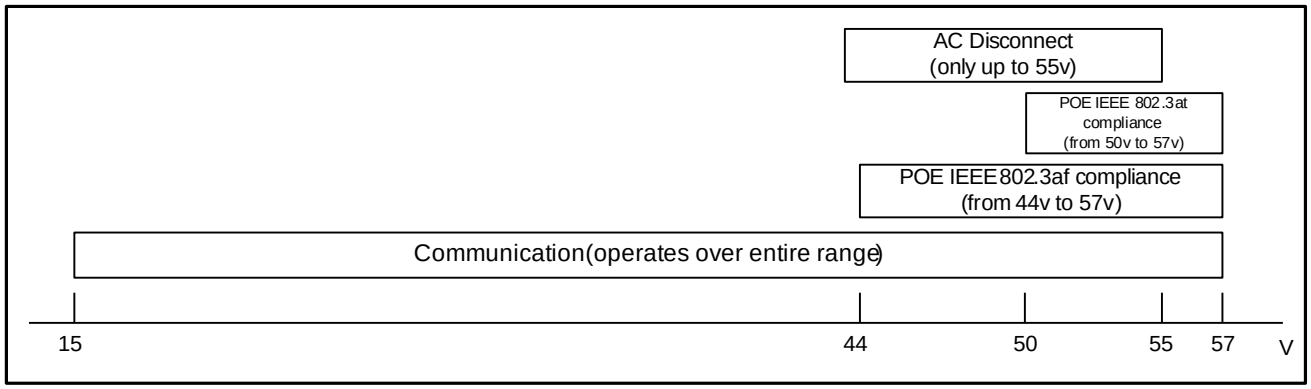

Figure 2: Operational Ranges

ELECTRICAL CHARACTERISTICS						
PIN NAME:	• **SCL** • **DISABLE_PORTS_N**					
PAD TYPE:	**Schmitt Trigger CMOS input, TTL Level with no internal Res.**					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage hysteresis		0.3			V	
Input High Current	I_{IH}	-1		1	µA	
Input Low Current	I_{IL}	-1		1	µA	

PIN NAME:	• **LSD Multiplexed with GPIO_2** • **LSC Multiplexed with GPIO_3** • **POWER_GOOD0 Multiplexed with GPIO_0** • **POWER_GOOD1 Multiplexed with GPIO_1** • **POWER_GOOD2 Multiplexed with GPIO_4**					
PAD TYPE:	**CMOS I/O, TTL Level with no internal pull up / pull down resistor, with Schmitt trigger Input**					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	

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Input Low Current	I_{IL}	-1		+1	µA	
High Level Output Voltage		VPERI-0.4V			V	Iout=-2 mA
Low Level Output Voltage				0.4	V	Iout=2 mA

PIN NAME:	• **SCK** • **CS_N** • **MOSI**					
PAD TYPE:	**CMOS I/O, TTL Level with internal pull up current source, with Schmitt trigger Input**					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	
Input Low Current	I_{IL}	-1		+1	µA	
High Level Output Voltage		VPERI-0.4 V			V	Iout = -2 mA
Low Level Output Voltage				0.4	V	Iout = 2 mA
Pull up current		10	20	50	uA	

PIN NAME:	• **MISO**					
PAD TYPE:	**CMOS I/O, TTL Level with internal pull up current source, with Schmitt trigger Input**					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	
Input Low Current	I_{IL}	-1		+1	µA	

High Level Output Voltage		VPERI-0.4V			V	Iout = -2 mA
Low Level Output Voltage				0.4	V	Iout = 2 mA
Pull down current		10	20	50	uA	

PIN NAME:	• **RESET_N** • **SDA** • **SDA_OUT Multiplexed with TEST_MODE**					
PAD TYPE:	**Digital I/O – input/output open drain** **CMOS Open Drain Output with Schmitt Trigger Input, TTL Level (external pull up res. Only))**					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Output Voltage	V_{OL}			0.4	V	Iout = 6 mA
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
OFF State Output Current		-1		+1	uA	

PIN NAME:	• **CS_EEPROM & LSL Multiplexed with INTERRUPT_N**					
PAD TYPE:	CMOS Open Drain Output (external pull up res. Only))					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Low Level Output Voltage				0.4	V	Iout = 6 mA
OFF State Output Current		-1		+1	uA	

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PIN NAME:	• VPORT_NEGx • REF_PORT_NEG					
PAD TYPE:	High Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Pin Current consumption		-10		+10	uA	Port driver OFF, Vport differential measurement OFF, AC generator OFF

PIN NAME:	• PORT_SENSEx					
PAD TYPE:	Low Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		0		0.5	V	With external 0.5 Ohms 2% to GND
Internal Current Consumption				20	uA	

PIN NAME:	• VPORT_POSx • VPORT_NEGx					
PAD TYPE:	High Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage (to GND)		0		62	V	

PIN NAME:	• VMAIN					
PAD TYPE:	High Voltage Supply Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		44		57	V	
VMAIN Current Consumption			13.6	16	mA	Total on VMAIN

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PIN NAME:	• CP_OUT					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Operating voltage		44		68	V	
Pin Internal Current Consumption				5	mA	

PIN NAME:	• CP_IN					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage		34		57	V	

PIN NAME:	• ADC2p5, VCC2p5, VPERI, EXT_REG					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
ADC2p5 Output Voltage		2.45		2.55	V	
ADC2p5 Internal Current Consumption				6	mA	Recommended external cap. = 47 nF to 135 nF
VCC2p5 Output Voltage		2.37		2.62	V	Recommended external cap. = 47 nF to 135 nF
VPERI Output Voltage		3.10		3.5	V	Recommended external cap. = 1 uF to 4.7 uF
VPERI External Current Load				6	mA	Without external NPN
EXT_REG Output Current				6	mA	

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PIN NAME:	• ASICINI, I2CINI (max. capacitance between mode input to GND should NOT exceed 1nF)					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage		0		ADC2p5	V	
Current Consumption		-1		+1	uA	

PIN NAME:	• IREF					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Output Voltage		1.21		1.34	V	With external 24.9 K resistor to GND

PIN NAME:	• FET_Gx					
PAD TYPE:	Analog					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Output voltage		11		14	V	

DYNAMIC CHARACTERISTICS

The PD69012 utilizes three programmable current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}). Loads that dissipate more than I_{cut} for longer than T_{cut} are classified as 'overloads' and are automatically shutdown. Loads that consume I_{lim} current for more than T_{lim} are shutdown and classified to be in short circuit state. If the PD69012 is configured to operate in DC-Disconnect mode and the output power is below I_{min} for more than $T_{min,}$ the PD is classified as 'no-load' and is shutdown. If the PD69012 is configured to operate in AC-Disconnect mode, then if the load's impedance is above a pre-defined impedance for more than $T_{min,}$ the PD is classified as 'no-load' and is shutdown

Automatic recovery from overload and no-load conditions is attempted every T_{OVLREC} and T_{UDLREC} periods (typically 5 and 1 seconds respectively). Output power is limited to $I_{lim,}$ which is a maximum peak current allowed at the port.

AF PORTS PARAMETERS

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown (can be modified through control port)		5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown (can be modified through control port)		1		s

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Cutoff timers accuracy	Typical accuracy of T_{cut}		4	2	0	ms
Inrush current	I_{Inrsh}	*For t=50 ms, C_{load}=180 uF max.*	400		450	mA
Output current operating range	I_{port}	*Continuous operation after startup period.*	10		I_{cut}	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		15.4	W
Off mode current	I_{min1}	Must disconnect for t greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over load current detection range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	T_{MPS}	DC modulation time for dc disconnect		49		ms
AC disconnect impedance	Zac		27	600	2000	KΩ

AT PORTS PARAMETERS

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown (can be modified through control port)			5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown (can be modified through control port)			1		s
Cutoff timers accuracy	Typical accuracy of T_{cut}		4	2	0	ms
Inrush current	I_{Inrsh}	*For t=50 ms, C_{load}=180 uF max.*	400		450	mA
Default output current operating range	I_{port}	*Continuous operation after startup period.*	10		I_{cut}	mA
Optional output current operating range	$I_{port\_optional}$	*Continuous operation after startup period*.*	10		$I_{cut\_optional}$	mA
Default output power available, operating range	P_{port}	Continuous operation after startup period, at port output @ V_{main} = 55V.	0.57		33	W
Optional output power available, operating range	$P_{port\_optional}$	Continuous operation after startup period, at port output @ V_{main} = 55V*	0.57		55	W
Off mode current	I_{min1}	Must disconnect for t greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Default over load current detection range	I_{cut}	Time limited to T_{OVL}	600		686	mA
Optional maximum over load current detection range	$I_{cut\_optional}$	Time limited to T_{OVL}*	1000		1140	mA

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Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	TMPS	DC modulation time for dc disconnect		49		ms
AC disconnect impedance	Zac		27	600	2000	KΩ

* To modify the default current threshold, registers' values should be modified

THERMAL DATA

Power Dissipation

The internal power consumption of a single device from the DC input is based on the following:

Input voltage range ..... 44 to 57 VDC
Input current ..... 13.6 mA typical; 16 mA max

$P_{main} = V_{main} \times I_{main}$

P_{main} typ. = 48 VDC x 13.6 mA = 0.652W.

P_{main} max. = 57 VDC x 16 mA = 0.912 W

The above data is considered with no external current consumption on Vperi (or with external NPN)

PROTECTION MECHANISM

The PD69012 has an internal thermal protection designed to protect against junction overheating. Two temperature sensors are integrated into the device: they are used for protection and for temperature monitoring.

Thermal protection mechanism protects the functionality of the device, in cases where over – temperature occurs.

Maximum temperature for ports operation = 155°C

Above this temperature the PD69012 will automatically shut down the ports to protect the device from overheating.

The PD69012 will turn-on the ports again after the temperature will decrease back to 130°C

An Interrupt signal will be generated from Interrupt_n pin when the measured temperature will reach the pre defined level in temperature alarm register.

Indicator Sensors

The temperature sensors monitor the local temperature inside the device. Their average temperature value is calculated by the PD69012. All values are stored in internal registers for data retrieval.

FUNCTIONAL PIN DESCRIPTION			
Pin	**Pin Name**	**Pin Type**	**Description**
0	**PAD**	Gnd	Exposed pad connected to underside of die
1	VPORT_POS0	Analog I/O	Port 0 positive input
2	VPORT_POS1	Analog I/O	Port 1 positive input
3	VPORT_POS2	Analog I/O	Port 2 positive input
4	VPORT_POS3	Analog I/O	Port 3 positive input
5	VPORT_POS4	Analog I/O	Port 4 positive input
6	VPORT_POS5	Analog I/O	Port 5 positive input
7	VPORT_POS6	Analog I/O	Port 6 positive input
8	VPORT_POS7	Analog I/O	Port 7 positive input
9	VPORT_POS8	Analog I/O	Port 8 positive input
10	VPORT_POS9	Analog I/O	Port 9 positive input
11	VPORT_POS10	Analog I/O	Port 10 positive input
12	VPORT_POS11	Analog I/O	Port 11 positive input
13	CP_OUT	Analog I/O	Charge Pump Output Pulse
14	CP_IN	Supply	Charge pump input
15	VMAIN	Supply	Main Voltage supply
16	REF_PORT_NEG	Analog I/O	Port negative reference
17	DGND2	GND	Digital ground
18	POWER_GOOD0 MULTIPLEXED WITH GPIO_0	Digital I/O	Power supply monitoring Multiplexed with General purpose I/O
19	POWER_GOOD1 MULTIPLEXED WITH GPIO_1	Digital I/O	Power supply monitoring Multiplexed with General purpose I/O
20	POWER_GOOD2 MULTIPLEXED WITH GPIO_4	Digital I/O	Power supply monitoring multiplexed with general purpose I/O
21	AGND1	GND	Analog ground
22	VPORT_NEG6	Analog I/O	Port 6 negative voltage feeding
23	PORT_SENSE6	Analog I/O	Channel current monitoring
24	FET_G6	Analog I/O	Port 6 – Gate control
25	FET_G7	Analog I/O	Port 7 – Gate control
26	PORT_SENSE7	Analog I/O	Channel current monitoring
27	VPORT_NEG7	Analog I/O	Port 7 negative voltage feeding
28	VPORT_NEG8	Analog I/O	Port 8 negative voltage feeding
29	PORT_SENSE8	Analog I/O	Channel current monitoring

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FUNCTIONAL PIN DESCRIPTION			
Pin	**Pin Name**	**Pin Type**	**Description**
30	FET_G8	Analog I/O	Port 8 – Gate control
31	FET_G9	Analog I/O	Port 9 – Gate control
32	PORT_SENSE9	Analog I/O	Channel current monitoring
33	VPORT_NEG9	Analog I/O	Port 9 negative voltage feeding
34	VPORT_NEG10	Analog I/O	Port 10 negative voltage feeding
35	PORT_SENSE10	Analog I/O	Channel current monitoring
36	FET_G10	Analog I/O	Port 10 – Gate control
37	FET_G11	Analog I/O	Port 11 – Gate control
38	PORT_SENSE11	Analog I/O	Channel current monitoring
39	VPORT_NEG11	Analog I/O	Port 11 negative voltage feeding
40	DGND1	GND	Digital ground
41	DISABLE_PORTS_N	Digital Input	Disable All Ports Power – active Low
42	CS_N	Digital I/O	SPI bus, Chip Select
43	MISO	Digital I/O	SPI bus, Master Data in/slave out
44	MOSI	Digital I/O	SPI bus, Master Data out/slave in
45	SCK	Digital I/O	SPI bus, Serial clock I/O
46	SCL	Digital Input	I²C bus, Serial Clock Input
47	SDA_OUT MULTIPLEXED WITH TEST_MODE	Digital I/O	Third pin in I²C protocol Test Mode Pin – Must be tied to VPERI with pull-up resistor if not used
48	SDA	Digital I/O	I²C bus, open drain
49	RESET_N	Digital I/O	Active Low Reset I/O
50	IREF	Analog I/O	Current reference
51	ASICINI	Analog Input	Analog input for chip initialization
52	VCC2P5	Internal Regulator	Internal 2.5v source – not to be used for external devices
53	I2CINI	Analog Input	Analog input for I²C initialization
54	QGND	GND	Quiet analog ground
55	ADC2P5	Internal reference	ADC reference – not to be used for external devices
56	EXT_REG	Analog Out	External regulation
57	VPERI	Analog Out	Regulated 3.3v output voltage source for external devices
58	CS_EEPROM_N & LSL MULTIPLEXED WITH INTERRUPT_N	Digital Output Open drain	SPI bus, EEPROM Chip Select & LED Stream Latch (if set) Multiplexed with interrupt out

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FUNCTIONAL PIN DESCRIPTION			
Pin	**Pin Name**	**Pin Type**	**Description**
59	LSD MULTIPLEXED WITH GPIO_2	Digital I/O	LED Stream Data – data out Multiplexed with General purpose I/O
60	LSC MULTIPLEXED WITH GPIO_3	Digital I/O	Led Stream CLK– CLK out Multiplexed with General purpose I/O
61	SENSE_NEG	Analog I/O	Port sense reference
62	AGND2	GND	Analog ground
63	VPORT_NEG0	Analog I/O	Port 0 negative voltage feeding
64	PORT_SENSE0	Analog I/O	Channel current monitoring
65	FET_G0	Analog I/O	Port 0 – Gate control
66	FET_G1	Analog I/O	Port 1 – Gate control
67	PORT_SENSE1	Analog I/O	Channel current monitoring
68	VPORT_NEG1	Analog I/O	Port 1 negative voltage feeding
69	VPORT_NEG2	Analog I/O	Port 2 negative voltage feeding
70	PORT_SENSE2	Analog I/O	Channel current monitoring
71	FET_G2	Analog I/O	Port 2 – Gate control
72	FET_G3	Analog I/O	Port 3 – Gate control
73	PORT_SENSE3	Analog I/O	Channel current monitoring
74	VPORT_NEG3	Analog I/O	Port 3 negative voltage feeding
75	VPORT_NEG4	Analog I/O	Port 4 negative voltage feeding
76	PORT_SENSE4	Analog I/O	Channel current monitoring
77	FET_G4	Analog I/O	Port 4 – Gate control
78	FET_G5	Analog I/O	Port 5 – Gate control
79	PORT_SENSE5	Analog I/O	Channel current monitoring
80	VPORT_NEG5	Analog I/O	Port 5 negative voltage feeding

CONFIGURATION PINS

There are two main configuration pins (see Figure 3) utilized in the PD69012, these pins configure the operation mode of the chip and the communication addresses (SPI and I^2C)

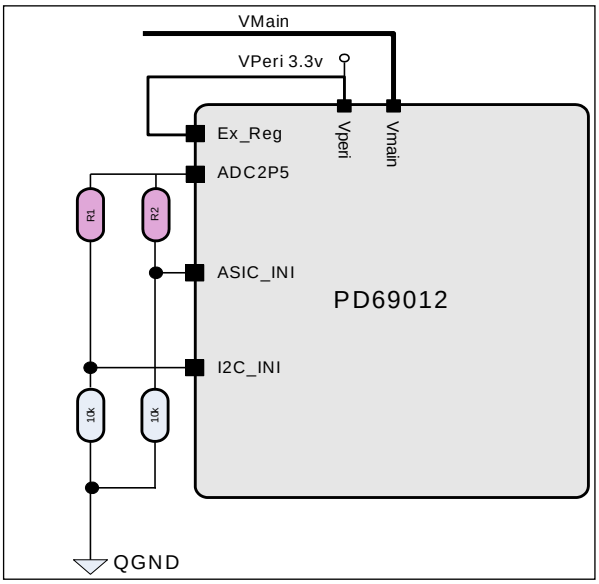

Figure 3: Electronic Connection of Configuration Pins

ASIC_INI

PoE Device's configuration is performed via the ASIC_INI pin, as shown in the following table. The ASIC_INI analog signal is converted into a 10-bit register (A/D). Once a hard Reset pulse is detected, the data is latched into an internal mode register.

Step	Min Voltage	Max Voltage	Mode	E-SPI Address (B2-B0)	Description
0	0	0.14	Master	000	Stand Alone Master Mode configuration – power management master
1	0.19	0.29	Slave0	000	Set the E-SPI address in Stand Alone Slave & macro Modes
2	0.35	0.44	Slave1	001	Set the E-SPI address in Stand Alone Slave & macro Modes
3	0.51	0.6	Slave2	010	Set the E-SPI address in Stand Alone Slave & macro Modes
4	0.67	0.75	Slave3	011	Set the E-SPI address in Stand Alone Slave & macro Modes
5	0.83	0.9	Slave4	100	Set the E-SPI address in Stand Alone Slave & macro Modes
6	0.99	1.06	Slave5	101	Set the E-SPI address in Stand Alone Slave & macro Modes
7	1.15	1.21	Slave6	110	Set the E-SPI address in Stand Alone Slave & macro Modes
8	1.3	1.36	Slave7	111	Set the E-SPI address in Stand Alone Slave & macro Modes
9-15	2.35	2.5	Manual	000	Internal use only – debug mode

Notes:

In the Auto mode – the PD69012 communicates with the Host via the I^2C bus.
In the other modes – the PD69012 is communicates with the controller via the ESPI bus or I^2C

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I2C_Address

A standard I2C interface is used to communicate between the PD69012 and the Host controller in Auto Mode, with a bit-rate of up to 400 kb/s. The I^2C address is based on 7 bits and is a combination of the I2C_INI and ASIC_INI pins as shown in the below tables:

The I^2C address is created by the following register:

MSB LSB

4 bit based on I^2C INIT Voltage Level				3 bit based on ASIC INI Voltage Level		
A4	A3	A2	A1	B2	B1	B0

ASIC_INI Voltage Level	B2, B1, B0
0 to 15 according to ASIC_INI table	ESPI address

I^2C Address Step	I2C_INI Voltage Level (Volt)		I2C_INI Internal Register (A4-A1)	Notes
	MIN	MAX		
0	0	0.14	0000	General call address – Should not be used
1	0.19	0.29	0001	
2	0.35	0.44	0010	
3	0.51	0.6	0011	
4	0.67	0.75	0100	
5	0.83	0.9	0101	
6	0.99	1.06	0110	
7	1.15	1.21	0111	
8	1.3	1.36	1000	
9	1.46	1.51	1001	
10	1.62	1.67	1010	
11	1.78	1.82	1011	
12	1.94	1.97	1100	
13	2.05	2.13	1101	
14	2.25	2.28	1110	
15	2.35	2.5	1111	

BLOCK DIAGRAM

The PD69012 PoE Manager (see Figure 4) complies with all the IEEE standard 802.3at detection requirements. The PD69012 is built around two major sections:

1. A common Digital section that serves all 12 channels
2. Eight separate identical channels for driving ports

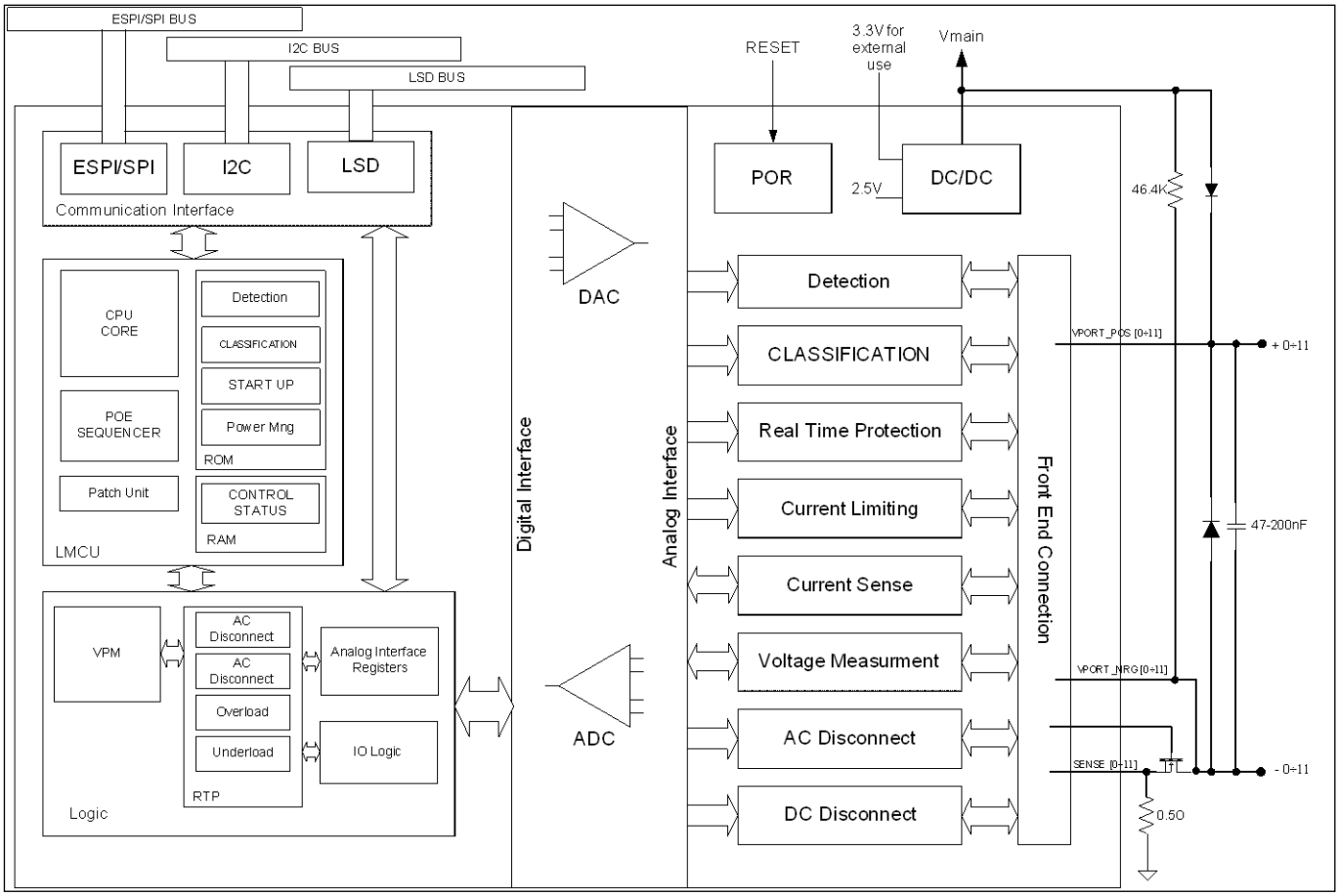

Figure 4: PoE Manager – Block Diagram

Communication I/O

The PD69012 incorporates two communication interfaces. The first interface is an SPI bus which connects the PD69012 devices to each other, or to the external Controller. The second interface is an I^2C utilized to communicate with Host. .
Both interfaces send the contents of the internal registers between the PD69012 logic and the PoE Controller.
LEDs indication circuit is supported by using the LED Stream Data bus (LSD).

Power Management

Receives data from the PoE sequencer and distribute total power to all relevant ports according to priority levels, depending on the system's total power.

Detection

The PoE Controller or the PoE sequencer generates a request to apply separate voltage levels to the output port. A measurement circuit monitors the difference between the various levels.
Voltage differences are compared with values stored in the registers. By comparing these values, the system can determine whether to enable a port or not.

Classification

Upon request from the PoE Controller or from the PoE sequencer, the state machine applies a regulated Class Event and Mark Event voltages to the ports as required by the IEEE standard.
The current is measured by comparing the real current flow with a number of preset thresholds; in this manner the class is verified.

Overload

This block senses when port current exceeds the maximum current level as specified in the IEEE-802.3at standard, and disconnects the port if required.

AC Disconnect

The system applies a sinusoidal signal to the positive port terminal. The voltage developed on the port terminals is proportional to the load's value. If the load is high, the AC component riding on the port terminals is low. If the load is low, the AC component is high. A dedicated circuit measures the AC component level and compares it with a pre-defined value stored in a register. Based on the comparison's results, the system determines whether to disable a port or not.

DC Disconnect

This block senses when the port current drops below 7.5 mA. If this is the case, timers in the Channel RT Controller start counting. The Channel RT Controller acts in accordance with pre-programmed thresholds limits and time windows, prior to initiating a disconnect status for that port. The circuitry takes into account PDs that modulate their current consumption, disconnecting them only if necessary.

Power on Reset (POR)

The POR Monitors the internal DC levels; if these voltages drop below specific thresholds, a Reset signal is generated and the PD690012s are reset via the RESET_N pin.

DC/DC Circuit

This circuit produces 2.5V and 3.3v, derived from the main supply.

Real Time Protection

This circuitry performs all real time measurements and sends the results to the logic circuitry in order to determine whether to disconnect a port or not.

Current Limit

This circuit continuously monitors the current of powered ports and limits the current to a specific value in cases where an over load occurs. If the current exceeds a specific level, the system starts measuring the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.

LMCU controller

The LMCU has an integrated CPU, RAM and ROM memories. Certain major functions are managed by the LMCU core running the SW from the ROM.

TYPICAL APPLICATION

The PD69012 may be integrated into a number of applications such as daughter boards, Ethernet switches or routers. Examples of such applications are described below:

Integrated directly into a switch – facilitates entire PoE concept, by including the IC(s) on the main switch's PCB.

Daughter board add-on – in which the IC is integrated into a small PCB dedicated for PoE, mounted on top of the switch's main PCB or in the DIMM module

Integrated into an RJ45 connector – saving space on the main board and creating small differences between the PoE and non-PoE versions of a switch

Midspans – stand alone devices, installed between the Ethernet switch and PDs (Powered Devices) such as telephone, camera, wireless LAN, etc.

These Midspans include the PD69012 IC as a PoE control element, destined to inject power over the communication lines.

Figure 5 and Figure 6 provide an example of basic applications of the PD69012 in an AC Disconnect Mode and the DC Disconnect Mode:

The PD69008 can be integrated into a number of applications such as daughter boards, Ethernet switches or routers. Examples of such applications are described below:

Integrated directly into a switch: Facilitates entire PoE concept by including the IC(s) on the main switch's PCB.

Daughter board add-on: The IC is integrated into a small dedicated PoE PCB, mounted on top of the switch's main PCB or into a DIMM module.

Integrated into an RJ45 connector: Saves space on the main board and creates small differences between the PoE and non-PoE versions of a switch.

Midspans: Stand-alone devices, installed between the Ethernet switch and the PDs (Powered Devices) such as telephones, cameras, wireless LANs, etc.

These Midspans include the PD69008 IC as a PoE control element, destined to inject power over the communication lines

Figure 5 and Figure 6 provide examples of basic applications of the PD69008 in an AC Disconnect Mode and the DC Disconnect Mode:

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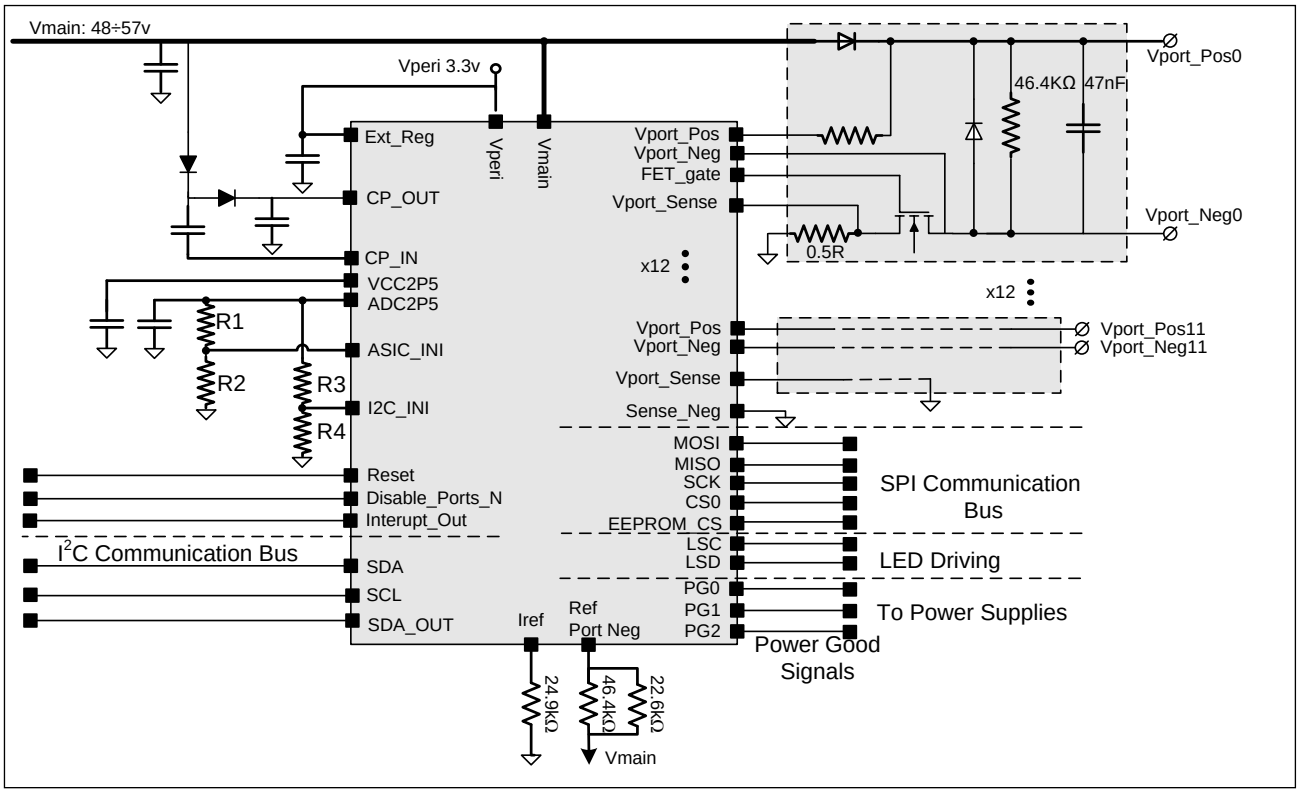

Figure 5: Basic Application with AC Disconnect Support

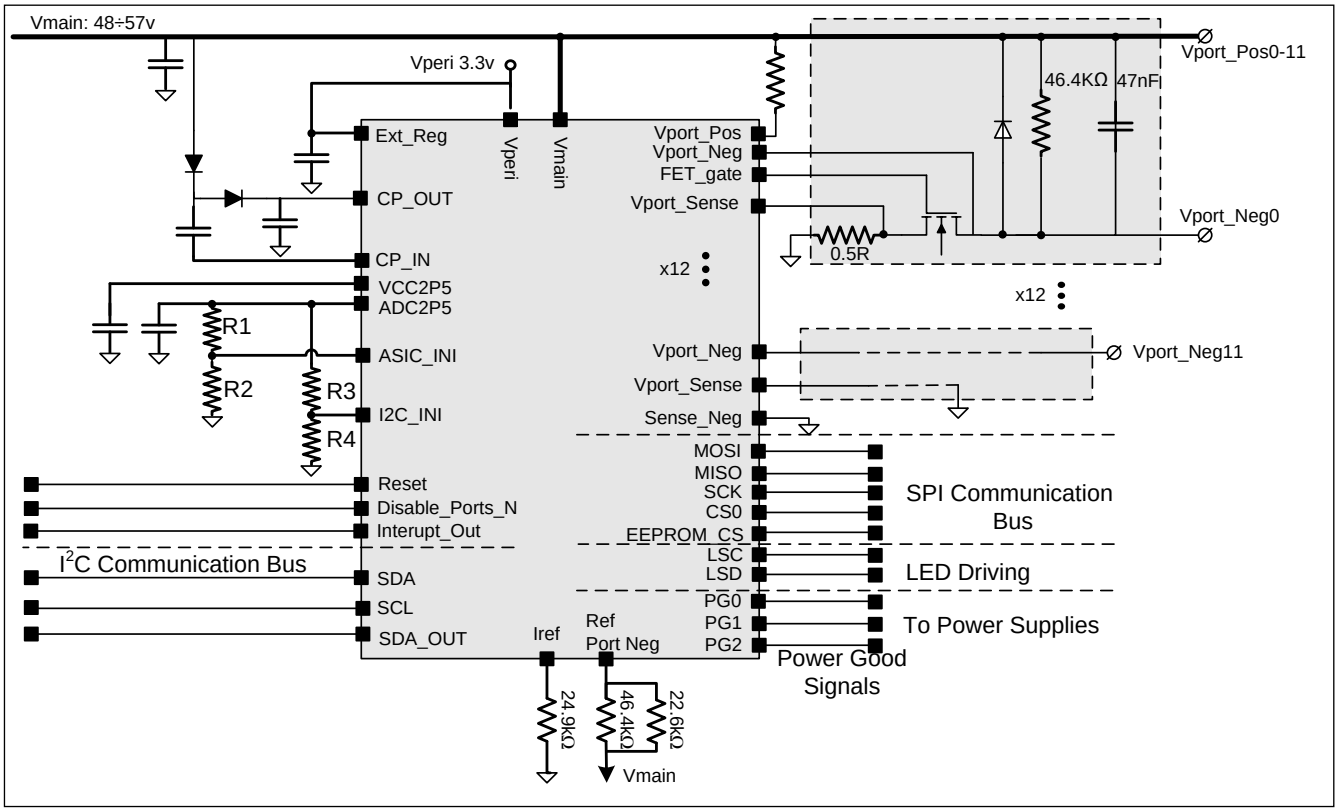

Figure 6: Basic Application with DC Disconnect Support

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 15 June 2008	-	Initial Preliminary Release
0.2 / 31 July 2008	-	Update Features List Add Operational Ranges figure Update Electrical Characteristics Update ports Parameters Update Basic Application Diagrams
0.3 / 22 January 2009	p1	Ordering info-modified
0.4 / 05 May 2009	Whole document	Added update for default current limit
0.4 / 27 Jul 2010		Changing catalog numbers metrology
0.5 / 14 Oct 2010	-	Update FET_Gx limits
1.0 / 18 Nov 2010	Whole document	Changing template
1.1 / 31-Jan-2011		Rotating package pin out figure
1.11 / 22 Ocvtober 2015		Updating footer

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