RE46C191

CMOS Low-Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode

Features

- Two AA Battery Operation
- Low Quiescent Current Consumption
- Local Alarm Memory
- Interconnect Up to 40 Detectors
- Nine-Minute Timer for Sensitivity Control
- Temporal or Continuous Horn Pattern
- Internal Low Battery and Chamber Test
- All Internal Oscillator
- Internal Infrared Emitter Diode (IRED) Driver
- Adjustable IRED Drive Current
- Adjustable Hush Sensitivity
- Two Percent Low Battery Set Point
- Pin-for-Pin Compatible with RE46C190

General Description

The RE46C191 is a low-power, low-voltage CMOS photoelectric-type smoke detector IC. With minimal external components, this circuit provides all the required features for a photoelectric-type smoke detector.

The design incorporates a gain-selectable photo amplifier for use with an infrared emitter/detector pair.

To keep the standby current to a minimum, an internal oscillator strobes power to the smoke detection circuitry every 10 seconds. If smoke is sensed, the detection rate is increased to verify an Alarm condition. A High-Gain mode is available for push button chamber testing.

A check for a Low Battery condition is performed every 86 seconds and the chamber integrity is tested once every 43 seconds when in Standby mode. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

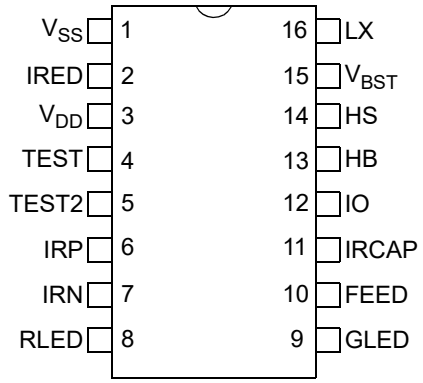
An interconnect pin allows multiple detectors to be connected, such that when one unit alarms, all units will sound.

An internal nine-minute timer can be used for a Reduced Sensitivity mode.

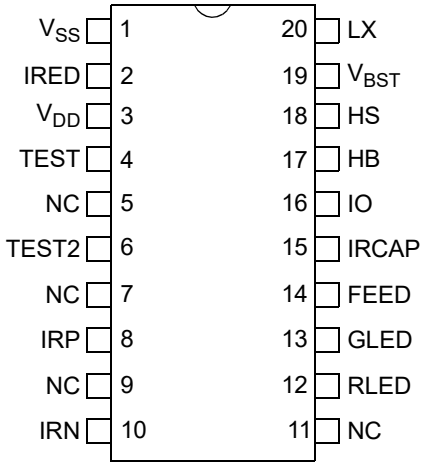
Utilizing low-power CMOS technology, the RE46C191 is designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217.

Package Types

RE46C191
SOIC

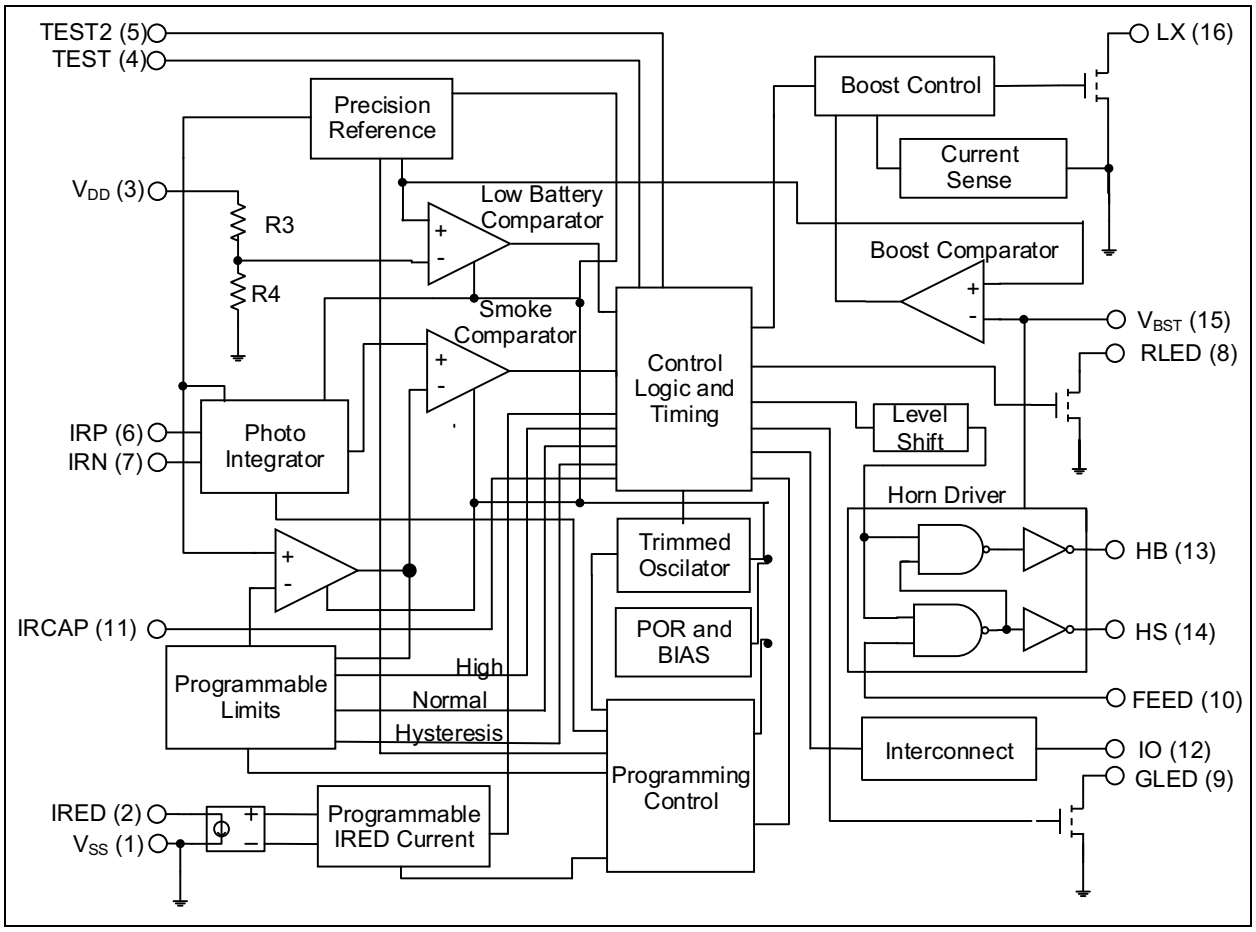


RE46C191
SSOP

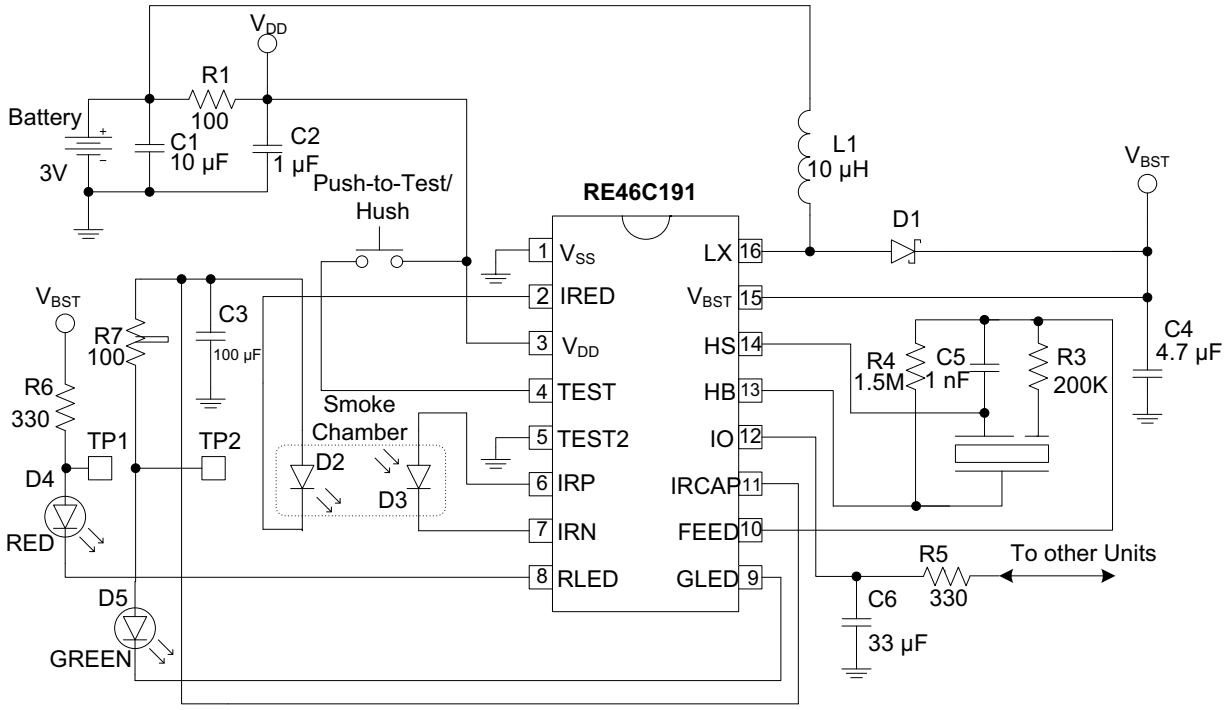


Note: See Table 2-1 for pin descriptions.

TYPICAL BLOCK DIAGRAM



TYPICAL BATTERY APPLICATION



Note 1: C2 must be located as close as possible to the device power pins. C1 must be located closest to V_{SS}.

2: R3, R4 and C5 are typical values, and may be adjusted to maximize sound pressure.

3: DC-DC converter in High Boost mode (nominal V_{BST} = 9.6V) can draw current pulses of greater than 1A and is very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to the LX pin and from the V_{SS} pin to the battery. To function properly under full load at V_{DD} = 2V, the total of the inductor and interconnect resistances must not exceed 0.3Ω. The internal battery resistance must not be more than 0.5Ω, and a low ESR capacitor of 10 µF or more should be connected in parallel with the battery to average the current draw over the boost converter cycle.

4: Schottky diode D1 must have a maximum peak current rating of at least 1.5A. For best results, it must have a forward voltage specification of less than 0.5V at 1A and low reverse leakage.

5: Inductor L1 must have a maximum peak current rating of at least 1.5A.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... V_{DD} = 5.5V; V_{BST} = 13V
Input Voltage Range Except FEED and TEST ..... V_{IN} = -0.3V to V_{DD} + 0.3V
FEED Input Voltage Range ..... V_{INFD} = -10V to +22V
TEST Input Voltage Range .... V_{INTEST} = -0.3V to V_{BST} + 0.3V
LX Voltage ..... V_{LX} = -0.3V to 13V
Maximum IRCAP Voltage ..... V_{IRCAP} = 5.5V
Input Current Except FEED ..... I_{IN} = 10 mA
Continuous Operating Current (HS, HB and V_{BST}) ..... I_O = 40 mA
Continuous Operating Current (IRED) ..... I_{OIR} = 300 mA
Storage Temperature ..... T_{STG} = -55°C to +125°C
ESD Human Body Model ..... V_{HBM} = 2 kV
ESD Machine Model ..... V_{MM} = 175V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10°C to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(1,2,3)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	V_{DD}	2.0	—	5.0	V	Operating
Supply Current	I_{DD1}	V_{DD}	—	1	2	µA	Standby, inputs low, no loads, boost off, no smoke check
Standby Boost Current	I_{BST1}	V_{BST}	—	100	—	nA	Standby, inputs low, no loads, boost off, no smoke check
IRCAP Supply Current	I_{IRCAP}	IRCAP	—	500	—	µA	During smoke check
Boost Voltage	V_{BST1}	V_{BST}	3.0	3.6	4.2	V	IRCAP charging for smoke check, GLED operation, I_{OUT} = 40 mA
	V_{BST2}	V_{BST}	8.5	9.6	10.7	V	No local alarm, RLED operation, I_{OUT} = 40 mA, IO as an input
Input Leakage	I_{INOP}	IRP	-200	—	200	pA	IRP = V_{DD} or V_{SS}
		IRN	-200	—	200	pA	IRN = V_{DD} or V_{SS}
	I_{IHF}	FEED	—	20	50	µA	FEED = 22V, V_{BST} = 9V
	I_{ILF}	FEED	-50	-15	—	µA	FEED = -10V, V_{BST} = 10.7V
Input Voltage Low	V_{IL1}	FEED	—	—	2.7	V	FEED, V_{BST} = 9V
	V_{IL2}	IO	—	—	800	mV	No local alarm, IO as an input

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10°C to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(1,2,3)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Input Voltage High	V_{IH1}	FEED	6.2	—	—	V	FEED, V_{BST} = 9V
	V_{IH2}	IO	2.0	—	—	V	No local alarm, IO as an input
IO Hysteresis	V_{HYST1}	IO	—	150	—	mV	
Input Pull-Down Current	I_{PD1}	TEST, TEST2	3	10	30	µA	V_{IN} = V_{DD}
	I_{PDIO1}	IO	20	—	80	µA	V_{IN} = V_{DD}
	I_{PDIO2}	IO	—	—	140	µA	V_{IN} = 15V
Output Voltage Low	V_{OL1}	HB, HS	—	—	500	mV	I_{OL} = 16 mA, V_{BST} = 9V
	V_{OL2}	RLED	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 9V
	V_{OL3}	GLED	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 3.6V
Output High Voltage	V_{OH1}	HB, HS	8.5	—	—	V	I_{OL} = 16 mA, V_{BST} = 9V
Output Current	I_{IOH1}	IO	-4	-5	—	mA	Alarm, V_{IO} = 3V or V_{IO} = 0V, V_{BST} = 9V
	I_{IODMP}	IO	5	15	—	mA	At conclusion of local alarm or test, V_{IO} = 1V
	I_{IRED50}	IRED	45	50	55	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (50 mA option selected, T_A = +27°C)
	$I_{IRED100}$	IRED	90	100	110	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (100 mA option selected, T_A = +27°C)
	$I_{IRED150}$	IRED	135	150	165	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (150 mA option selected, T_A = +27°C)
	$I_{IRED200}$	IRED	180	200	220	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (200 mA option selected, T_A = +27°C)
IRED Current Temperature Coefficient	TC_{IRED}	—	—	0.5	—	%/°C	V_{BST} = 5V, IRCAP = 5V **(Note 4)**

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10°C to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(1,2,3)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Low Battery Alarm Voltage	V_{LB1}	V_{DD}	2.05	2.1	2.15	V	Falling edge, 2.1V nominal selected
	V_{LB2}	V_{DD}	2.15	2.2	2.25	V	Falling edge, 2.2V nominal selected
	V_{LB3}	V_{DD}	2.25	2.3	2.35	V	Falling edge, 2.3V nominal selected
	V_{LB4}	V_{DD}	2.35	2.4	2.45	V	Falling edge, 2.4V nominal selected
	V_{LB5}	V_{DD}	2.45	2.5	2.55	V	Falling edge, 2.5V nominal selected
	V_{LB6}	V_{DD}	2.55	2.6	2.65	V	Falling edge, 2.6V nominal selected
	V_{LB7}	V_{DD}	2.65	2.7	2.75	V	Falling edge, 2.7V nominal selected
	V_{LB8}	V_{DD}	2.75	2.8	2.85	V	Falling edge, 2.8V nominal selected
Low Battery Hysteresis	V_{LBHYST}	V_{DD}	—	100	—	mV	
IRCAP Turn-On Voltage	V_{TIR1}	IRCAP	3.6	4.0	4.4	V	Falling edge, V_{BST} = 5V, I_{OUT} = 20 mA
IRCAP Turn-Off Voltage	V_{TIR2}	IRCAP	4.0	4.4	4.8	V	Rising edge, V_{BST} = 5V, I_{OUT} = 20 mA

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

AC ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) **(Notes 1 through 4)**.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Time Base							
Internal Clock Period	T_{PCLK}	—	9.80	10.4	11.0	ms	PROGSET, IO = High
RLED Indicator							
On Time	T_{ON1}	RLED	9.80	10.4	11.0	ms	Operating
Standby Period	T_{PLED1}	RLED	320	344	368	s	Standby, no alarm
Local Alarm Period	T_{PLED2A}	RLED	470	500	530	ms	Local Alarm condition with temporal horn pattern
	T_{PLED2B}	RLED	625	667	710	ms	Local Alarm condition with continuous horn pattern
Hush Timer Period	T_{PLED4}	RLED	10	10.7	11.4	s	Timer mode, no local alarm
External Alarm Period	T_{PLED0}	RLED	LED IS NOT ON			s	Remote alarm only
GLED Indicator							
On Time	T_{ON2}	GLED	9.8	10.4	11.0	ms	Operating
Latched Alarm Period	T_{PLED3}	GLED	40	43	46	s	Latched Alarm condition, LED enabled
Latched Alarm Pulse Train (3x) Off Time	T_{OFLED}	GLED	1.25	1.33	1.41	s	Latched Alarm condition, LED enabled
Latched Alarm LED Enabled Duration	T_{LALED}	GLED	22.4	23.9	25.3	Hours	Latched Alarm condition, LED enabled
Smoke Check							
Smoke Test Period with Temporal Horn Pattern	T_{PER0A}	IRED	10	10.7	11.4	s	Standby, no alarm
	T_{PER1A}	IRED	1.88	2.0	2.12	s	Standby (after one valid smoke sample)
	T_{PER2A}	IRED	0.94	1.0	1.06	s	Standby (after two consecutive valid smoke samples)
	T_{PER3A}	IRED	0.94	1.0	1.06	s	Local alarm (after three consecutive valid smoke samples)
	T_{PER4A}	IRED	235	250	265	ms	Push button test, >1 chamber detections
			313	333	353	ms	Push button test, no chamber detections
	T_{PER5A}	IRED	7.5	8.0	8.5	s	In remote alarm

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested and are based on characterization data.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) **(Notes 1 through 4)**.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Smoke Test Period with Continuous Horn Pattern	T_{PER0B}	IRED	10	10.7	11.4	s	Standby, no alarm
	T_{PER1B}	IRED	2.5	2.7	2.9	s	Standby (after one valid smoke sample)
	T_{PER2B}	IRED	1.25	1.33	1.41	s	Standby (after two consecutive valid smoke samples)
	T_{PER3B}	IRED	1.25	1.33	1.41	s	Local alarm (after three consecutive valid smoke samples)
	T_{PER4B}	IRED	313	333	353	ms	Push button test
	T_{PER5B}	IRED	10	10.7	11.4	s	In remote alarm
Chamber Test Period	T_{PCT1}	IRED	40	43	46	s	Standby, no alarm
Long-Term Drift Sample Period	T_{LTD}	IRED	400	430	460	s	Standby, no alarm, long-term drift enabled
Low Battery							
Low Battery Sample Period	T_{PLB1}	V_{DD}	320	344	368	s	RLED on
	T_{PLB2}	V_{DD}	80	86	92	s	RLED off
Horn Operation							
Low Battery Horn Period	T_{HPER1}	HB	40	43	46	s	Low battery, no alarm
Chamber Fail Horn Period	T_{HPER2}	HB	40	43	46	s	Chamber failure
Low Battery Horn On Time	T_{HON1}	HB	9.8	10.4	11.0	ms	Low battery, no alarm
Chamber Fail Horn On Time	T_{HON2}	HB	9.8	10.4	11.0	ms	Chamber failure
Chamber Fail Off Time	T_{HOF1}	HB	305	325	345	ms	Failed chamber, no alarm, 3x chirp
Alarm On Time with Temporal Horn Pattern	T_{HON2A}	HB	470	500	530	ms	Local or remote alarm **(Note 1)**
Alarm Off Time with Temporal Horn Pattern	T_{HOF2A}	HB	470	500	530	ms	Local or remote alarm **(Note 1)**
	T_{HOF3A}	HB	1.4	1.5	1.6	s	Local or remote alarm **(Note 1)**
Alarm On Time with Continuous Horn Pattern	T_{HON2B}	HB	235	250	265	ms	Local or remote alarm **(Note 1)**
Alarm Off Time with Continuous Horn Pattern	T_{HOF2B}	HB	78	83	88	ms	Local or remote alarm **(Note 1)**

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested and are based on characterization data.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) **(Notes 1 through 4)**.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Push-to-Test (PTT) Alarm Memory On Time	T_{HON4}	HB	9.8	10.4	11.0	ms	Alarm memory active, PTT
PTT Alarm Memory Horn Period	T_{HPER4}	HB	235	250	265	ms	Alarm memory active, PTT
Interconnect Signal Operation (IO)							
IO Active Delay	T_{IODLY1}	IO	—	0	—	s	From start of local alarm to IO active
Remote Alarm Delay with Temporal Horn Pattern	$T_{IODLY2A}$	IO	0.780	1.00	1.25	s	No local alarm, from IO active to alarm
Remote Alarm Delay with Continuous Horn Pattern	$T_{IODLY2B}$	IO	380	572	785	ms	No local alarm, from IO active to alarm
IO Charge Dump Duration	T_{IODMP}	IO	1.23	1.31	1.39	s	At conclusion of local alarm or test
IO Filter	T_{IOFILT}	IO	—	—	313	ms	Standby, no alarm
Hush Timer Operation							
Hush Timer Period	T_{TPER}	—	8.0	8.6	9.1	Min	No alarm
Low Battery Hush Timer Period	T_{TPERLB}	—	7.73	8.22	8.71	Hours	No alarm
EOL							
End-of-Life Age Sample	T_{EOL}	—	314	334	354	Hours	EOL enabled, standby
Detection							
IRED On Time	T_{IRON}	IRED	—	100	—	µs	Prog Bits 32,33 = 1,1
		IRED	—	200	—	µs	Prog Bits 32,33 = 0,1
		IRED	—	300	—	µs	Prog Bits 32,33 = 1,0
		IRED	—	400	—	µs	Prog Bits 32,33 = 0,0

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested and are based on characterization data.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: All limits specified for V_{DD} = 3V, V_{BST} = 4.2V and V_{SS} = 0V, except where noted in the Electrical Characteristics.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-10	—	+60	°C	
Storage Temperature Range	T_{STG}	-55	—	+125	°C	
Thermal Package Resistances						
Thermal Resistance, 16-Lead SOIC (150 mil.)	θ_{JA}	—	86.1	—	°C/W	

NOTES:

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

RE46C191 SOIC	RE46C191 SSOP	Symbol	Function
1	1	V_{SS}	Connects to the negative supply voltage.
2	2	IRED	Provides a regulated and programmable pulsed current for the infrared emitter diode.
3	3	V_{DD}	Connects to the positive supply or battery voltage.
4	4	TEST	This input is used to invoke Test modes and the Timer mode. This input has an internal pull-down.
5	6	TEST2	Test input for Test and Programming modes. This input has an internal pull-down.
6	8	IRP	Connects to the anode of the photo diode.
7	10	IRN	Connects to the cathode of the photo diode.
8	12	RLED	An open-drain NMOS output used to drive a visible LED. This pin provides load current for the low battery test and is a visual indicator for Alarm and Hush modes.
9	13	GLED	An open-drain NMOS output used to drive a visible LED to provide visual indication of an Alarm Memory condition.
10	14	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to V_{DD} or V_{SS}.
11	15	IRCAP	Used to charge and monitor the IRED capacitor.
12	16	IO	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull-down device and a charge dump device.
13	17	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
14	18	HS	This pin is a complementary output to HB. It is connected to the ceramic electrode of the piezoelectric transducer.
15	19	V_{BST}	Boosted voltage produced by DC-DC converter.
16	20	LX	An open-drain NMOS output used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low-resistance path.
—	5, 7, 9, 11	NC	Not connected.

NOTES:

3.0 DETAILED DESCRIPTION

3.1 Standby Internal Timing

The internal oscillator is trimmed to ±6% tolerance. Once every ten seconds, the boost converter is powered up, the IRCAP is charged from V_{BST} and the detection circuitry is active for 3 ms. Prior to completion of the 3 ms period, the IRED pulse is active for a user-programmable duration of 100-400 µs. During this IRED pulse, the photo diode current is integrated and then digitized. The result is compared to a limit value stored in EEPROM during calibration to determine the photo chamber status. If a Smoke condition is present, the period to the next detection decreases and additional checks are made.

3.2 Smoke Detection Circuitry

The digitized photo amplifier integrator output is compared to the stored limit value at the conclusion of the IRED pulse period. The IRED drive is all internal, and both the period and current are user programmable. Three consecutive smoke detections will cause the device to go into Alarm mode, and activate the horn and interconnect circuits. In Alarm mode, the horn is driven at the high boost voltage level, which is regulated based on an internal voltage reference, and results in consistent audibility over battery life. RLED will turn on for 10 ms at a 2 Hz rate. In Local Alarm mode, the integration limit is internally decreased to provide alarm hysteresis. The integrator has three separate gain settings:

- Normal and Hysteresis
- Reduced Sensitivity (Hush)
- High Gain for Chamber Test and PTT

There are four separate sets of alarm limits, which are all user programmable:

- Normal Detection
- Hysteresis
- Hush
- Chamber Test and PTT Modes

In addition, there are user-selectable integrator gain settings to optimize detection levels (see Table 4-1).

3.3 Supervisory Tests

Once every 86 seconds, the status of the battery voltage is checked by enabling the boost converter for 10 ms and comparing a fraction of the V_{DD} voltage to an internal reference. In each period of 344 seconds, the battery voltage is checked four times. Three checks are unloaded and one check is performed with the RLED enabled, which provides a battery load. The High Boost mode is active only for the loaded low battery test. If the low battery test fails, the horn will pulse on for 10 ms every 43 seconds and will continue to pulse until the failing condition passes.

As an option, a Low Battery Silence mode can be invoked. If a Low Battery condition exists and the TEST input is driven high, the RLED will turn on. If the TEST input is held for more than 0.5 seconds, the unit enters the PTT operation described in **Section 3.4 "Push-to-Test Operation (PTT)"**. After the TEST input is driven low, the unit enters the Low Battery Hush mode and the 10 ms horn pulse is silenced for eight hours. The activation of the test button will also initiate the nine-minute Reduced Sensitivity mode described in **Section 3.6 "Reduced Sensitivity Mode"**. After eight hours, the audible indication will resume if the Low Battery condition still exists.

Once every 43 seconds, the chamber test is activated and the High Gain mode with chamber test limits is internally selected. The chamber is checked by amplifying background reflections. The Low Boost mode is used for the chamber test.

If two consecutive chamber tests fail, the horn will pulse on for 10 ms three times, with the pulses separated by 330 ms every 43 seconds. The horn will continue to pulse until the failing condition passes.

Each of the two supervisory test audible indicators is separated by approximately 20 seconds.

3.4 Push-to-Test Operation (PTT)

When the TEST input pin is activated (V_{IH}), the smoke detection rate increases to once every 250 ms after one internal clock cycle. In PTT, the photo amplifier High Gain mode is selected and background reflections are used to simulate a Smoke condition. After the required three consecutive detections, the device goes into a Local Alarm condition. When the TEST input is driven low (V_{IL}), the photo amplifier normal gain is selected after one clock cycle. The detection rate continues at once every 250 ms until three consecutive No Smoke conditions are detected. At this point, the device returns to standby timing. In addition, after the TEST input goes low, the device enters the Hush mode (see **Section 3.6 "Reduced Sensitivity Mode"**).

3.5 Interconnect Operation

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high (High Boost) immediately through a constant-current source. Shorting this output to ground will not cause excessive current. The IO is ignored as input during a Local Alarm.

The IO pin also has a NMOS discharge device that is active for 1.3 seconds after the conclusion of any type of Local Alarm. This device helps quickly discharge any capacitance associated with the interconnect line.

If a remote, active-high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED is off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have a higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 336 ms nominal digital filter. This allows the interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

3.6 Reduced Sensitivity Mode

A Reduced Sensitivity or Hush mode is initiated by activating the TEST input (V_{IH}). If the TEST input is activated during a Local Alarm, the unit is immediately reset out of the Alarm condition and the horn is silenced. When the TEST input is deactivated (V_{IL}), the device enters into a nine-minute nominal Hush mode. During this period, the hush integration limit is selected. The hush gain is user programmable. In Reduced Sensitivity mode, the RLED flashes for 10 ms every 10 seconds to indicate that the mode is active. As an option, the Hush mode will be canceled if any of the following conditions exist:

- Reduced sensitivity threshold is exceeded (high smoke level)
- An interconnect alarm occurs
- TEST input is activated again

3.7 Local Alarm Memory

An alarm memory feature allows easy identification of any unit that had previously been in a Local Alarm condition. If a detector has entered a Local Alarm condition, the alarm memory latch is set when it exits that Local Alarm. Initially, the GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED flashes three times, spaced 1.3 seconds apart. This pattern repeats every 43 seconds. The duration of the Flash is 10 ms. To preserve battery power, this visual indication stops after a period of 24 hours. The user will still be able to identify a unit with an active alarm memory by pressing the PTT button. When this button is active, the horn chirps for 10 ms every 250 ms.

If the Alarm Memory condition is set, the alarm memory latch is reset any time the PTT button is pressed and released.

The initial 24-hour visual indication is not displayed if a Low Battery condition exists.

3.8 End-of-Life Indicator

As an option, after 14 days of continuous operation, the device will read a stored age count from the EEPROM and increment this count. After ten years of powered operation, an audible warning occurs, indicating that the unit should be replaced. This indicator is similar to the chamber test failure warning in that the horn pulses on three times for 10 ms, separated by 330 ms every 43 seconds. This indicator will be separated from the low battery indicator by approximately 20 seconds.

3.9 Photo Chamber Long-Term Drift (LTD) Adjustment

As an option, the design includes an LTD adjustment for the photo chamber. If the LTD adjustment is selected during calibration, a normal no smoke baseline integration measurement is made using Test mode T8 and this value is stored in EEPROM. During normal operation, a new baseline value is calculated by making 64 integration measurements over a period of eight hours. These measurements are averaged and the result is used to calculate the LTD adjustment.

The LTD adjustment is scaled for the operating mode and added to all four alarm limits stored in EEPROM during calibration. It is calculated by subtracting the original baseline from the averaged LTD value. The new alarm limits are not stored in EEPROM. The alarm limits cannot be adjusted to a value greater than 1.5 times the original alarm limit value stored in EEPROM.

LTD sampling is suspended during a Hush, Local Alarm or Remote Alarm condition. Any LTD values being saved for a new LTD average calculation are discarded when LTD sampling is suspended. The LTD sampling is restarted after the Hush, Local Alarm or Remote Alarm condition has ended.

4.0 USER PROGRAMMING MODES

User Programming modes provide the means to configure the RE46C191 for a particular application.

Parametric programming allows the photo amp gain and integration time to be adjusted for the particular application, along with the IRED current. Table 4-1 lists the parametric characteristics that can be selected for the application.

TABLE 4-1: PARAMETRIC PROGRAMMING(1,2,3)

Parametric Programming		Range		Resolution	
IRED Period		100-400 µs		100 µs	
IRED Current Sink		50-200 mA		50 mA	
Low Battery Detection Voltage		2.1-2.8V		100 mV	
Photo Detection Limits		Typical Maximum Input Current (nA)			
		100 µs	200 µs	300 µs	400 µs
Normal/Hysteresis	GF = 1	58	29	19.4	14.5
	GF = 2	29	14.5	9.6	7.2
	GF = 3	14.5	7.2	4.8	3.6
	GF = 4	7.2	3.6	2.4	1.8
Hush	GF = 1	116	58	38.8	29
	GF = 2	58	29	19.4	14.5
	GF = 3	29	14.5	9.6	7.2
	GF = 4	14.5	7.2	4.8	3.6
Chamber Test	GF = 1	29	14.5	9.6	7.2
	GF = 2	14.5	7.2	4.8	3.6
	GF = 3	7.2	3.6	2.4	1.8
	GF = 4	3.6	1.8	1.2	0.9

Note 1: GF is the user-selectable photo integration Gain Factor. Once selected, it applies to all modes of operation. For example, if GF = 1 and integration time is selected to be 100 µs, the ranges will be as follows: Normal/Hysteresis = 58 nA, Hush = 116 nA and Chamber Test = 29 nA.

2: Nominal measurement resolution in each case will be 1/63 of the maximum input range.

3: The same current resolution and ranges apply to the limits.

Features programming allows a number of device performance options to be selected or enabled. These features are listed in Table 4-2. In addition to programming the RE46C191, the User Programming modes provide the means to calibrate and test the RE46C191 in its various operating modes.

TABLE 4-2: FEATURES PROGRAMMING

Features	Options
Tone Select	Continuous or NFPA Tone
Ten-Year End-of-Life Indicator	Enable/Disable
Photo Chamber LTD Adjustment	Enable/Disable
Low Battery Hush	Enable/Disable
Hush Options	Option 1: Hush mode is not canceled for any reason. If the test button is pushed during Hush, the unit reverts to normal sensitivity to test the unit, but when it comes out of test, it resumes in Hush where it left off.
	Option 2: The Hush mode is canceled if the reduced sensitivity threshold is exceeded (high smoke level) and if an external interconnect alarm is signaled. If the test button is pushed during Hush after the test is executed, Hush mode is terminated.

4.1 Calibration and Programming Procedures

Thirteen separate Programming and Test modes are available for user customization. To enter these modes, after power-up, TEST2 must be driven to V_{DD} and held at that level. The TEST input is then clocked to step through the modes. FEED and IO are reconfigured to become Test mode inputs, while RLED, GLED and HB become Test mode outputs. The Test mode functions for each pin are outlined in Table 4-3.

When TEST2 is held at V_{DD}, TEST becomes a tri-state input with nominal input levels at V_{SS}, V_{DD} and V_{BST}. A TEST clock occurs whenever the TEST input switches from V_{SS} to V_{BST}. The TEST Data column represents the state of TEST when used as a data input, which is either V_{SS} or V_{DD}. The TEST pin can therefore be used as a clock to change modes and a data input once a mode is set. Other pin functions are described in **Section 4.2 "User Selections"**. V_{BST} is nominally 5V and V_{DD} is nominally 3V as shown in Figure 4-1.

TABLE 4-3: TEST MODE FUNCTIONS(5)

Mode	Description	TEST Clock	TEST Data	TEST2	FEED	IO	RLED	GLED	HB
	V_{IH}	V_{BST}	V_{DD}	V_{DD}	V_{BST}	V_{DD}	—	—	—
	V_{IL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	—	—	—
T0	Horn Test	0	HornEn	V_{DD}	FEED	IO	RLED	GLED	HB
T1	Low Battery test	1	Not Used	V_{DD}	FEED	LBstrb	RLEDen	GLEDen	LBout
T2	Photo Gain Factor (2 bits)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Integ. Time (2 bits)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	IRED Current (2 bits)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Low Battery Trip (3 bits)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LTD Enable (1 bit)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Hush Option (1 bit)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LB Hush Enable (1 bit)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	EOL Enable (1 bit)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Tone Select (1 bit)	2	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
T3	Norm. Lim. Set (6 bits)	3	Not Used	V_{DD}	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T4	Hyst. Lim. Set (6 bits)	4	Not Used	V_{DD}	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T5	Hush Lim. Set (6 bits)	5	Not Used	V_{DD}	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T6	Ch. Test Lim. Set (6 bits)	6	Not Used	V_{DD}	CalCLK	IntLat(3,4) ProgEn 24 bits	Gamp	IntegOut	SmkComp(1)
T7	Serial Read/Write	7	ProgData	V_{DD}	ProgCLK	ProgEn	RLED	GLED	Serial Out
T8	LTD Baseline (6 bits)	8	Not Used	V_{DD}	MeasEn	ProgEn	Gamp	IntegOut	HB
T9	Norm. Lim. Check	9	Not Used	V_{DD}	MeasEn	Not Used	Gamp	IntegOut	SCMP(2)
T10	Hyst. Lim. Check	10	Not Used	V_{DD}	MeasEn	Not Used	Gamp	IntegOut	SCMP(2)
T11	Hush Lim. Check	11	Not Used	V_{DD}	MeasEn	Not Used	Gamp	IntegOut	SCMP(2)
T12	Ch Test Lim. Check	12	Not Used	V_{DD}	MeasEn	Not Used	Gamp	IntegOut	SCMP(2)

Note 1: SmkComp (HB) – digital comparator output (high if Gamp < IntegOut; low if Gamp > IntegOut).

2: SCMP (HB) – digital output representing comparison of measurement value and associated limit. Signal is valid only after MeasEn has been asserted and measurement has been made. (SCMP high if measured value > limit; low if measured value < limit).

3: IntLat (IO) – digital input used for two purposes. If FEED is at a high logic level, then a low-to-high transition on IntLat will initiate an integration cycle. If FEED is at a low logic level, then a low-to-high transition on IntLat will latch the present state of the limits (Gamp level) for later storage. T2-T5 limits are latched, but not stored until ProgEn is asserted in T6 mode.

4: At the end of T6 mode, to store the limits, the IO input must be pulsed twice consecutively with FEED held low. The first pulse latches the data and the second stores them in EEPROM.

5: Test modes are only intended for product development and agency certification.

4.2 User Selections

Prior to smoke calibration, the user must program the functional options and parametric selections. This requires that 14 bits, representing selected values, be clocked in serially using TEST as a data input and FEED as a clock input and then be stored in the internal EEPROM.

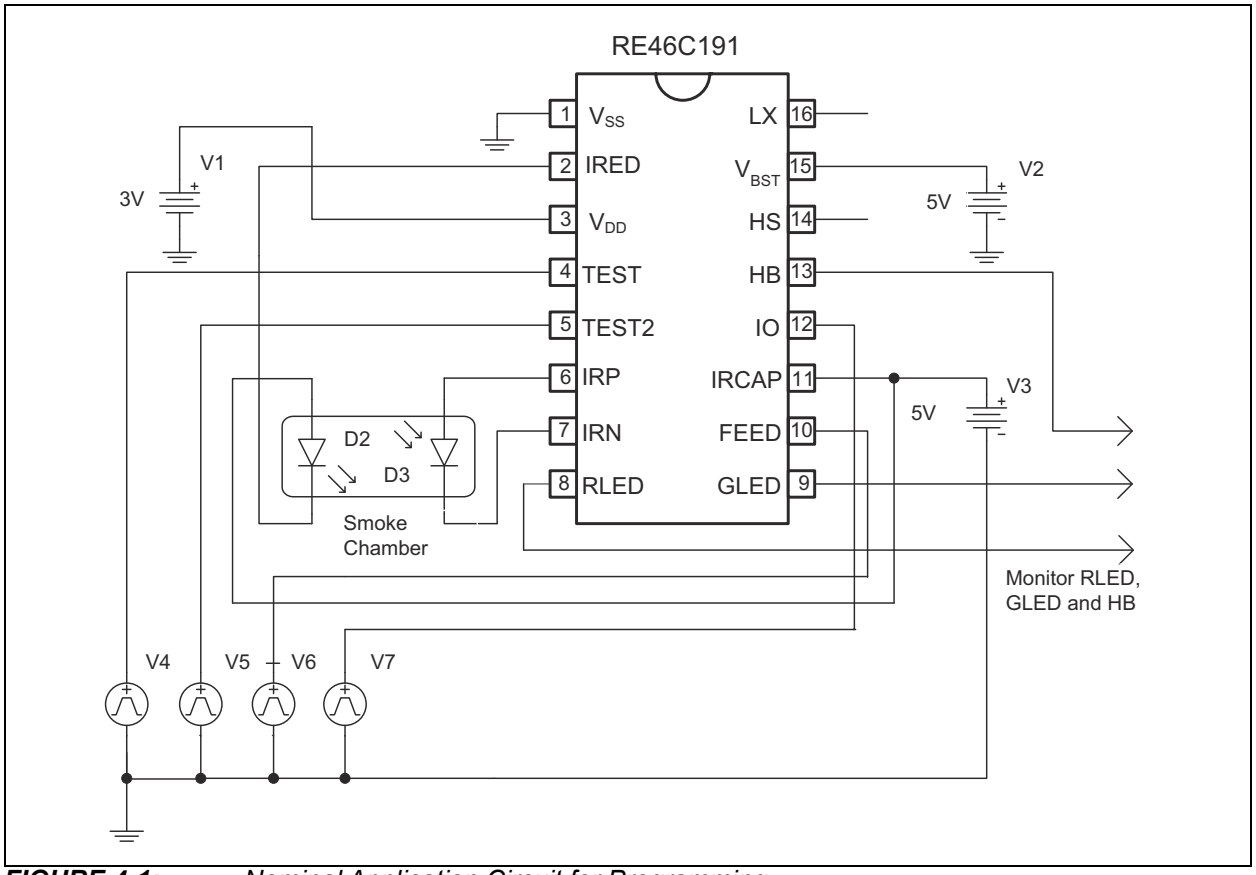


FIGURE 4-1: *Nominal Application Circuit for Programming.*

The detailed steps are as follows:

1. Power up with bias conditions as shown in Figure 4-1. At power-up, TEST = TEST2 = FEED = IO = V_{SS}.
2. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} through Step 5 below.
3. Using TEST as data and FEED as clock, shift in values as selected from Register 4-1.

Note:	For Test mode T2, only 14 bits (bits 30-43) will be loaded. For Test mode T8, all 44 bits (bits 0-43) will be loaded.

The minimum pulse width for FEED is 10 µs, while the minimum pulse width for TEST is 100 µs. For example, for the following options, the sequence would be:

Data =	0	0	0	1	1	0	0	0	1	0	0	0	0	1
Bit =	30	31	32	33	34	35	36	37	38	39	40	41	42	43

Photo Amp Gain Factor = 1
Integration Time = 200 µs
IRED Current = 100 mA
Low Battery Trip = 2.5V
LTD, Low Battery Hush and EOL are All Disabled
Hush Option = Never Cancel
Tone Select = Temporal

4. After shifting in data, pull IO input to V_{DD}, then V_{SS} (minimum pulse width of 10 ms) to store Shift register contents into the memory.
5. If any changes are required, power down the part and return to Step 1. All bit values must be reentered.

REGISTER 4-1: CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

W	W	W	W
TS	EOL	LBH	HUSH
bit 43			bit 40

W	W	W	W	W	W	W	W
LTD	LB2	LB1	LB0	IRC1	IRC0	IT1	IT0
bit 39							bit 32

W	W	W	W	W	W	W	W
PAGF1	PAGF0	NL5	NL4	NL3	NL2	NL1	NL0
bit 31							bit 24

W	W	W	W	W	W	W	W
HYL5	HYL4	HYL3	HYL2	HYL1	HYL0	HUL5	HUL4
bit 23							bit 16

W	W	W	W	W	W	W	W
HUL3	HUL2	HUL1	HUL0	CTL5	CTL4	CTL3	CTL2
bit 15							bit 8

W	W	W	W	W	W	W	W
CTL1	CTL0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 43 **TS:** Tone Select
1 = Temporal horn pattern
0 = Continuous horn pattern

bit 42 **EOL:** End-of-Life Enable
1 = Enable
0 = Disable

bit 41 **LBH:** Low Battery Hush Enable
1 = Enable
0 = Disable

bit 40 **HUSH:** Hush Option
1 = Canceled for high smoke level, interconnect alarm or second push of TEST button (as described above)
0 = Never cancel

bit 39 **LTD:** Long-Term Drift Enable
1 = Enable
0 = Disable

bit 38-36 **LB[2:0]:** Low Battery Trip Point
000 = 2.1V
001 = 2.2V
010 = 2.3V
011 = 2.4V
100 = 2.5V
101 = 2.6V
110 = 2.7V
111 = 2.8V

REGISTER 4-1: CONFIGURATION SETTINGS AND CALIBRATION SETTINGS (CONTINUED)

bit 35-34 **IRC[1:0]:** IRED Current
00 = 50 mA
01 = 100 mA
10 = 150 mA
11 = 200 mA

bit 33-32 **IT[1:0]:** Integration Time
00 = 400 µs
01 = 300 µs
10 = 200 µs
11 = 100 µs

bit 31-30 **PAGF[1:0]:** Photo Amplifier Gain Factor
00 = 1
01 = 2
10 = 3
11 = 4

bit 29-24 **NL[5:0]:** Normal Limits (**Section 3.2 "Smoke Detection Circuitry"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

bit 23-18 **HYL[5:0]:** Hysteresis Limits (**Section 3.2 "Smoke Detection Circuitry"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

bit 17-12 **HUL[5:0]:** Hush Limits (**Section 3.6 "Reduced Sensitivity Mode"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

bit 11-6 **CTL[5:0]:** Chamber Test Limits (**Section 3.3 "Supervisory Tests"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

bit 5-0 **LTD[5:0]:** Long-Term Drift Sample (**Section 3.9 "Photo Chamber Long-Term Drift (LTD) Adjustment"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

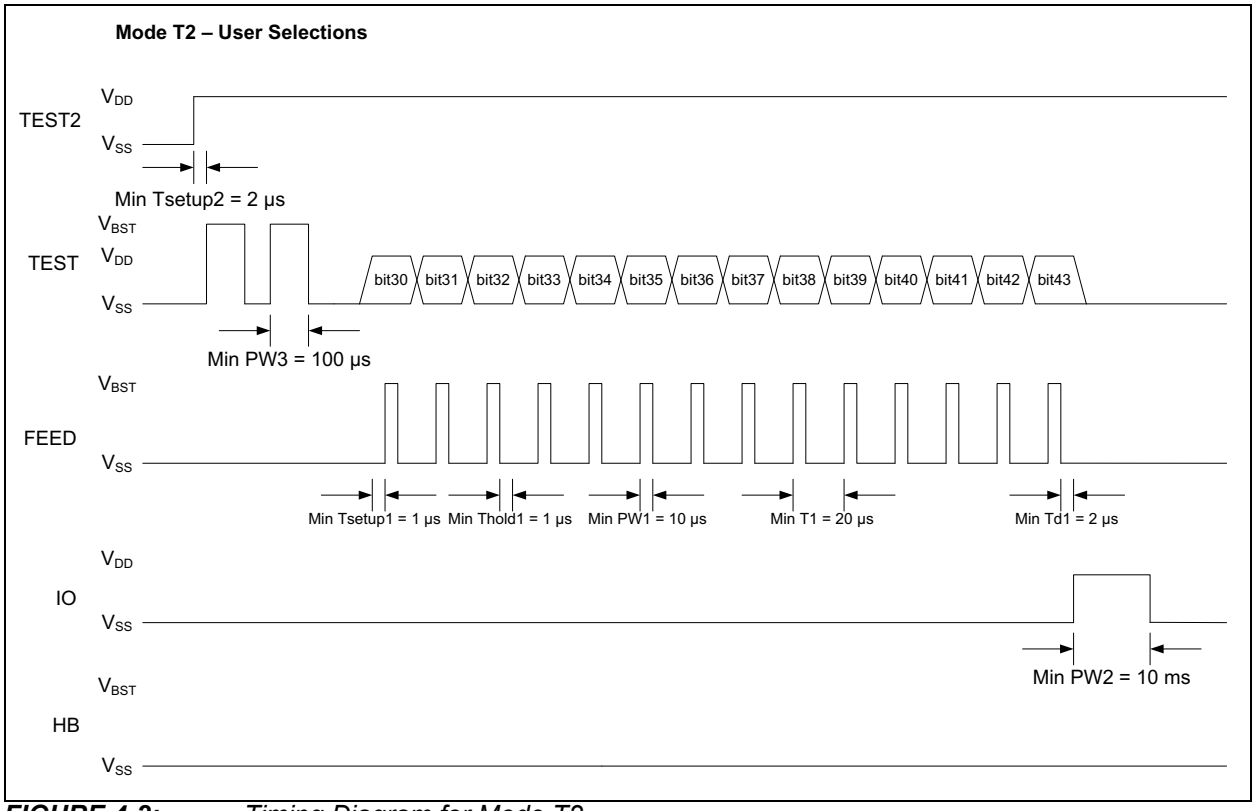


FIGURE 4-2: *Timing Diagram for Mode T2.*

As an alternative to Figure 4-1, Figure 4-3 can be used to program while in the application circuit. Note that in addition to the five programming supplies, connections to V_{SS} are needed at TP1 and TP2.

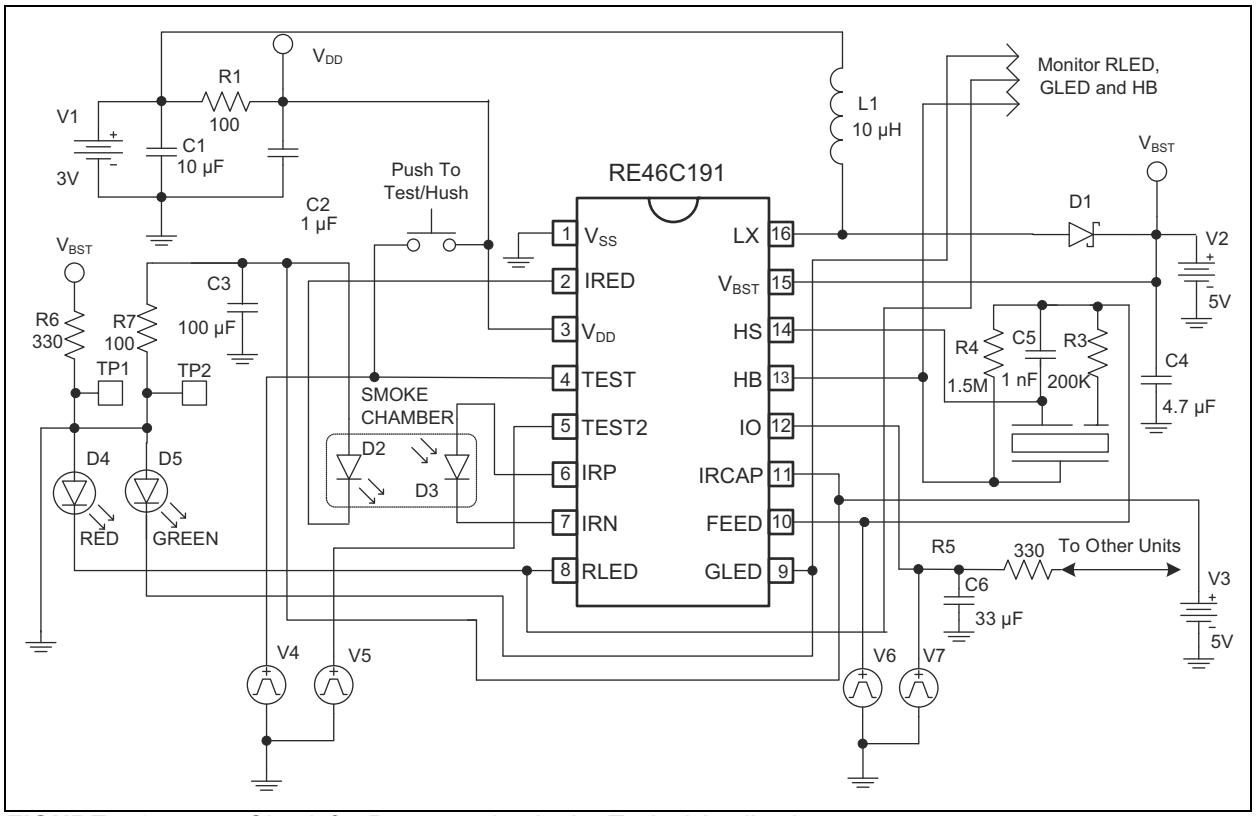


FIGURE 4-3: *Circuit for Programming in the Typical Application.*

4.3 Smoke Calibration

A separate Calibration mode is entered for each Measurement mode (Normal, Hysteresis, Hush and Chamber Test), so that independent limits can be set for each. In all Calibration modes, the integrator output can be accessed at the GLED output.

The Gamp output voltage, which represents the smoke detection level, can be accessed at the RLED output. The SmkComp output voltage is the result of the comparison of Gamp with the integrator output and can be accessed at HB. The FEED input can be clocked to step up the smoke detection level at RLED. Once the desired smoke threshold is reached, the TEST input is pulsed low-to-high to store the result.

The procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 4-1.
2. Drive TEST2 input from V_{SS} to V_{DD} to enter Programming mode. TEST2 should remain at V_{DD} through Step 8 described below.
3. Apply three clock pulses to the TEST input to enter T3 mode. This initiates the Calibration mode for normal limits setting. The integrator output should appear at GLED and the smoke detection level at RLED.
4. At this point, clock FEED to increase the smoke detection level as needed. Pulling IO high with FEED at a high logic level will initiate an integration. The integrator output signal should appear at GLED. The sequence of incrementing the limit, performing an integration and monitoring the HB output for the resulting comparison, can be repeated until the desired threshold is reached. Once the desired smoke threshold is reached, with FEED held low, the IO input should be pulsed low-to-high to latch the smoke detection level.
5. Apply a fourth clock pulse to the TEST input to enter T4 mode. This initiates the Calibration mode for hysteresis limits. The sequence in Step 4 should be repeated to set the hysteresis limit.
6. Apply a clock pulse to the TEST input again to enter T5 mode and initiate calibration for hush limits. Repeat Step 4 to set the hush limit.
7. Apply clock pulse to the TEST input a sixth time to enter T6 mode and initiate calibration for chamber test limits. Repeat Step 4 to set the chamber test limit.
8. After pulsing the IO input to latch the chamber test limit, the IO must be pulsed low-to-high a second time to store the limits in memory.

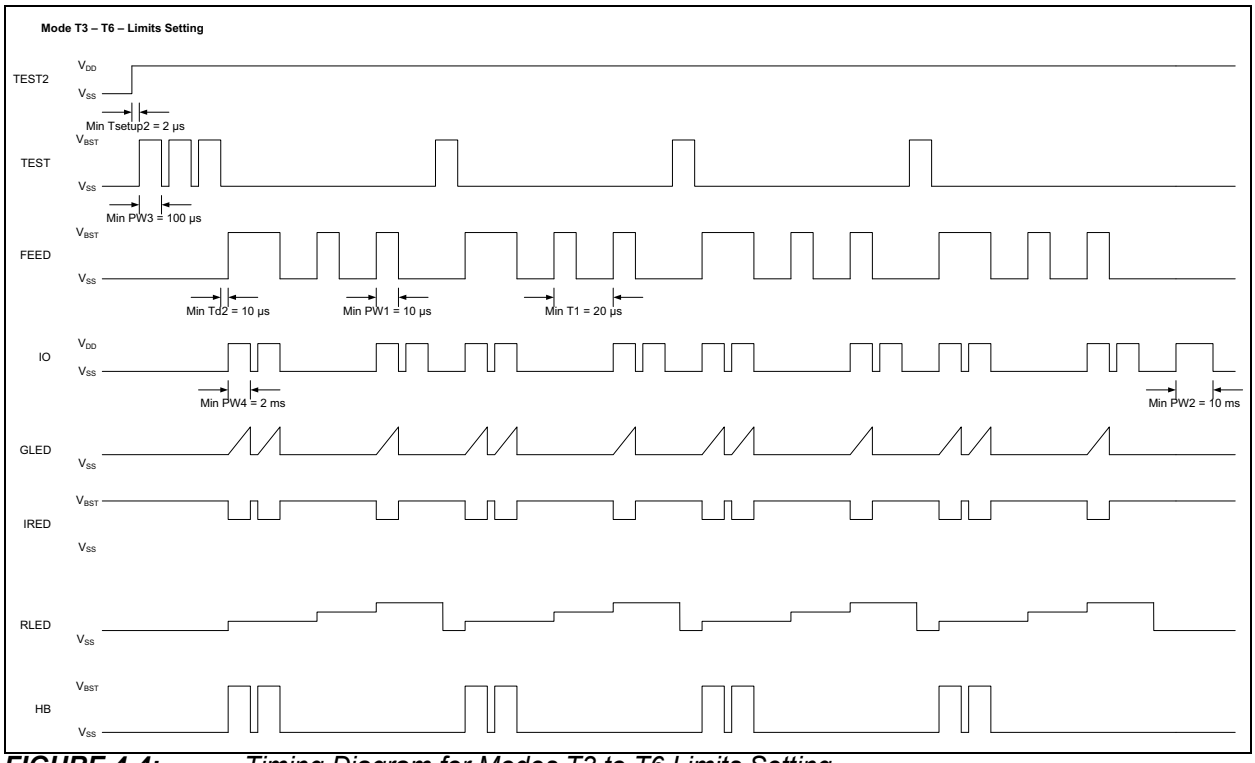


FIGURE 4-4: *Timing Diagram for Modes T3 to T6 Limits Setting.*

4.4 Serial Read/Write

As an alternative to the steps in **Section 4.3 "Smoke Calibration"**, if the system has been well characterized, the limits and baseline can be entered directly from a Serial Read/Write Calibration mode.

To enter this mode, follow these steps:

1. Set up the application as shown in Figure 4-1.
2. Drive TEST2 input from V_{SS} to V_{DD} to enter the Programming mode. TEST2 should remain at V_{DD} until all data have been entered.
3. Clock the TEST input to mode T7 (High = V_{BST}, Low = V_{SS}, seven clocks). This enables the Serial Read/Write mode.
4. TEST now acts as a data input (High = V_{DD}, Low = V_{SS}). FEED acts as the clock input (High = V_{BST}, Low = V_{SS}). Clock in the limits, LTD baseline, functional and parametric options. The data sequence follows the pattern described in Register 4-1. A serial data output is available at HB.
5. Pulse IO to store all 44 bits into the EEPROM memory.

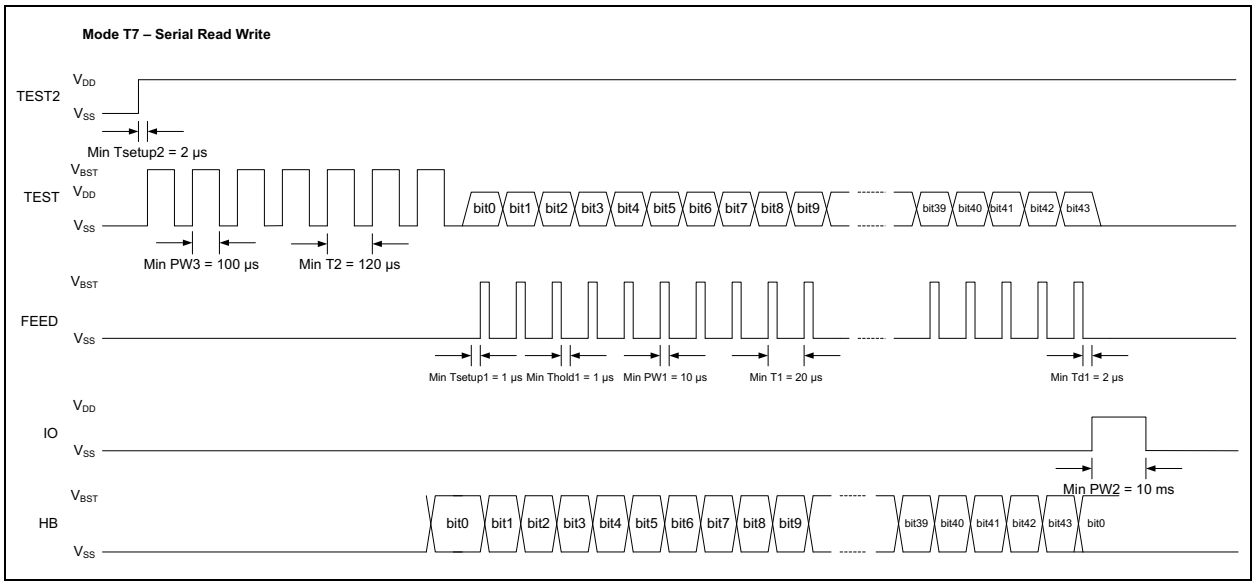


FIGURE 4-5: *Timing Diagram for Mode T7.*

The RE46C191 is shipped with the programming values shown in Table 4-4. These are not recommended values for a smoke detector design. The smoke detector must be calibrated using the Test modes provided.

TABLE 4-4: REGISTER 4-1 PROGRAMMING VALUES

Bit Value					0	0	0	0
Bit Name					TS	EOL	LBH	HUSH
Bit Count					bit 43			bit 40
Bit Value	0	1	1	0	0	1	1	0
Bit Name	LTD	LB2	LB1	LB0	IRC1	IRC0	IT1	IT0
Bit Count	bit 39							bit 32
Bit Value	0	1	0	1	0	0	0	0
Bit Name	PAGF1	PAGF0	NL5	NL4	NL3	NL2	NL1	NL0
Bit Count	bit 31							bit 24
Bit Value	0	1	0	0	0	0	0	0
Bit Name	HYL5	HYL4	HYL3	HYL2	HYL1	HYL0	HUL5	HUL4
Bit Count	bit 23							bit 16
Bit Value	1	0	0	0	0	0	0	0
Bit Name	HUL3	HUL2	HUL1	HUL0	CTL5	CTL4	CTL3	CTL2
Bit Count	bit 15							bit 8
Bit Value	1	0	1	1	0	0	0	1
Bit Name	CTL1	CTL0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
Bit Count	bit 7							bit 0

4.5 LTD Baseline Measurement

If the LTD adjustment is enabled, an LTD baseline must be set. If an accurate value is known based on previous chamber characterization, it can be loaded above in T7 with the serial data. If not, zeros can be entered as placeholders in T7 and an LTD baseline measurement must be made. To do this, the unit should be connected to its smoke chamber and placed in a No Smoke condition.

To complete the LTD baseline measurement, follow these steps:

1. Set up the application as shown in Figure 4-1.
2. Drive the TEST2 input from V_{SS} to V_{DD} to enter Programming mode. TEST2 must remain at V_{DD} until the measurement is completed.
3. Apply eight clock pulses (V_{SS} to V_{BST}) to the TEST input to enter T8 mode. This initiates the LTD baseline measurement.
4. Pulse FEED from V_{SS} to V_{BST} to make the baseline measurement. The duration of this pulse should be at least 2 ms.
5. To save the LTD baseline measurement to EEPROM, pulse IO from V_{SS} to V_{DD} with FEED held low. The duration of this pulse should be at least 10 ms.

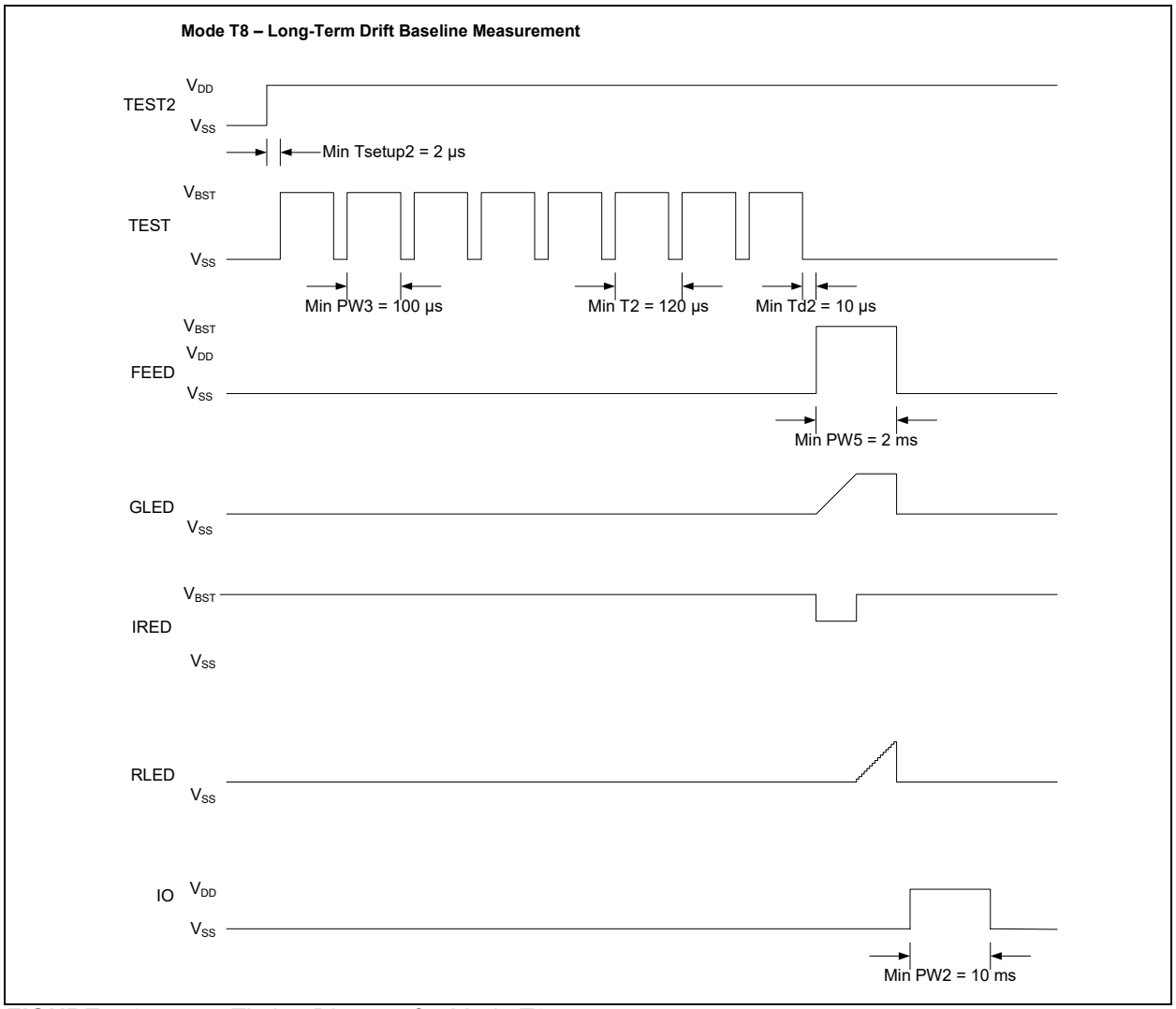


FIGURE 4-6: *Timing Diagram for Mode T8.*

4.6 Limits Verification

After all limits and the LTD baseline are entered and stored into the memory, additional Test modes are available to verify if the limits are functioning as expected.

The procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 4-1.
2. Drive the TEST2 input from V_{SS} to V_{DD} to enter the Programming mode. TEST2 should remain at V_{DD} through Step 7 described below.
3. Apply nine clock pulses to the TEST input to enter T9 mode. This initiates the Verification mode for normal limits setting. The integrator output will appear at GLED and the smoke detection level, Gamp, at RLED.
4. At this point, pulse FEED high for at least 2 ms to initiate a smoke check. When the smoke detection level exceeds the alarm threshold, the HB output will be asserted high. The test is repeated each time FEED is clocked high.
5. Apply a clock pulse to the TEST input to enter T10 mode. This initiates the Verification mode for hysteresis limits. The sequence in Step 4 should be repeated to verify the hysteresis limit.
6. Apply a clock pulse to the TEST input again to enter T11 mode and initiate verification for hush limits. Repeat Step 4 to verify the hush limit.
7. Apply a clock pulse to the TEST input again to enter T12 mode and initiate verification for chamber test limits. Repeat Step 4 to verify the chamber test limit.

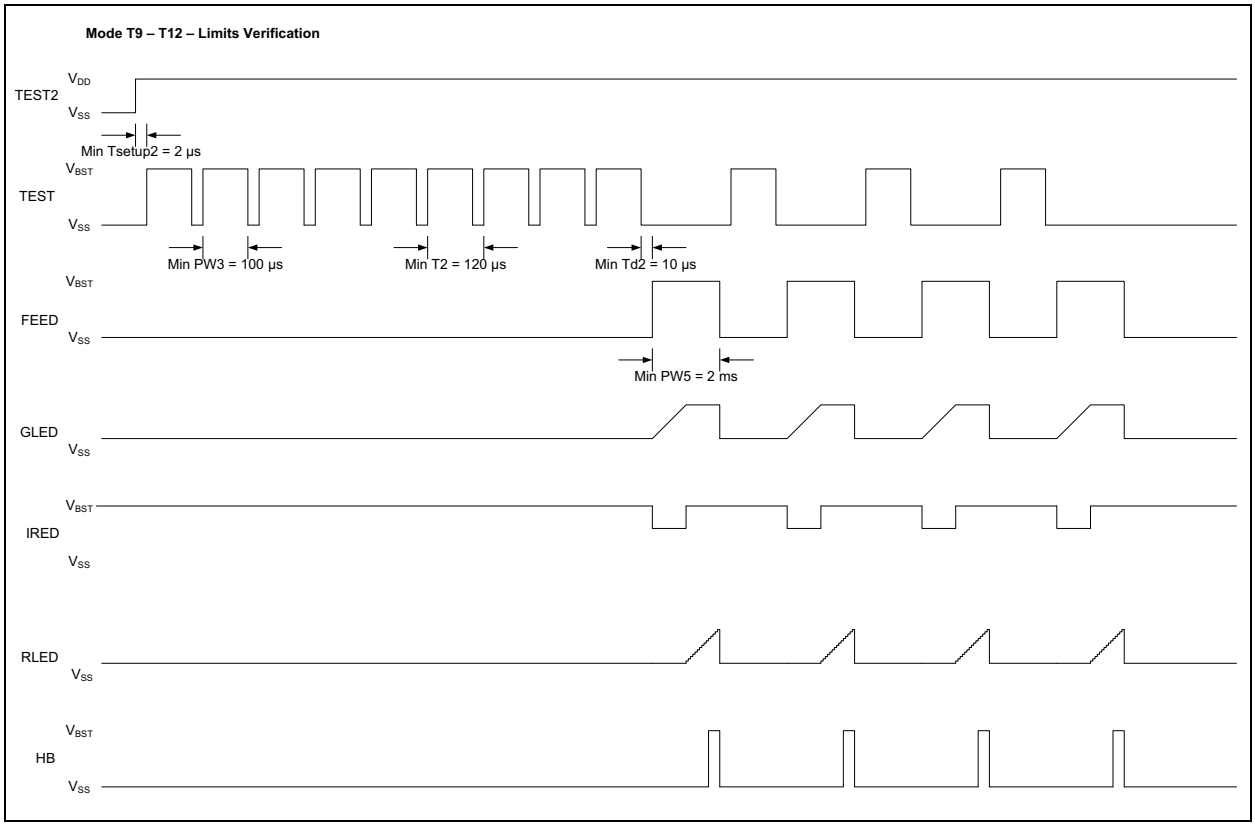


FIGURE 4-7: *Timing Diagram for Mode T9-T12.*

The equation for digitizing the integrator voltage, V_{INT}, that displays on GLED is shown in Equation 4-1, where DV represents the digitized value and V_{INT} is measured in volts.

EQUATION 4-1:

$$DV = Integer\left(\frac{V_{INT} - 0.200}{0.0375}\right)$$

4.7 Horn Test

Test mode T0 allows the horn to be enabled indefinitely for audibility testing. TEST must go high to V_{DD} first, then TEST2. Enabling the horn indefinitely allows V_{BST} to reach the high V_{BST} level and the horn to achieve the necessary sound pressure level.

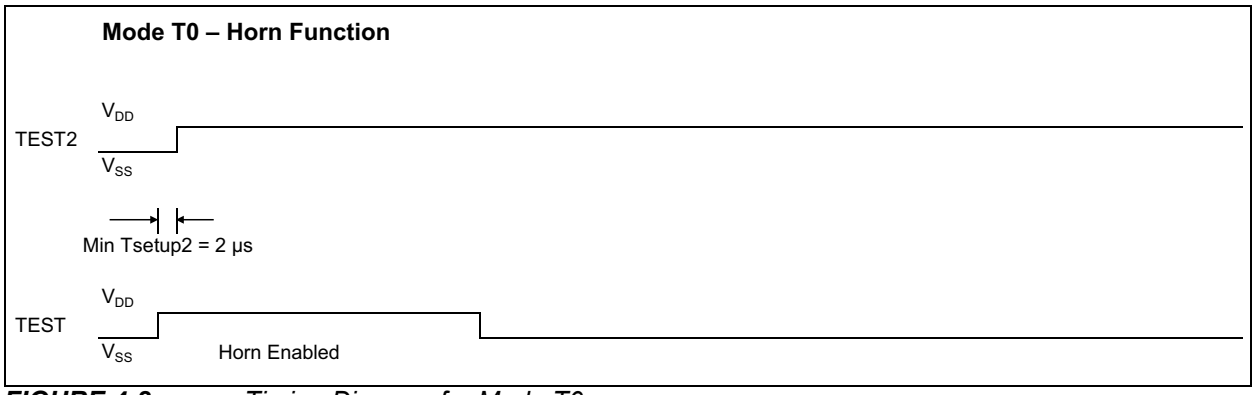


FIGURE 4-8: *Timing Diagram for Mode T0.*

4.8 Low Battery Test

This mode allows the user to enable the internal low battery circuitry to perform a low battery test. To implement this test, the 5V power supply needs to be diode-connected to V_{BST} and IRCAP. This will allow the boost converter to turn on properly as described in Step 4. To enter this mode, follow these steps:

1. Power up with the bias conditions shown in Figure 4-1.
2. Drive the TEST2 input from V_{SS} to V_{DD} to enter the Programming mode. TEST2 should remain at V_{DD} through the following steps.
3. Apply one clock pulse to the TEST input to enter the T1 mode.
4. Drive the IO input from V_{SS} to V_{DD}. This will enable the boost converter and turn on the RLED driver.
5. Monitor the HB output for the low battery comparator status.

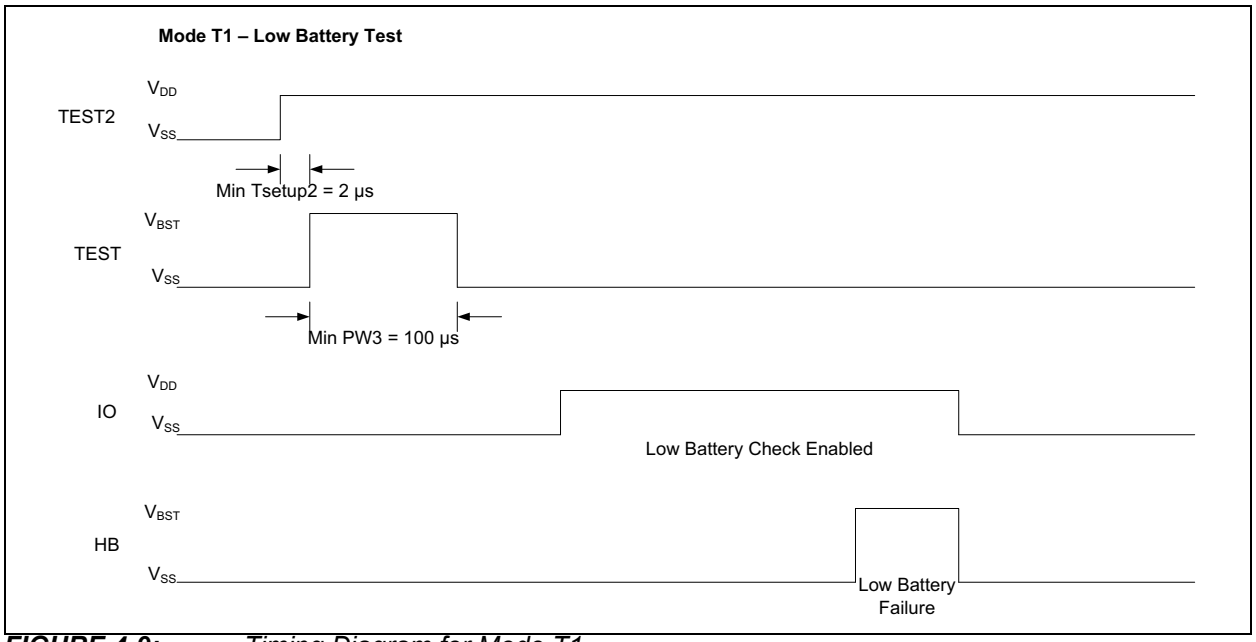


FIGURE 4-9: *Timing Diagram for Mode T1.*

5.0 APPLICATION INFORMATION

5.1 Standby Current Calculation and Battery Life

The supply current shown in the **DC Electrical Characteristics** table is only one component of the average standby current. In most cases, the supply current can be a small fraction of the total because power consumption generally occurs in relatively infrequent bursts and depends on many external factors. These include the values selected for IRED current and integration time, the V_{BST} and IR capacitor sizes and leakages, the V_{BAT} level and the magnitude of any external resistances that will adversely affect boost converter efficiency.

Table 5-1 shows a calculation of standby current for the battery life based on the following parameters:

V_{BAT}	=	3
V_{BST1}	=	3.6
V_{BST2}	=	9
Boost Capacitor Size	=	4.70E-06
Boost Efficiency	=	8.50E-01
IRED On Time	=	2.000E-04
IRED Current	=	1.000E-01

TABLE 5-1: STANDBY CURRENT CALCULATION

I_{DD} Component	Voltage (V)	Current (A)	Duration (s)	Energy (J)	Period (s)	Average Power (W)	I_{BAT} Contribution (A)	I_{BAT} (µA)
Fixed I_{DD}	3	1.00E-06	—	—	—	3.00E-06	1.00E-06	1.0
Photo Detection Current								
Chamber Test (excluding IR drive)	3.6	1.00E-03	3.0E-03	1.08E-05	43	2.95E-07	9.85E-08	0.1
IR Drive during Chamber Test	3.6	0.10	2.00E-04	7.20E-05	43	1.97E-06	6.57E-07	0.7
Smoke Detection (excluding IR drive)	3.6	1.00E-03	3.0E-03	1.08E-05	10.75	1.18E-06	3.94E-07	0.4
IR Drive during Smoke Detection	3.6	0.10	2.00E-04	7.20E-05	10.75	7.88E-06	2.63E-06	2.6
Low Battery Check Current								
Loaded Test								
Load	9	2.00E-02	1.00E-02	1.80E-03	344	6.16E-06	2.05E-06	2.1
Boost	V_{BST1} to V_{BST2}	—	—	6.85E-05	344	2.34E-07	7.81E-08	0.1
Unloaded Test								
Load	3.6	1.00E-04	1.00E-02	3.60E-06	43	9.85E-08	3.28E-08	0.0
						Total	6.94E-06	6.9

The following paragraphs explain the components in Table 5-1 and the calculations in the example.

5.1.1 FIXED I_{DD}

The I_{DD} is the Supply Current shown in the **DC Electrical Characteristics** table.

5.1.2 PHOTO DETECTION CURRENT

Photo detection current is the current drawn due to the smoke testing every 10.75 seconds and the chamber test every 43 seconds. The current for both the IR diode and the internal measurement circuitry comes primarily from V_{BST}, so the average current must be scaled for both on time and boost voltage.

The contribution to I_{BAT} is determined by first calculating the energy consumed by each component given its duration. An average power is then calculated based on the period of the event and the boost converter efficiency (assumed to be 85% in this case). An I_{BAT} contribution is then calculated based on this average power and the given V_{BAT}. For example, the IR drive contribution during a chamber test is detailed in Equation 5-1:

EQUATION 5-1:

$$\frac{3.6V \times 0.1A \times 200\mu s}{43s \times 0.85 \times 3V} = 0.657\mu A$$

5.1.3 LOW BATTERY CHECK CURRENT

The low battery check current is the current required for the low battery test. It includes both the loaded (RLED on) and unloaded (RLED off) tests. The boost component of the loaded test represents the cost of charging the boost capacitor to the higher voltage level. This has a fixed cost for every loaded check because the capacitor is gradually discharged during subsequent operations and the energy is generally not recovered. The other calculations are similar to those shown in Equation 5-1. The unloaded test has a minimal contribution because it involves only some internal reference and comparator circuitry.

5.1.4 BATTERY LIFE

When estimating the battery life, several additional factors must be considered. These include battery resistance, battery self-discharge rate, capacitor leakages and the effect of the operating temperature on all of these characteristics. Some number of false alarms and user tests should also be included in any calculation.

For 10-year applications, a 3V spiral wound lithium manganese dioxide battery with a laser seal is recommended. These can be found with capacities of 1400 to 1600 mAh.

5.1.5 FUNCTIONAL TIMING DIAGRAMS

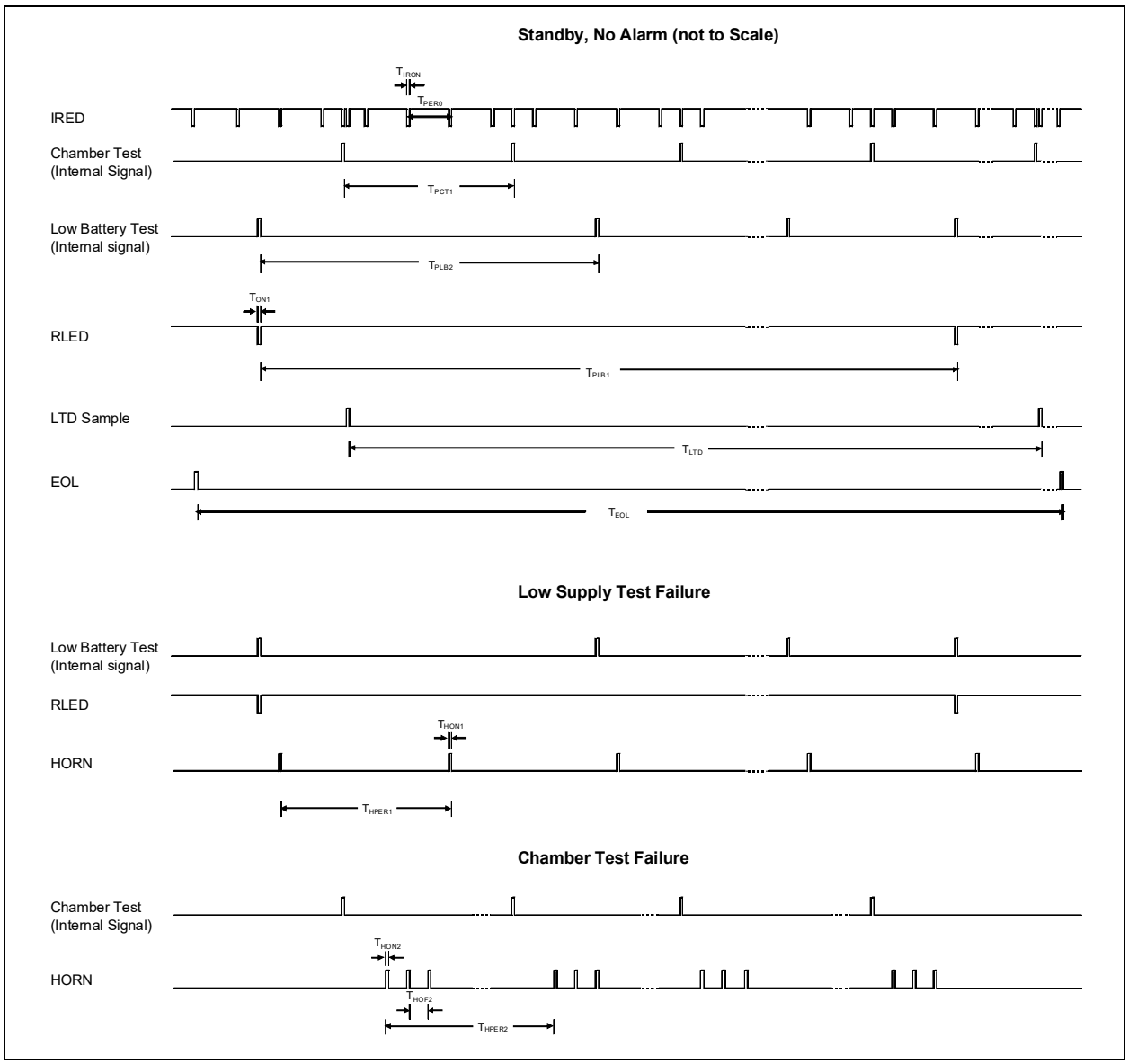


FIGURE 5-1: *RE46C191 Timing Diagram – Standby, No Alarm, Low Supply Test Failure and Chamber Test Failure.*

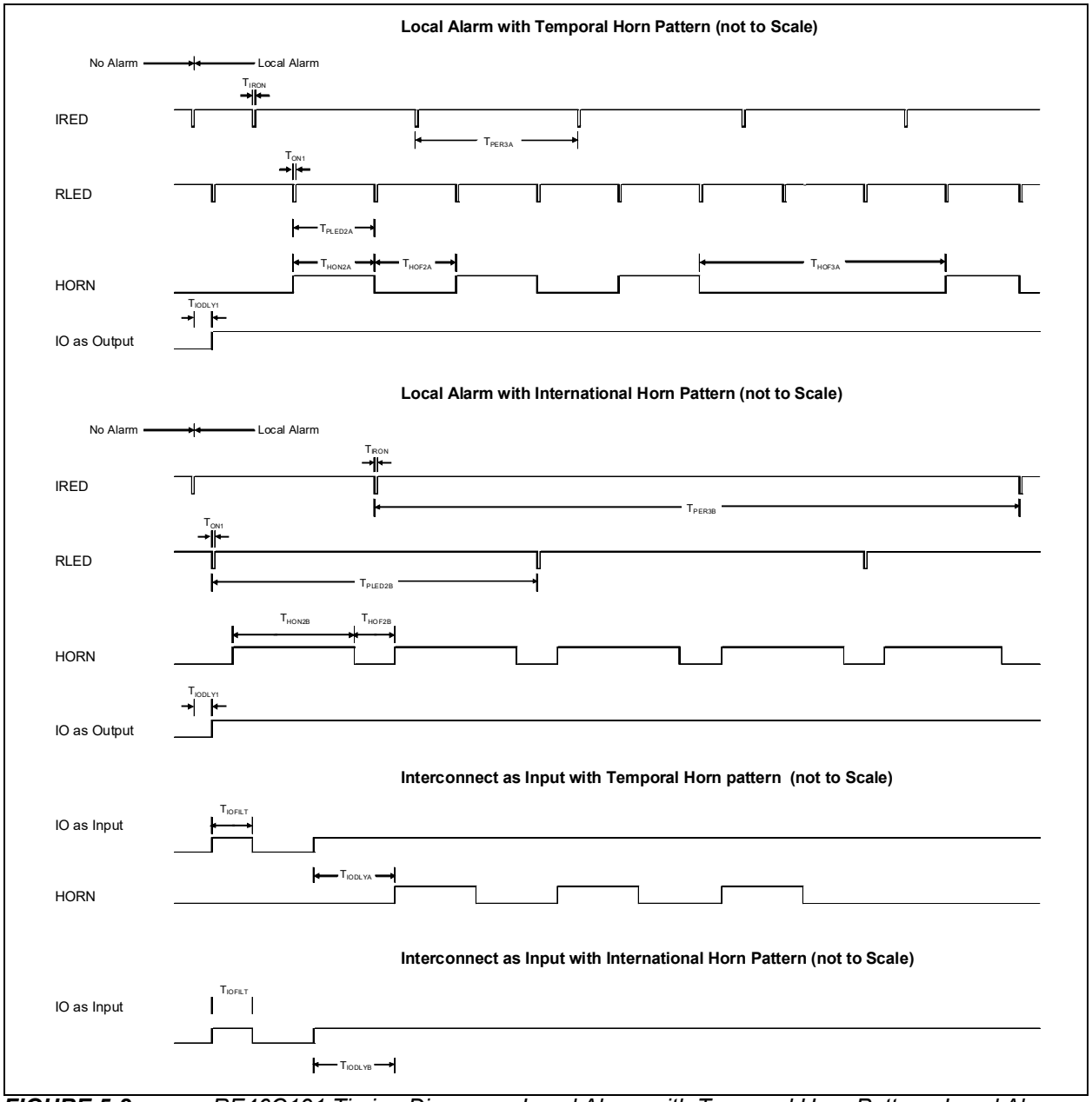


FIGURE 5-2: *RE46C191 Timing Diagram – Local Alarm with Temporal Horn Pattern, Local Alarm with International Horn Pattern, Interconnect as Input with Temporal Horn Pattern and Interconnect as Input with International Horn Pattern.*

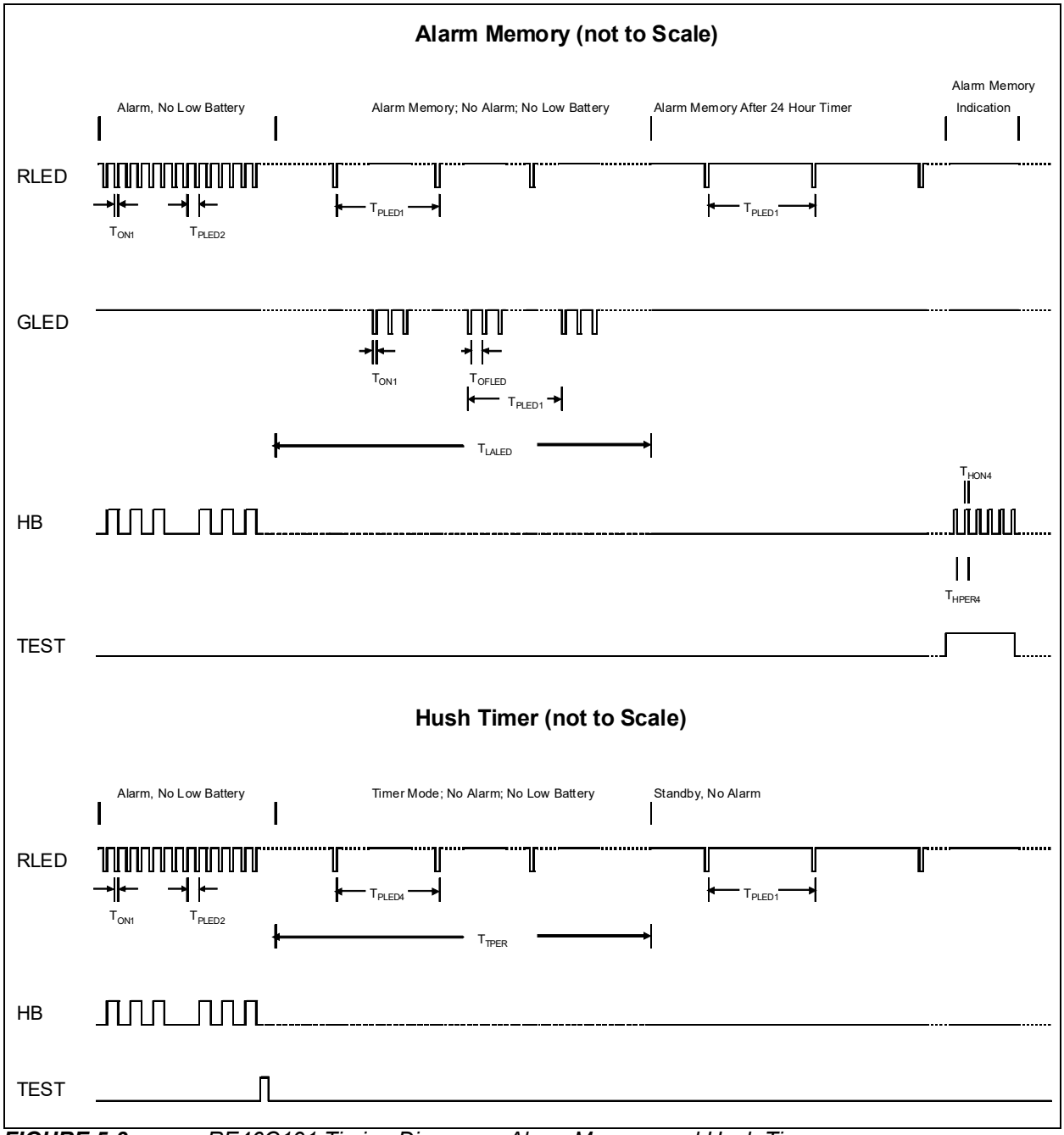


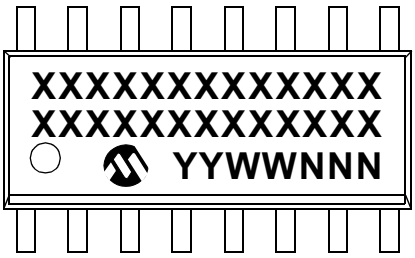
FIGURE 5-3: *RE46C191 Timing Diagram – Alarm Memory and Hush Timer.*

NOTES:

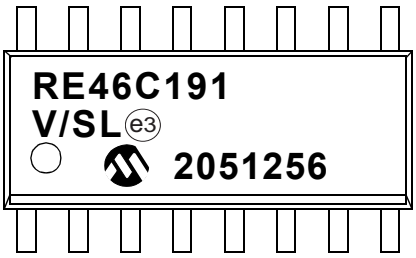
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

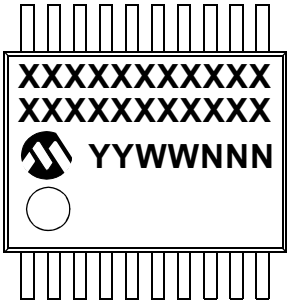
16-Lead Narrow SOIC (3.90 mm)



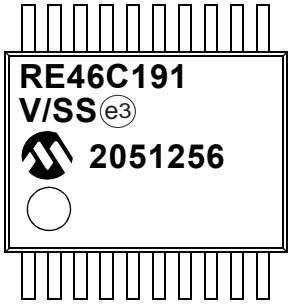
Example



20-Lead SSOP (5.30 mm)



Example

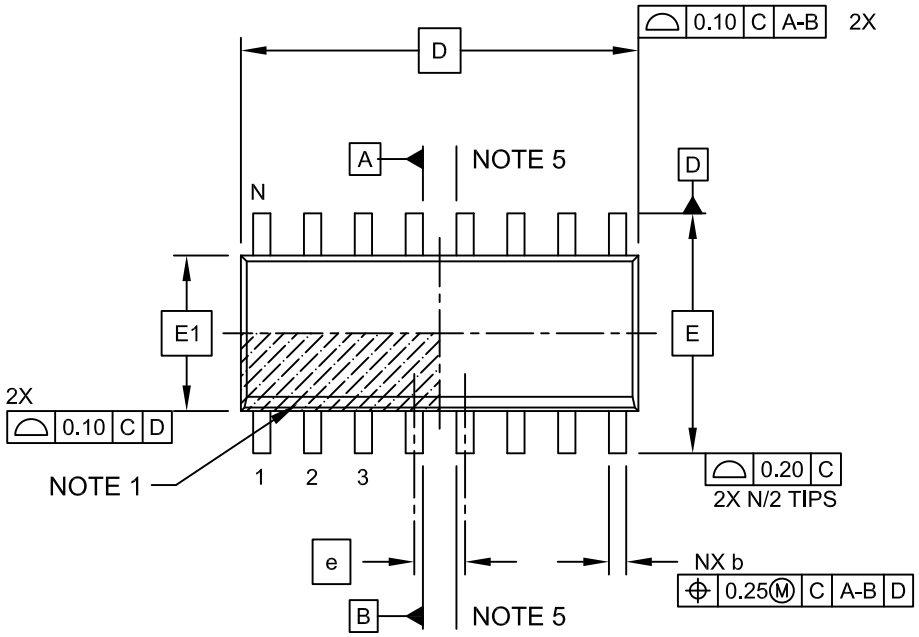


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

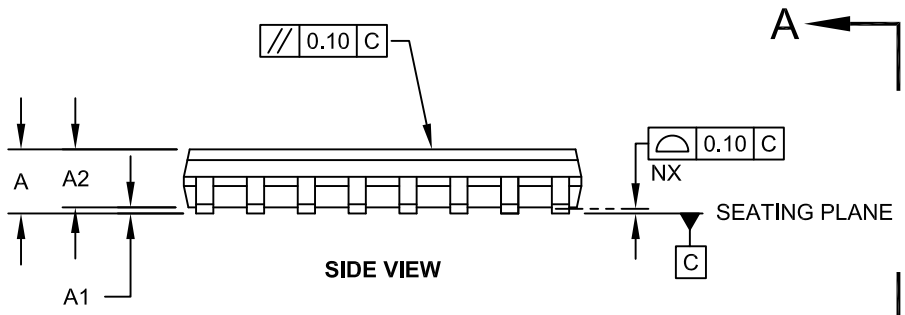
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

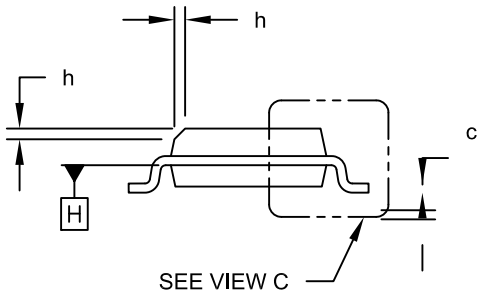
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

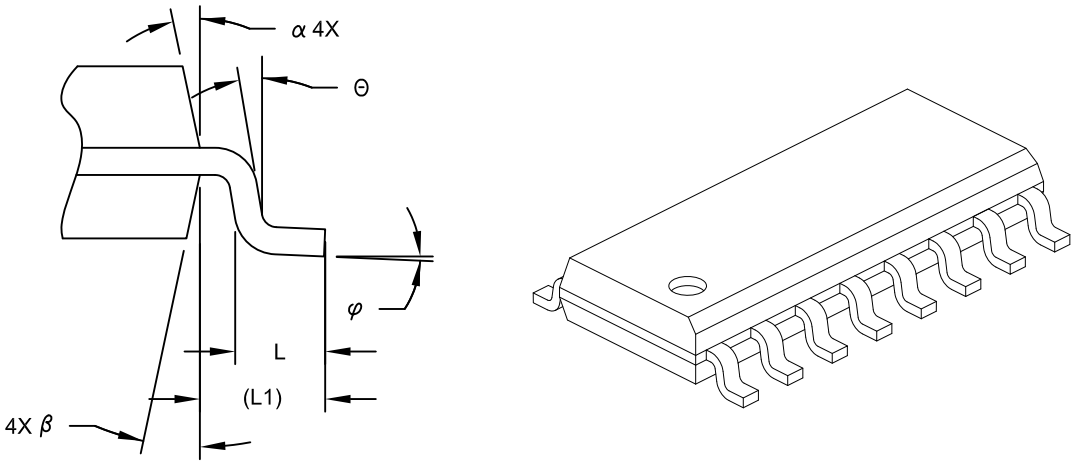


VIEW A-A

Microchip Technology Drawing No. C04-108C Sheet 1 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		9.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

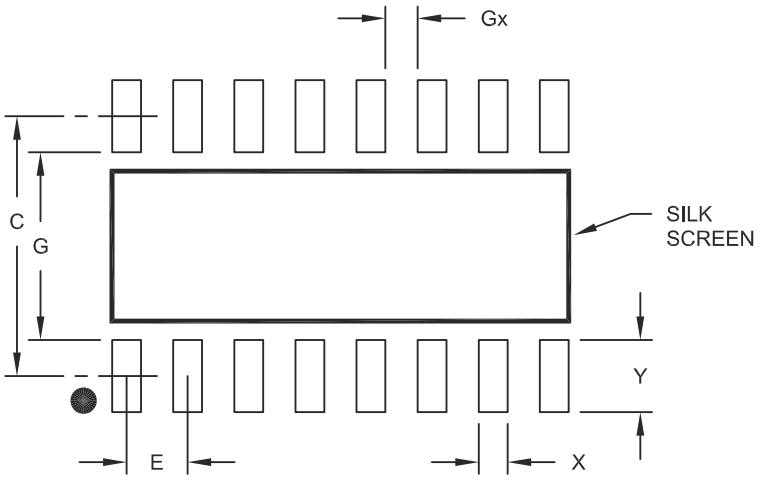
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-108C Sheet 2 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

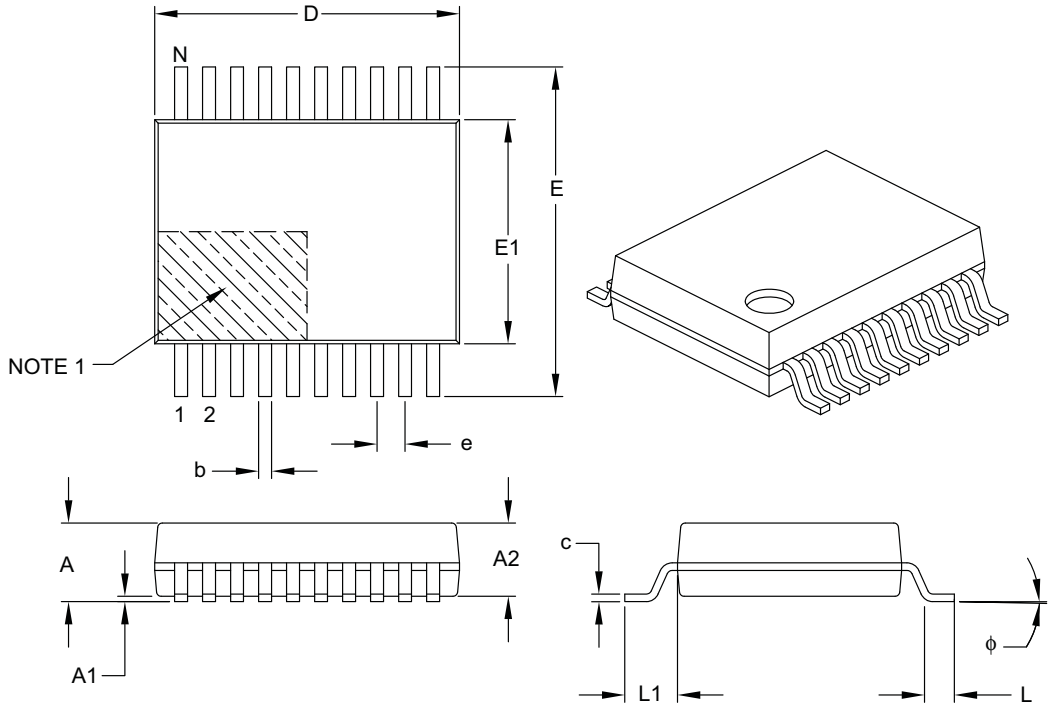
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

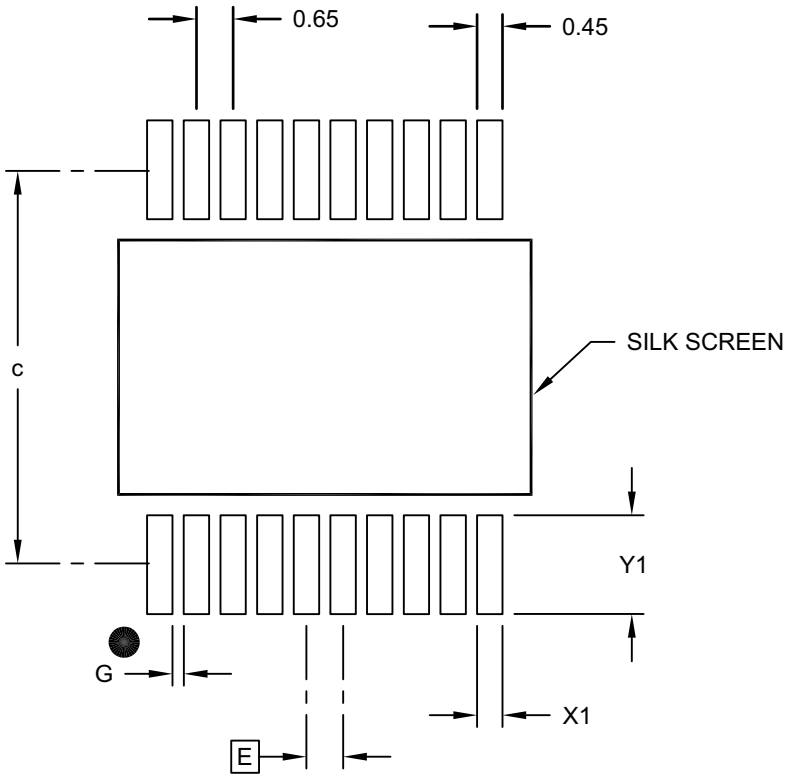
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

APPENDIX A: REVISION HISTORY

Revision G (February 2021)

The following is the list of modifications:

1. Corrected Table 4-4.
2. Minor typographical errors.

Revision F (February 2021)

The following is the list of modifications:

1. Added 20-Lead SSOP package option and related information throughout the document.
2. Updated Table 4-3.
3. Updated **Section 4.7 "Horn Test"**.

Revision E (October 2017)

1. Removed "Confidential" from the document.

Revision D (December 2015)

The following is the list of modifications:

1. Updated **Section 4.1 "Calibration and Programming Procedures"**.
2. Updated **Section 4.4 "Serial Read/Write"**.
3. Added Table 4-4.
4. Updated **Section 4.6 "Limits Verification"**.
5. Added Equation 4-1.

Revision C (October 2014)

The following is the list of modifications:

1. Added LX Voltage specification in the Absolute Maximum Ratings† section.
2. Updated Table 4-3.
3. Updated **Section 4.7 "Horn Test"**.

Revision B (January 2014)

The following is the list of modifications:

1. Updated the IRED on Time parameter condition in the "AC Electrical Characteristics" section.
2. Updated Register 4-1.
3. Updated **Section 4.7 "Horn Test"**.

Revision A (November 2013)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	T	X
Device	Package	Number of Pins	Tape and Reel	Lead Free

Device:	RE46C191:	CMOS Photoelectric Smoke Detector ASIC
	RE46C191T:	CMOS Photoelectric Smoke Detector ASIC (Tape and Reel)
Package:	SL =	Plastic Small Outline – Narrow, 3.90 mm Body, 16-Lead (SOIC)
	SS =	Plastic Shrink Small Outline – 5.30 mm Body, 20-Lead (SSOP)

Examples:

a) RE46C191S16F: 16-Lead SOIC Package, Lead Free

b) RE46C191S16TF: 16-Lead SOIC Package, Tape and Reel, Lead Free

c) RE46C191SS20: 20-Lead SSOP Package

d) RE46C191SS20T: 20-Lead SSOP Package, Tape and Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with Microchip for package availability with the Tape and Reel option.

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