



Helping Customers Innovate, Improve & Grow




VC-806

### Description

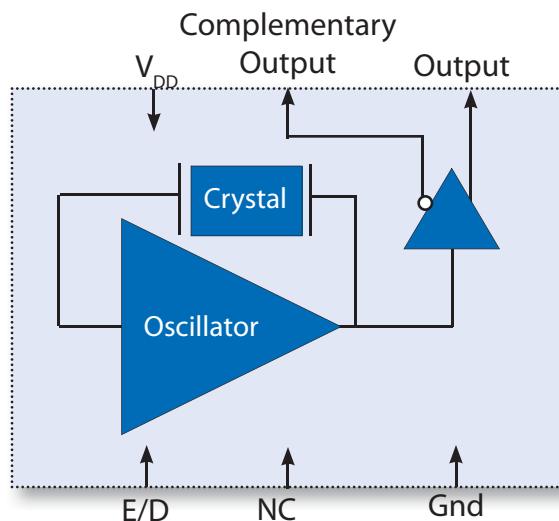
Vectron's VC-806 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 2.5 volt supply in a hermetically sealed 3.2x5 ceramic package.

### Features

- Ultra Low Jitter Performance, Fundamental or 3rd OT Crystal Design
- 156.250 Output Frequency
- <0.8 ps RMS jitter, 12kHz-20MHz
- Differential Output
- Enable/Disable
- -40/100°C Operation
- Hermetically Sealed 3.2x5 Ceramic Package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

### Applications

### Block Diagram



# Performance Specifications

Table 1. Electrical Performance					
Parameter	Symbol	Min	Typ	Max	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	2.375	2.5	2.625	V
Current (No Load)	$I_{DD}$			60	mA
<b>Frequency</b>					
Nominal Frequency	$f_N$		156.250		MHz
Stability <sup>2</sup> (Ordering Option)				±100	ppm
<b>Outputs</b>					
Output Logic Levels <sup>3</sup> Output Logic High Output Logic Low	$V_{OH}$ $V_{OL}$	0.9	1.43 1.10	1.6	V
Output Swing		247	330	454	mV
Differential Output Swing		494	660	908	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current				10	uA
Output Rise and Fall Time <sup>4</sup> Rise Time Fall Time	$t_R$ / $t_F$			600 600	ps ps
Load		100 ohms differential			
Duty Cycle <sup>4</sup>		45	50	55	%
Jitter (12 kHz - 20 MHz BW) <sup>5</sup>	$\phi J$		0.35	0.8	ps
Period Jitter <sup>6</sup> RMS P/P	$\phi J$		2.9 25.1		ps ps
Random Jitter	$R_J$		2.9		ps
Deterministic Jitter	$D_J$		<0.2		ps
<b>Enable/Disable</b>					
Output Enabled <sup>7</sup> Output Disabled	$V_{IH}$ $V_{IL}$	$0.7 * V_{DD}$		$0.3 * V_{DD}$	V V
Enable/Disable Time	$t_D$			200	ns
Enable/Disable Leakage Current				±200	uA
Enable Pull-Up Resistor Output Enabled Output Disabled			33 1		KOhm MOhm
Start-Up Time	$t_{SU}$			10	ms
Operating Temp. (Ordering Option)	$T_{OP}$	-40		100	°C
Package Size		3.2x5.0x1.3			mm

1. The VC-806 power supply pin should be filtered, eg, a 0.1 and 0.01 uF capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines these parameters and Figure 2 defines the test circuit.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052, 156.250MHz.
6. Measured using a Wavecrest SIA3300C, 90K samples.
7. Outputs will be Enabled if Enable/Disable is left open.

# Test Diagrams

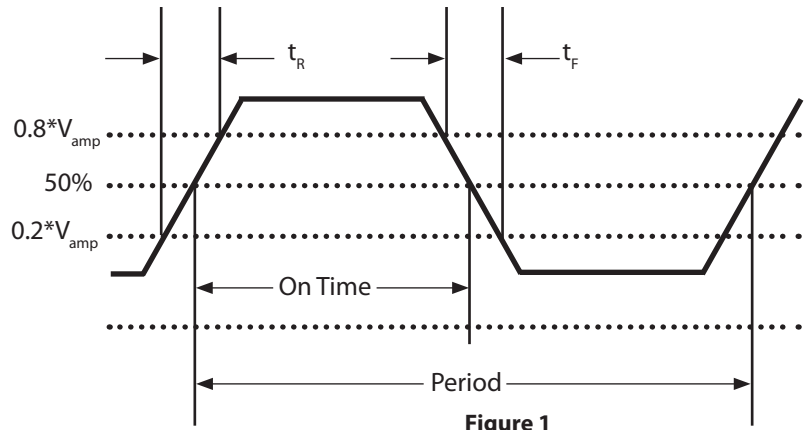


Figure 1

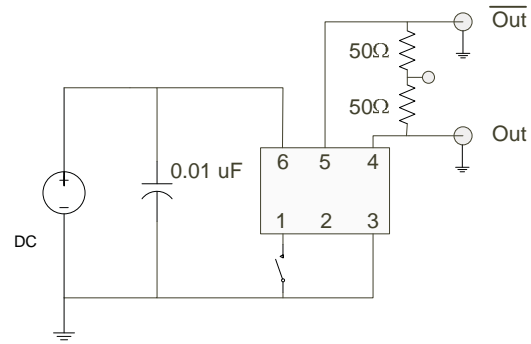


Figure 2

# Package and Pinout

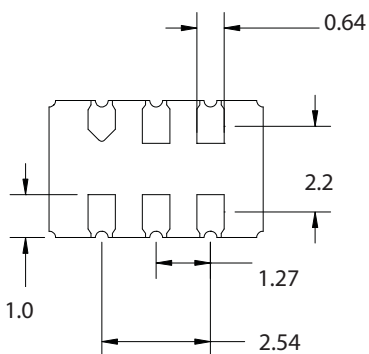
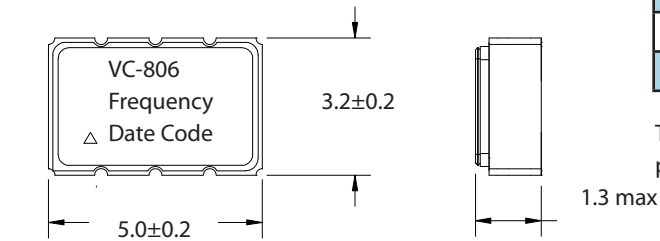


Figure 3 Package Dimensions in mm

Pin #	Symbol	Function
1	E/D	Enable Disable
2	NC	No Connection
3	GND	Electrical and Lid Ground
4	$f_o$	Output Frequency
5	$Cf_o$	Complementary Output Frequency
6	$V_{DD}$	Supply Voltage

The Enable/Disable function is set at the factory on either pin 1 or pin 2 and is an ordering option.

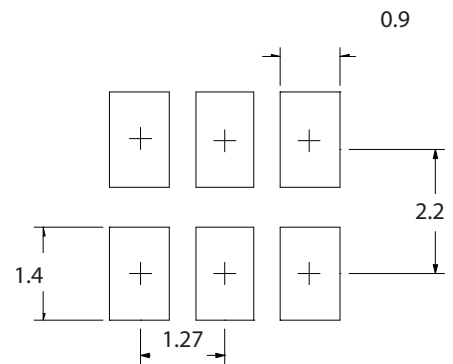
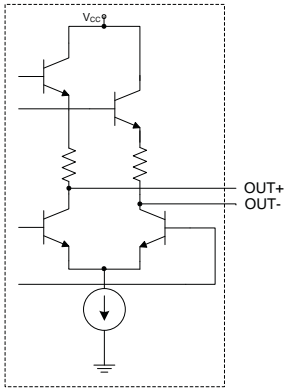
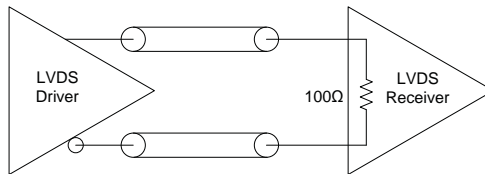


Figure 4 Pad Layout Dimensions in mm

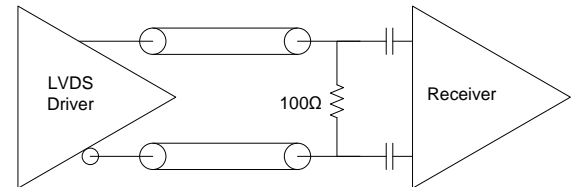
## LVDS Application Diagrams



**Figure 5 Standard LVDS Output Configuration**



**Figure 6 LVDS to LVDS Connection, Internal 100ohm**  
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.



**Figure 7 LVDS to LVDS Connection External 100ohm and AC blocking caps**  
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## Environmental and IR Compliance

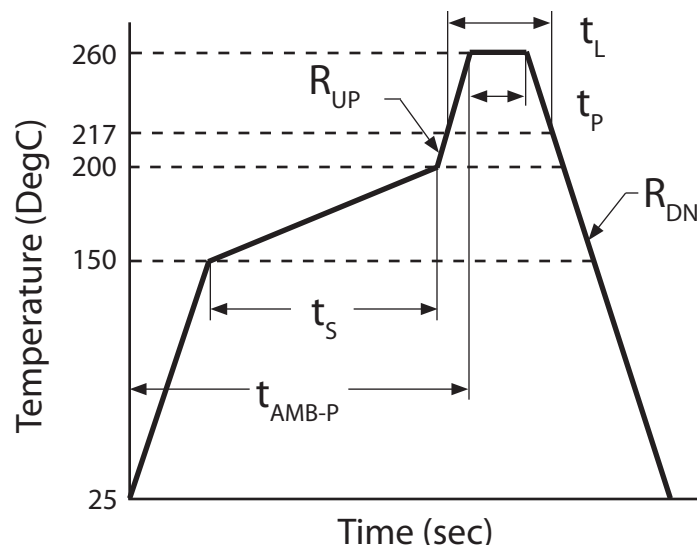
Table 3. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel

## IR Compliance

### Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 4. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Parameter	Symbol	Value
PreHeat Time	$t_s$	200 sec Max
Ramp Up	$R_{UP}$	3°C/sec Max
Time above 217°C	$t_L$	150 sec Max
Time to Peak Temperature	$t_{AMB-P}$	480 sec Max
Time at 260°C	$t_p$	20 sec Max
Time at 240°C	$t_{P2}$	60 sec Max
Ramp down	$R_{DN}$	6°C/sec Max



## Maximum Ratings, Tape & Reel

### Absolute Maximum Ratings and Handling Precautions

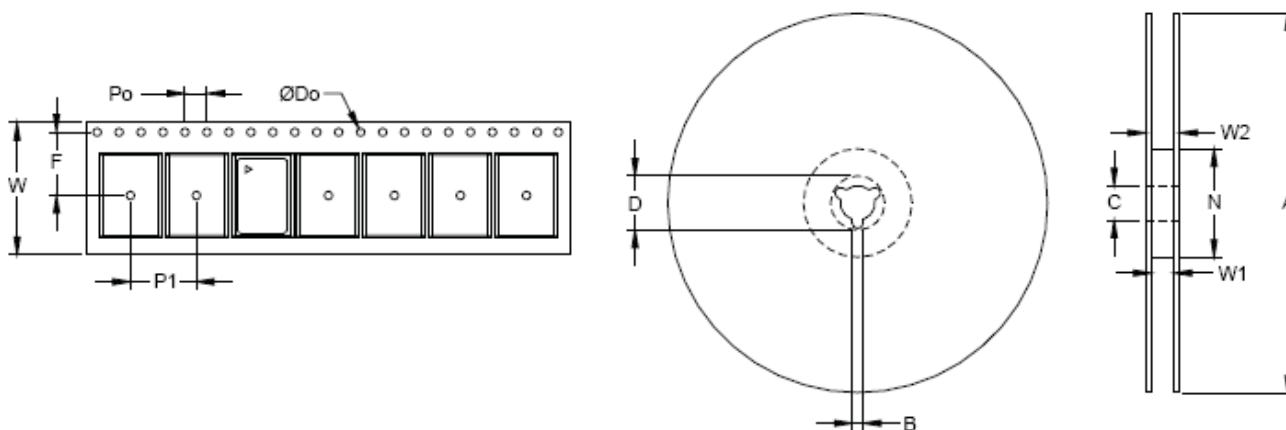
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VC-806, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Parameter	Symbol	Rating	Unit
Storage Temperature	$T_{STORE}$	-55/125	°C
Supply Voltage	$V_{DD}$	-0.5 to 5.0	V
Enable Disable Voltage	E/D	-0.5 to $V_{DD}+0.5$	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

**Table 6. Tape and Reel Information**

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	60	17	21	250



## Ordering Information

**VC-806- 0001 - 156M250000**

**Product**

XO

**Package**

3.2x5mm

**SCD Number**

**Frequency in MHz**

## For Additional Information, Please Contact

### **USA:**

Vectron International  
267 Lowell Road  
Hudson, NH 03051  
Tel: 1.888.328.7661  
Fax: 1.888.329.8328

### **Europe:**

Vectron International  
Landstrasse, D-74924  
Neckarbischofsheim, Germany  
Tel: +49 (0) 3328.4784.17  
Fax: +49 (0) 3328.4784.30

### **Asia:**

VI Shanghai  
1589 Century Avenue, the 19th Floor  
Chamtime International Financial Center  
Shanghai, China  
Tel: 86.21.6081.2888  
Fax: 86.21.6163.3598

### **Disclaimer**

Vectron International reserves the right to make changes to the product(s) and or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information.

Rev: 09/23/2011