

**FEATURES**

- Single 3.3V or 5V power supply
- Up to 3.2Gbps operation
- Low noise PECL data outputs
- Chatter-free open collector TTL LOS output
- TTL /EN Input
- Differential PECL inputs for data
- Available in a tiny 10-pin (3mm) MSOP and 10-pin (3mm) EPAD-MSOP

**APPLICATIONS**

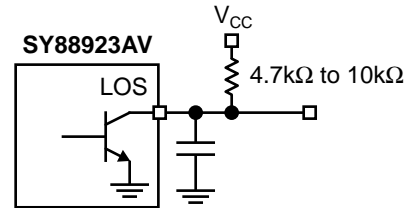
- 1.25Gbps and 2.5Gbps Gigabit Ethernet
- 531Mbps, 1062Mbps and 2.12Gbps Fibre Channel
- 622Mbps SONET
- Gigabit interface converter
- 2.5Gbps SDH/SONET
- 2.5Gbps proprietary links
- Parallel 10G Ethernet

**DESCRIPTION**

The SY88923AV limiting post amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 3.2Gbps. Signals as small as  $5mV_{PP}$  can be amplified to drive devices with PECL inputs. The SY88923AV generates a chatter-free Loss-of-Signal (LOS) open collector TTL output.

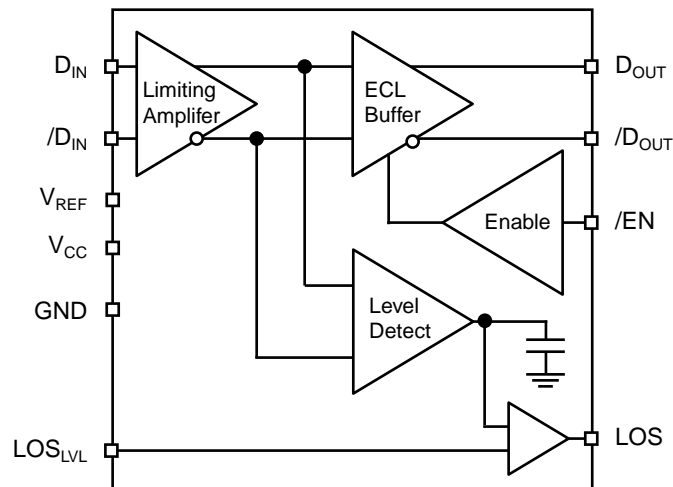
The SY88923AV incorporates a programmable level detect function to identify when the input signal has been lost. The LOS output will change from logic "LOW" to logic "HIGH" when input signal is smaller than the swing set by  $LOS_{LVL}$ . This information can be fed back to the EN input of the device to maintain stability under loss-of-signal condition. Using  $LOS_{LVL}$  pin, the sensitivity of the level detection can be adjusted. The  $LOS_{LVL}$  voltage can be set by connecting a resistor divider between  $V_{CC}$  and  $V_{REF}$  shown in Figure 3. "Typical Operating Characteristics" on page 6 show the relationship between input level sensitivity and the voltage set on  $LOS_{LVL}$ .

The LOS output is a TTL open collector output that requires a pull-up resistor for proper operation, Figure 1.

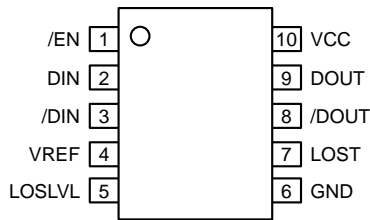


**Figure 1. LOS Output with Desired Rise Time**

**BLOCK DIAGRAM**



## PACKAGE/ORDERING INFORMATION



**10-Pin MSOP (K10-1)**  
**10-Pin EPAD-MSOP (K10-2)**

## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88923AVKC	K10-1	Commercial	923AV	Sn-Pb
SY88923AVKCTR <sup>(2)</sup>	K10-1	Commercial	923AV	Sn-Pb
SY88923AVEC	K10-2	Commercial	923AV	Sn-Pb
SY88923AVECTR <sup>(2)</sup>	K10-2	Commercial	923AV	Sn-Pb
SY88923AVKG <sup>(3)</sup>	K10-1	Industrial	923AV with Pb-free bar-line indicator	NiPdAu Pb-Free
SY88923AVKGTR <sup>(2, 3)</sup>	K10-1	Industrial	923AV with Pb-free bar-line indicator	NiPdAu Pb-Free
SY88923AVEY <sup>(3)</sup>	K10-2	Industrial	923AV with Pb-free bar-line indicator	Matte-Sn Pb-Free
SY88923AVEYTR <sup>(2, 3)</sup>	K10-2	Industrial	923AV with Pb-free bar-line indicator	Matte-Sn Pb-Free

### Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

## PIN DESCRIPTION

Pin Number MSOP	Pin Number EPAD-MSOP	Pin Name	Type	Pin Function
1	1	/EN	TTL Input	Output Enable (Active Low).
2	2	DIN	Data Input	Data Input.
3	3	/DIN	Data Input	Inverting Data Input.
4	4	VREF	Output	Reference Voltage Output for LOS Level Set (see Figure 3).
5	5	LOSLVL	Input	LOS Limit Set.
6	6, (Exposed Pad)	GND	Ground	Ground. Exposed pad must be connected to PCB ground plane.
7	7	LOS	TTL Output (Open Collector)	Loss of Signal Indicator (Active High).
8	8	/DOUT	PECL Output	Inverting Data Output.
9	9	DOUT	PECL Output	Data Output.
10	10	VCC	Power Supply	Positive Power Supply.

**Absolute Maximum Ratings<sup>(1)</sup>**

Power Supply Voltage ( $V_{CC}$ )	0V to +7.0V
Input Voltage	
( $D_{IN}$ , $/D_{IN}$ )	0V to $V_{CC}$
( $/EN$ )	0V to $V_{CC}$
( $LOS_{LVL}$ )	0V to $V_{CC}$
Output Voltage (with 50 $\Omega$ load)	
( $D_{OUT}$ , $/D_{OUT}$ )	$V_{CC} - 2.5V$ to $V_{CC} + 0.3V$
( $V_{REF}$ )	$V_{CC} - 2.0V$ to $V_{CC}$
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature ( $T_S$ )	-55°C to +125°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ )	+3.0V to +5.5V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance	
MSOP ( $\theta_{JA}$ )	
Still-Air	113°C/W
EPAD-MSOP ( $\theta_{JA}$ )	
Still-Air	38°C/W

**DC ELECTRICAL CHARACTERISTICS<sup>(3)</sup>**

$V_{CC} = +5V \pm 10\%$  or  $+3.3V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	No output load		38	60	mA
		$V_{CC} = 5V \pm 10\%$ , $V_{CC} = 3.3V \pm 10\%$		35	53	mA
$I_{IL}$	$/EN$ Input LOW Current	$V_{IN} = 0.5V$	-0.3			mA
$I_{IH}$	$/EN$ Input HIGH Current	$V_{IN} = 2.7V$			20	$\mu\text{A}$
		$V_{IN} = V_{CC}$			100	$\mu\text{A}$
$V_{CMR}$	Common Mode Range		GND +2.0		$V_{CC}$	V
$V_{offset}$	Differential Output Offset				$\pm 80$	mV
$LOS_{LVL}$	$LOS_{LVL}$ Level		$V_{REF}$		$V_{CC}$	V
$V_{OL}$	LOS Output LOW Level	$I_{OL} = +2\text{mA}$			0.5	V
$I_{OH}$	LOS Output Leakage	$V_{OH} = 5.5V$			100	$\mu\text{A}$
$V_{OH}$	$D_{OUT}$ and $/D_{OUT}$ Output HIGH Voltage		$V_{CC} - 1085$	$V_{CC} - 955$	$V_{CC} - 880$	mV
$V_{OL}$	$D_{OUT}$ and $/D_{OUT}$ Output LOW Voltage		$V_{CC} - 1830$	$V_{CC} - 1705$	$V_{CC} - 1555$	mV
$V_{REF}$	Reference Supply		$V_{CC} - 1.38$	$V_{CC} - 1.32$	$V_{CC} - 1.26$	V
$I_{REF}$	$V_{REF}$ Output Current		-0.8		0.5	mA
$V_{IH}$	$/EN$ Input HIGH Voltage		2.0			V
$V_{IL}$	$/EN$ Input LOW Voltage				0.8	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of  $\geq 500\text{fpm}$  is maintained.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V \pm 10\%$  or  $+3.3V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{ID}$	Input Voltage Range		5		1800	mV <sub>PP</sub>
$V_{OD}$	Differential Output Voltage Swing	<b>Note 4</b> $V_{ID} = 15mV_{PP}$ $V_{ID} = 5mV_{PP}$		1400 600		mV <sub>PP</sub> mV <sub>PP</sub>
$t_{ON}$	LOS Assert Time	<b>Note 5</b>		0.2	0.5	$\mu s$
$t_{OFF}$	LOS Release Time	<b>Note 5</b>		0.1	0.5	$\mu s$
$V_{SR}$	LOS Sensitivity Range	2 <sup>23</sup> -1 pattern	5		50	mV <sub>PP</sub>
HYS	LOS Hysteresis	2 <sup>23</sup> -1 pattern	2	4.6	8	dB
$t_r, t_f$	Output Rise/Fall Time	$V_{ID} > 100mV_{PP}$ $V_{ID} < 100mV_{PP}$		115 $t_{rin}, t_{fin}$	150	ps

### Notes:

4. Input is a 200MHz square wave,  $t_r < 300ps$ .
5. Input is a 200MHz square wave,  $t_r < 300ps$ ,  $1.8V_{PP}$ .

## GENERAL DESCRIPTION

### General

The SY88923AV is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical trans-impedance amplifiers found within a fiber-optics link. The linear signal output from a trans-impedance amplifier can contain significant amounts

of noise, and may vary in amplitude over time. The SY88923AV limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The /EN pin allows the user to disable the output signal without removing the input signal.

## DESIGN PROCEDURE

### Output Termination

The SY88923AV outputs must be terminated with a 50Ω load to  $V_{CC} - 2V$  (or Thevenin equivalent).

### Layout and PCB Design

Since the SY88923AV is a high-frequency component, performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply.

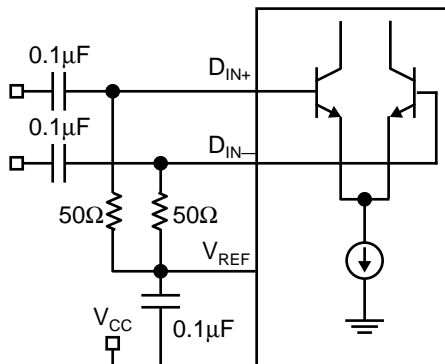


Figure 2. Differential Input Configuration

The SY88923AV ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

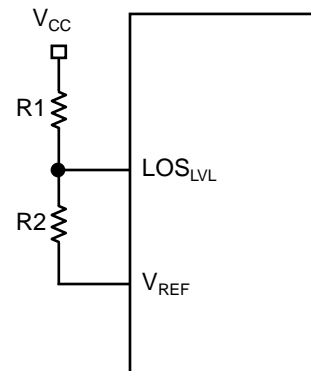
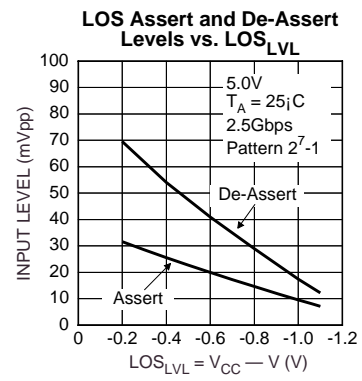
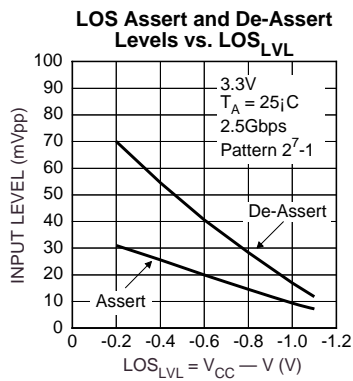
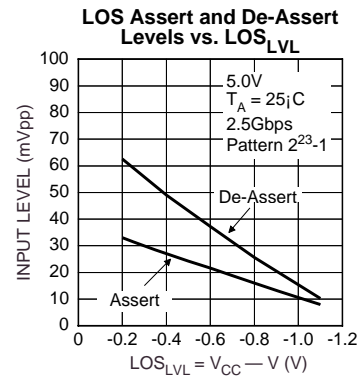
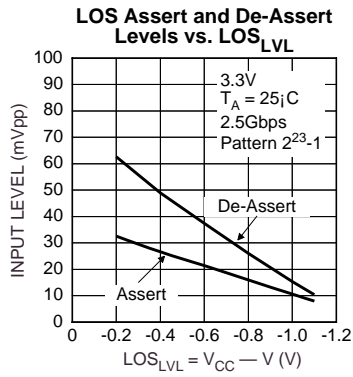


Figure 3. LOS<sub>LVL</sub> Circuit

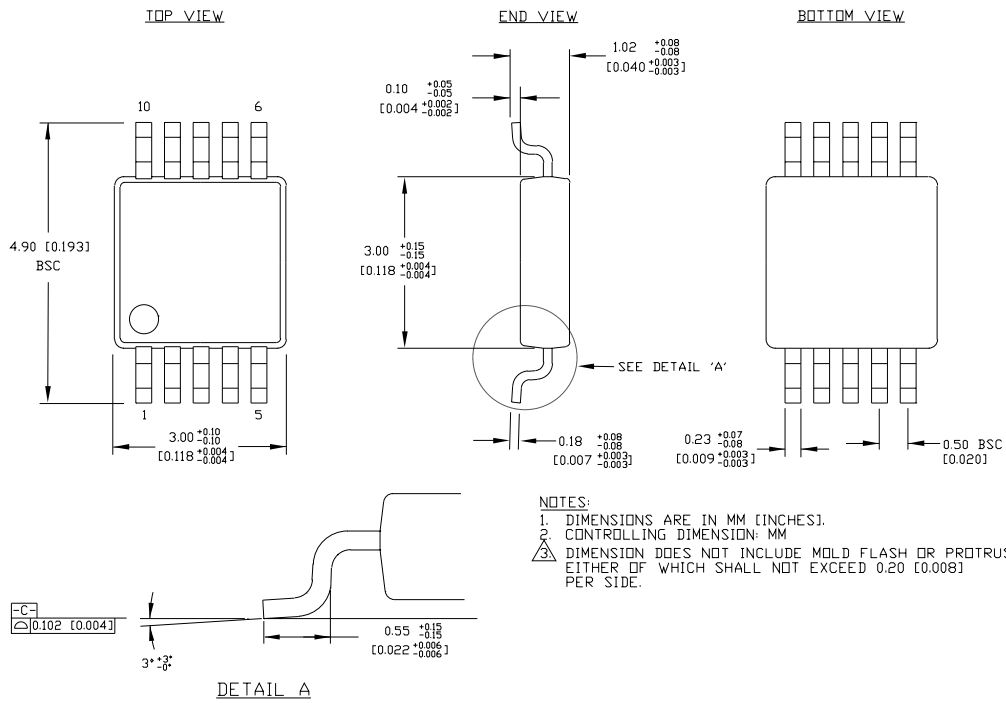
**Note 1.** 
$$LOS_{LVL} = V_{CC} - 1.32V + \frac{R2 \times 1.32V}{R1 + R2}$$
  

$$R1 + R2 \geq 2.6k\Omega$$

**TYPICAL OPERATING CHARACTERISTICS**

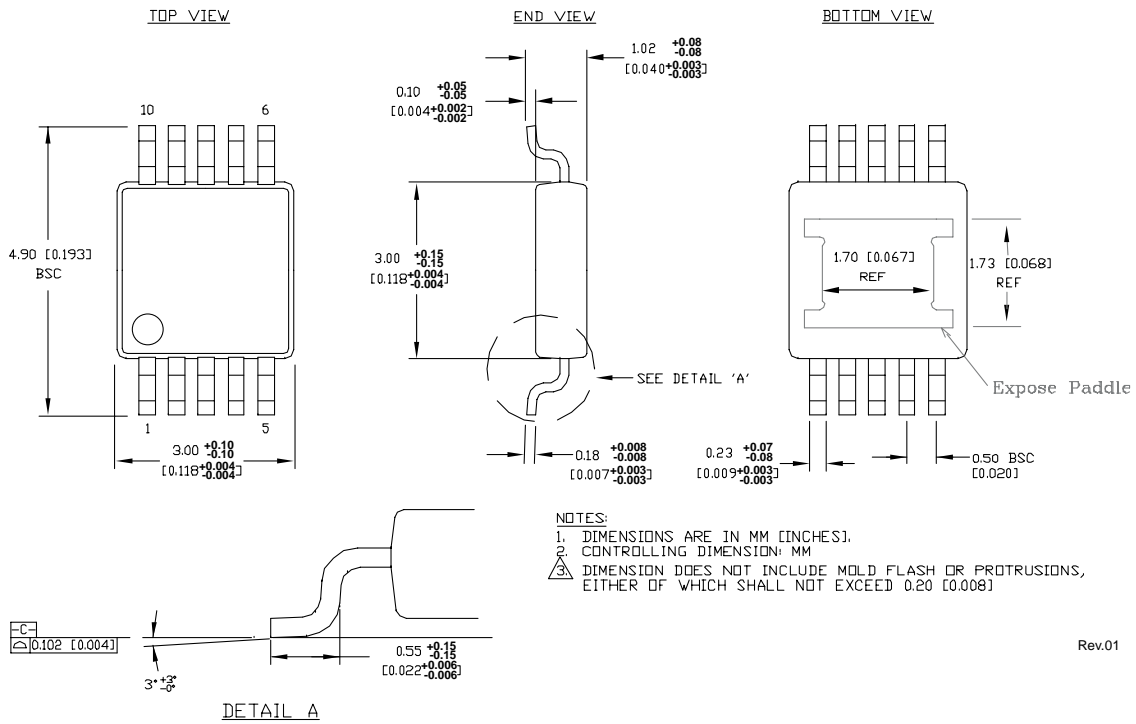


**10-PIN MSOP (K10-1)**



Rev. 00

**10-PIN EPAD-MSOP (K10-2)**



Rev.01

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