MIC4950

Hyper Speed Control™ 5A Buck Regulator

General Description

The MIC4950 is a high-efficiency, 5A synchronous buck regulator with ultra-fast transient response. It is perfectly suited for supplying processor core and I/O voltages from a 5V or 3.3V bus. The MIC4950 provides a switching frequency up to 3.3MHz while achieving peak efficiencies up to 95%. An additional benefit of high-frequency operation is very low output ripple voltage throughout the entire load range with the use of a small output capacitor. The MIC4950 is designed for use with a very small inductor, down to 1µH, and an output ceramic capacitor as small as 10µF, without the need for external ripple injection. A wide range of output capacitor types and values can also be accommodated.

The MIC4950 supports safe start-up into a pre-biased output, and offers short-circuit and thermal shutdown protections.

The MIC4950 is available in 8-Pin SOIC and 10-Pin 3mm × 4mm DFN packages with an operating junction temperature range from –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

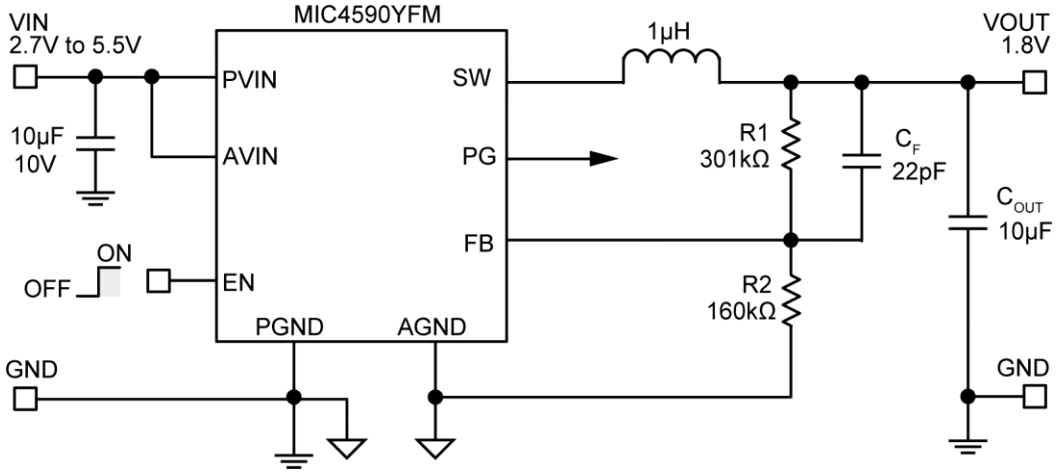
Features

- Input voltage: 2.7V to 5.5V
- 5A output current
- Up to 95% efficiency
- Up to 3.3MHz operation
- Safe start-up into a pre-biased output
- Power Good output
- Ultra-fast transient response
- Low output voltage ripple
- Low R_{DSON} integrated MOSFET switches
- 0.01µA shutdown current
- Thermal shutdown and current limit protection
- Output voltage as low as 0.7V
- 8-Pin SOIC and 3mm × 4mm DFN-10L
- –40°C to +125°C junction temperature range

Applications

- DTVs
- Set-top boxes
- Printers
- DVD players
- Distributed power supplies

Typical Application



Hyper Speed Control is a trademark of Micrel, Inc.

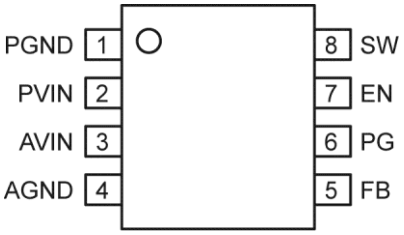
Ordering Information

Part Number[1]	Top Mark	Temperature Range	Package	Lead Finish
MIC4950YFM	4950YFM	–40°C ≤ T_J ≤ +125°C	8-pin SOIC	Pb-Free
MIC4950YFL	MIC4950	–40°C ≤ T_J ≤ +125°C	10-pin 3mm x 4mm DFN[2]	Pb-Free

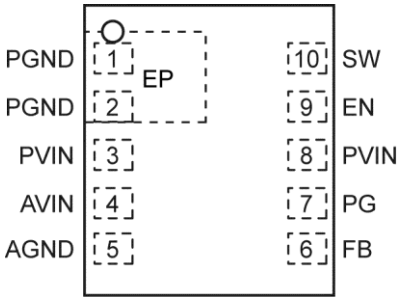
Note:

1. Other options are available. Contact Micrel for details.
2. DFN is GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



8-Pin SOIC (FM)
(Top View)



3mm x 4mm DFN (FL)
(Top View)

Pin Description

Pin Number SOIC-8 (YFM)	Pin Number DFN-10 (YFL)	Pin Name	Pin Function
1	1, 2, EP	PGND	Power Ground.
2	3, 8	PVIN	Power Input Voltage: Connect a 10µF ceramic capacitor between PVIN and PGND for input decoupling. Pins 3 and 8 are internally connected in the DFN-10 package.
3	4	AVIN	Analog Input Voltage: Connect a 1µF ceramic capacitor between AVIN and AGND to decouple the noise from the internal reference and error comparator.
4	5	AGND	Analog Ground Input: Connect to a quiet ground plane for best operation. Do not route power switching currents on the AGND net. Connect AGND and PGND nets together at a single point.
5	6	FB	Feedback (Input): Connect an external divider between VOUT and AGND (Analog Ground) to program the output voltage.
6	7	PG	Power Good (Output): Open-drain output. A pull-up resistor from this pin to a voltage source is required to detect an output power-is-good condition.
7	9	EN	Enable (Input): Logic high enables operation of the regulator. Logic low shuts down the device. Do not leave floating.
8	10	SW	Switch (Output): Internal power MOSFET output switches.

Absolute Maximum Ratings[3]

PVIN, AVIN Supply Voltage (V_{IN}) ..... –0.3V to 6V
SW Output Switch Voltage (V_{SW}) ..... –0.3V to V_{IN}
EN, PG (V_{EN}, V_{PG}) ..... –0.3V to V_{IN}
FB Feedback Input Voltage (V_{FB}) ..... –0.3V to V_{IN}
Storage Temperature Range ..... –65°C to +150°C
ESD Rating[5] ..... 2kV, HBM

Operating Ratings[4]

Supply Voltage (V_{IN}) ..... 2.7V to 5.5V
Enable Input Voltage (V_{EN}) ..... 0V to VIN
Junction Temperature Range (T_J) ..... –40°C ≤ T_J ≤ +125°C
Thermal Resistance
SOIC-8 (θ_{JA}) ..... 120°C/W
DFN-10 (θ_{JA}) ..... 35°C/W

Electrical Characteristics[6]

V_{IN} = V_{EN} = 3.3V; L = 1.0µH; C_{IN} = 10µF; C_{OUT} = 10µF; T_A = 25°C, **bold** values indicate –40°C≤ T_J ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage Range		**2.7**		**5.5**	V
V_{UVLO}	Under-Voltage Lockout Threshold	Turn-On	**2.41**	2.5	**2.61**	V
V_{UVLOH}	Under-Voltage Lockout Hysteresis			400		mV
I_Q	Quiescent Current	I_{OUT} = 0mA , FB > 1.2*$V_{FB\ (Nominal)}$		0.8	**2**	mA
I_{SD}	Shutdown Current	V_{EN} = 0V		0.01	**2**	µA
V_{FB}	Feedback Voltage		**0.609**	0.625	**0.64**	V
I_{LIMIT}	Current Limit	FB = 0.9*$V_{FB\ (Nominal)}$	5.5	7.5	10	A
LINEREG	Output Voltage Line Regulation	V_{IN} = 2.7 to 3.5V, V_{OUTNOM} = 1.8V, I_{LOAD} = 20mA		1		%/V
		V_{IN} = 4.5V to 5.5V if V_{OUTNOM} ≥ 2.5V, I_{LOAD} = 20mA				
LOADREG	Output Voltage Load Regulation	20mA < I_{LOAD} < 500mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V		0.3		%
		20mA < I_{LOAD} < 500mA, V_{IN} = 5.0V if V_{OUTNOM} ≥ 2.5V				
		20mA < I_{LOAD} < 5A, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V		1		%
		20mA < I_{LOAD} < 5A, V_{IN} = 5.0V if V_{OUTNOM} ≥ 2.5V				
R_{DSON-P}	PWM Switch ON-Resistance	I_{SW} = 1A P-Channel MOSFET		30		Ω
R_{DSON-N}		I_{SW} = –1A N-Channel MOSFET		25		
t_{ON}	Maximum Turn-On Time	V_{IN} = 4.5V, V_{FB} = 0.5V		665		ns
		V_{IN} = 3.0V, V_{FB} = 0.5V		1000		
		V_{IN} = 2.7V, V_{FB} = 0.5V		1120		
t_{OFF}	Minimum Turn-Off Time	V_{IN} = 3.0V, V_{FB} = 0.5V		176		ns
$t_{SOFT-ON}$	Soft Start Time	V_{OUT} = 90% of V_{OUTNOM}		500		µs
V_{EN}	Enable Threshold	Turn-On	**0.5**	0.8	**1.2**	V

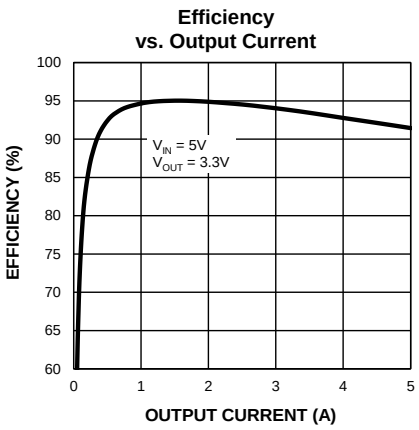
Notes:

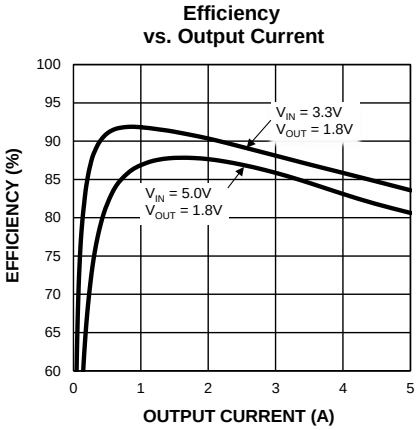
3. Exceeding the absolute maximum ratings may damage the device.
4. The device is not guaranteed to function outside its operating ratings.
5. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
6. Specification for packaged product only.

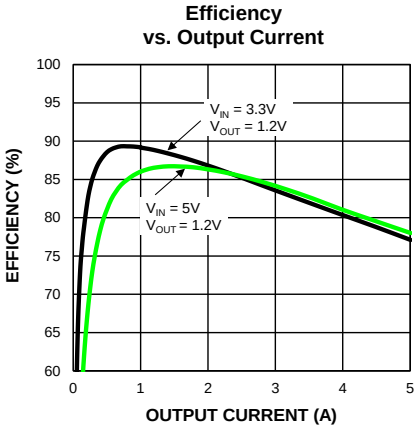
Electrical Characteristics[6] (Continued)

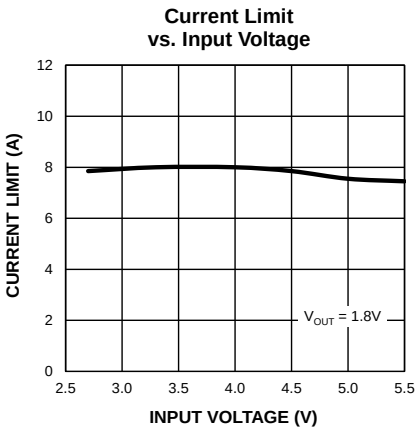
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{EN}	Enable Input Current			0.1	**1**	µA
V_{OUTPG}	Power Good Threshold	Rising	**82**	88	**94**	%
V_{OUTPGH}	Power Good Hysteresis			7		%
T_{SD}	Overtemperature Shutdown			150		°C
T_{SDH}	Overtemperature Shutdown Hysteresis			20		°C

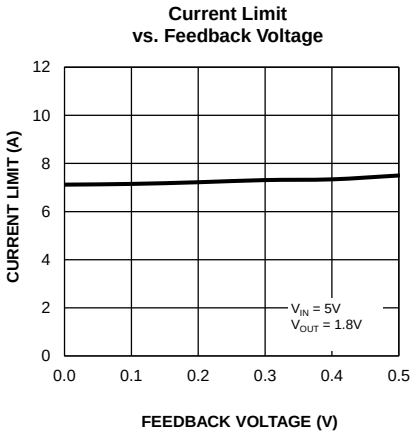
Typical Characteristics

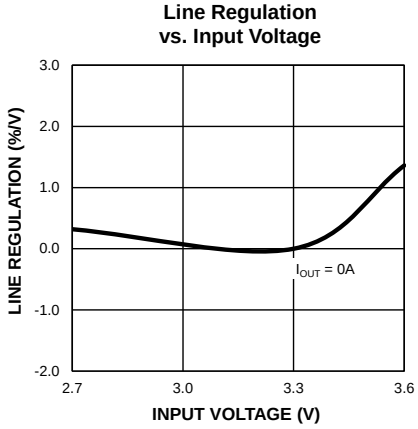


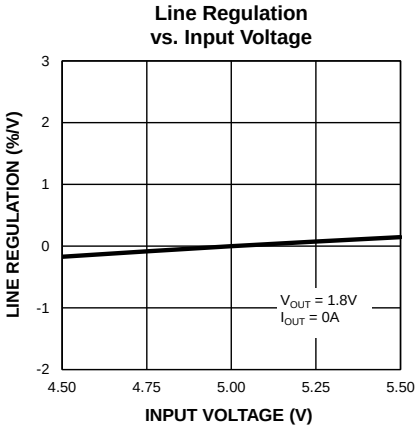


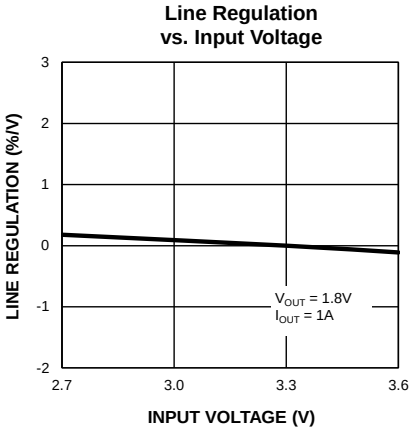


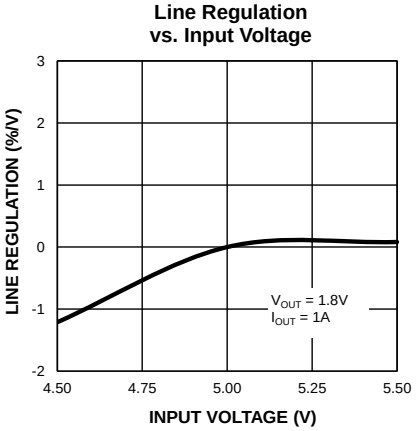






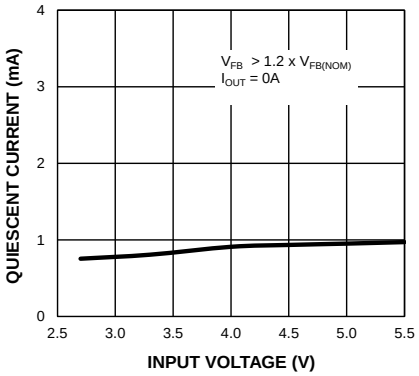




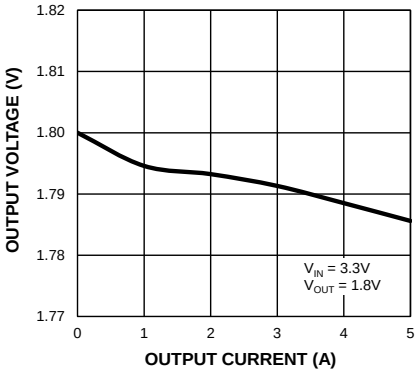


Typical Characteristics (Continued)

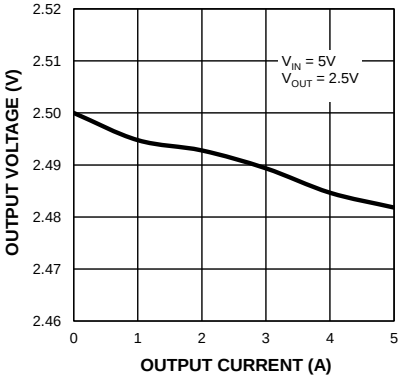
Quiescent Current vs. Input Voltage



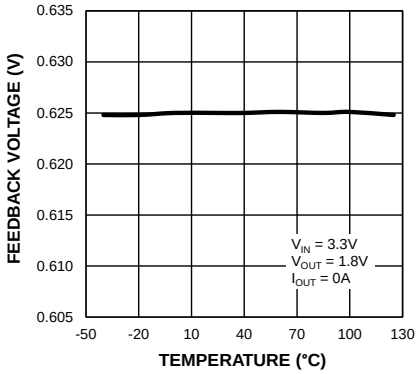
Output Voltage (V_{IN} = 3.3V) vs. Output Current



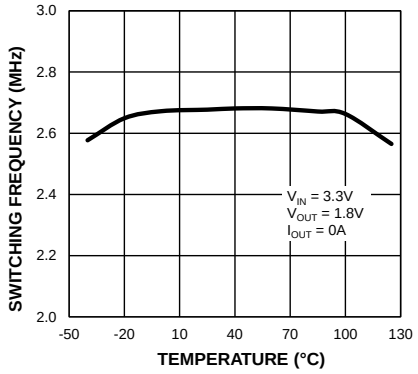
Output Voltage (V_{IN} = 5V) vs. Output Current



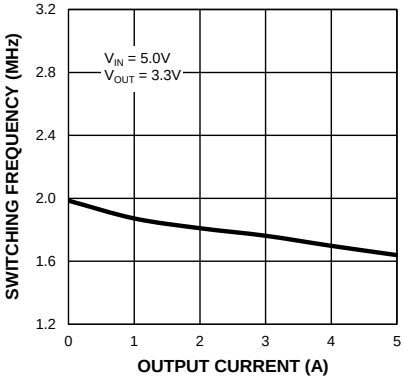
Feedback Voltage vs. Temperature



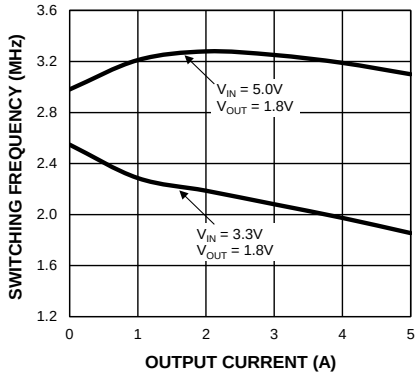
Switching Frequency vs. Temperature



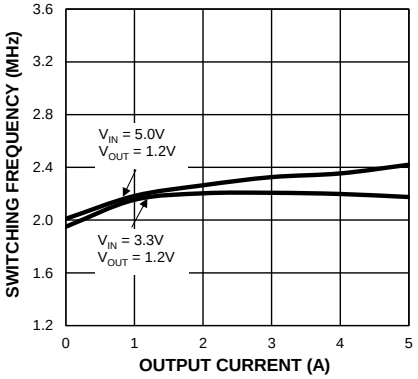
Switching Frequency vs. Output Current



Switching Frequency vs. Output Current

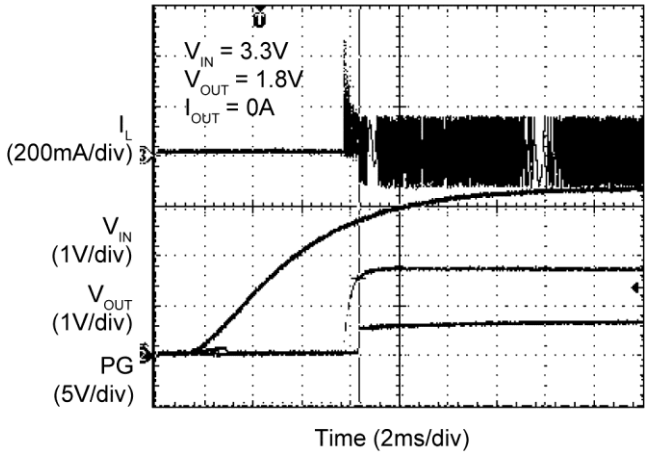


Switching Frequency vs. Output Current

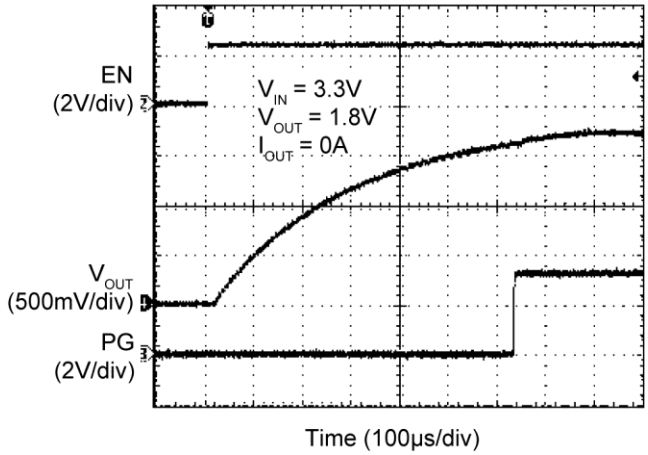


Functional Characteristics

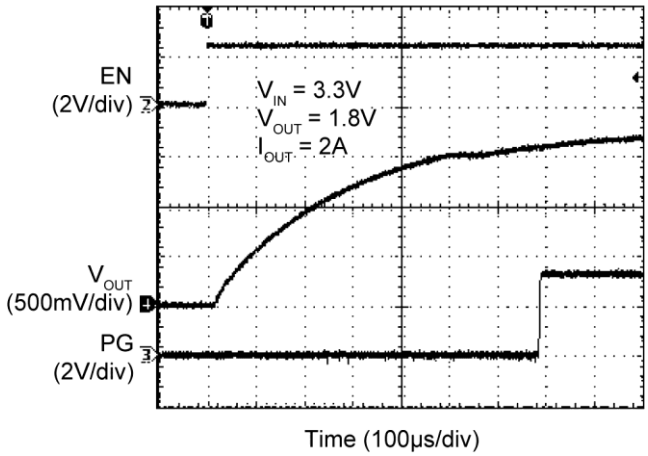
VIN Soft Turn-On



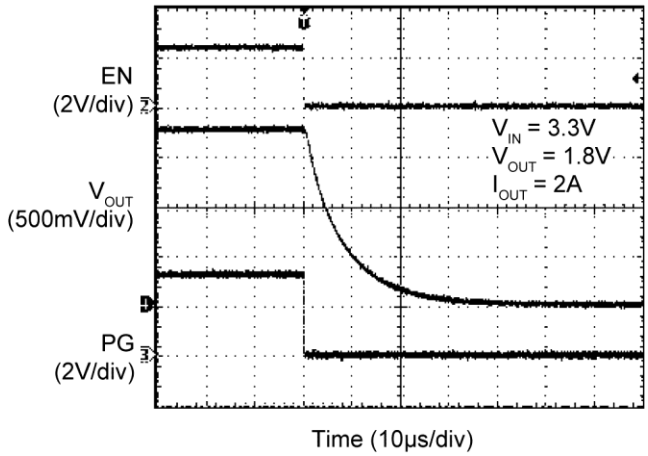
Enable Turn-On (No Load)



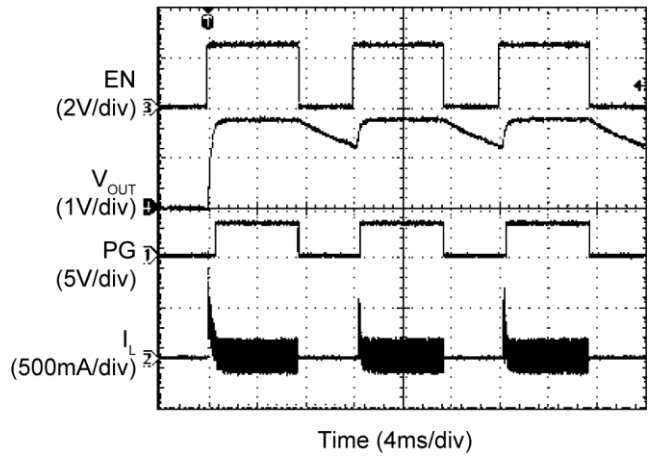
Enable Turn-On (2A Load)



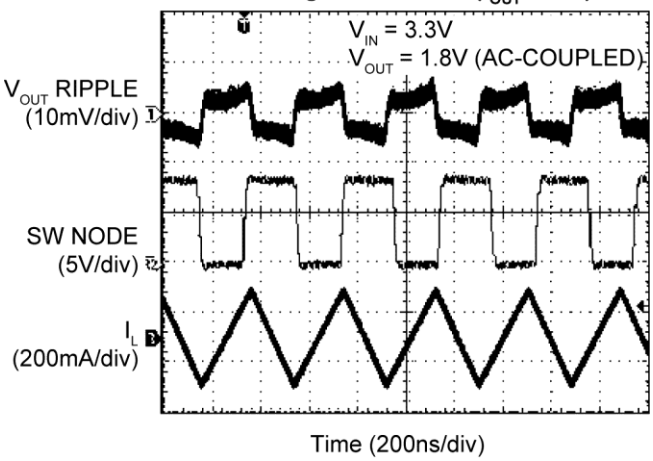
Enable Turn-Off (2A Load)



1.4V Prebias Start-Up (EN Rising)

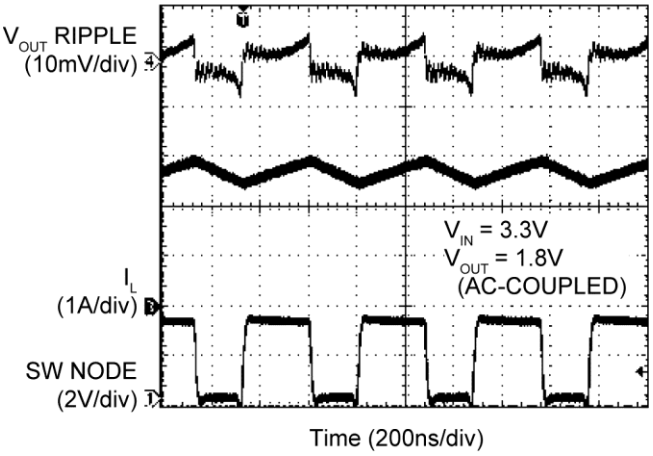


Switching Waveforms (I_{OUT} = 0A)

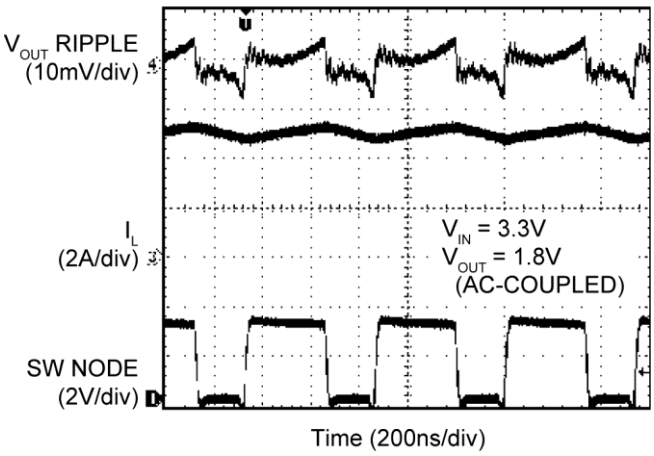


Functional Characteristics (Continued)

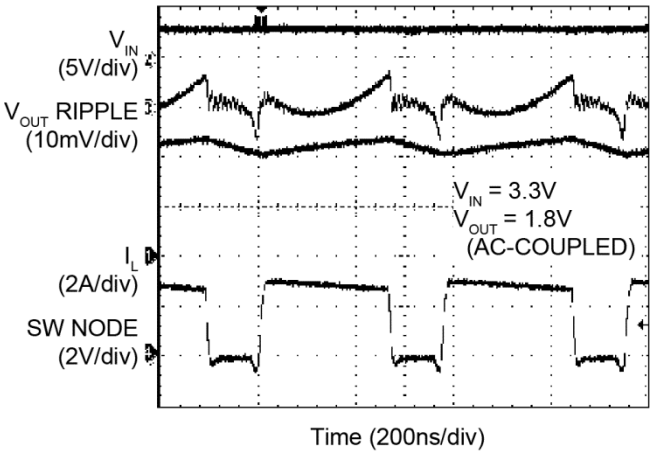
Switching Waveforms (I_{OUT} = 2.5A)



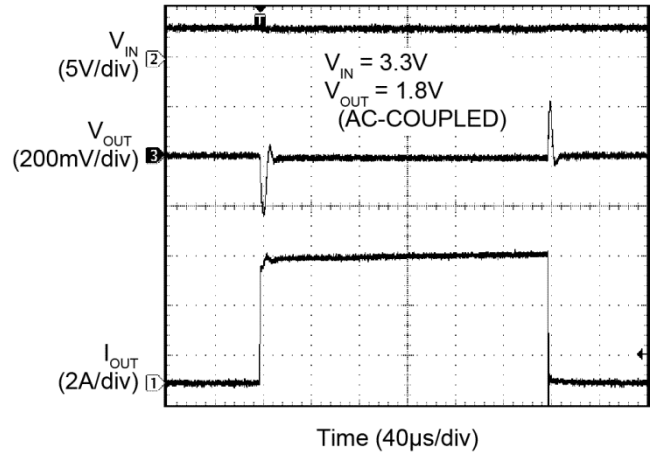
Switching Waveforms (I_{OUT} = 5A)



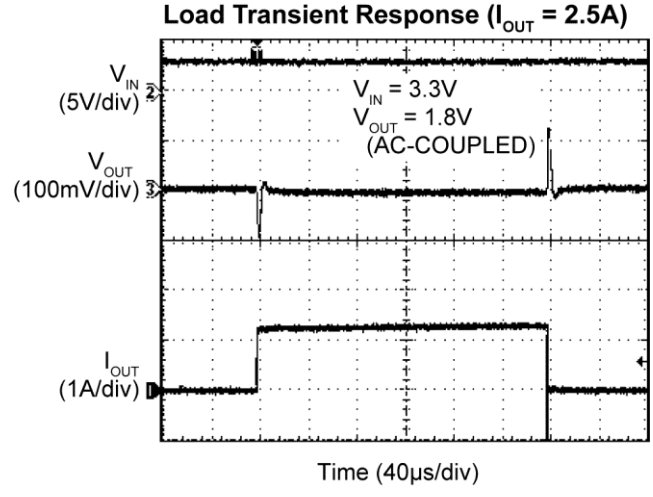
Switching Waveforms (Current Limit)



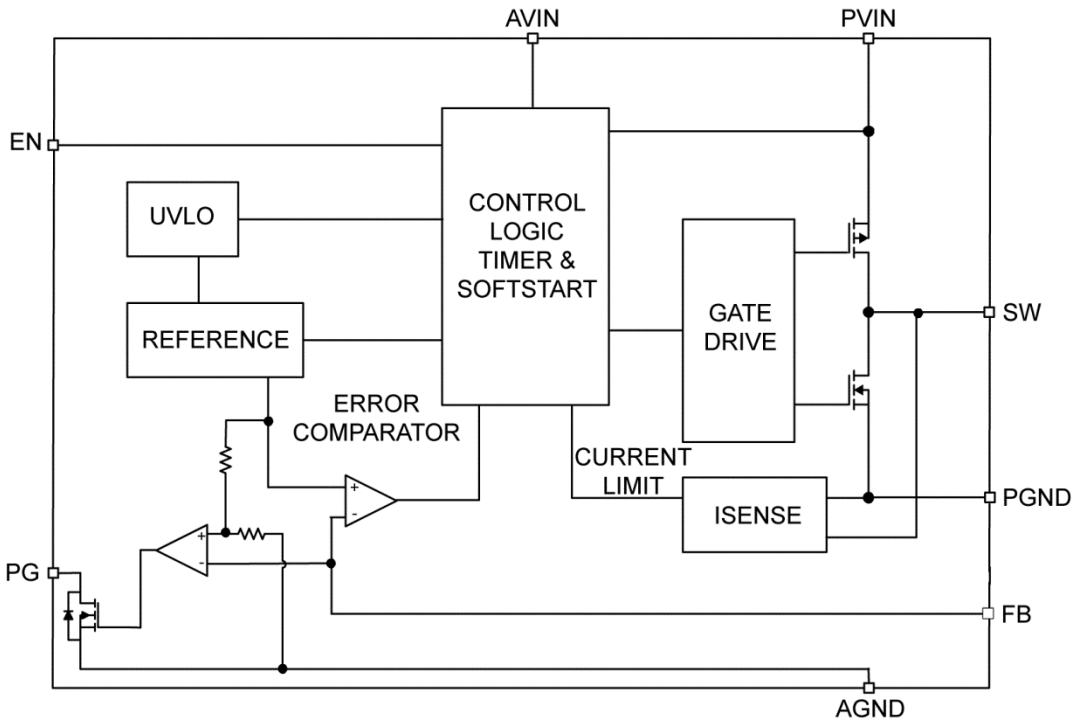
Load Transient Response (I_{OUT} = 5A)



Load Transient Response (I_{OUT} = 2.5A)



Functional Block Diagram



Functional Description

PVIN

The power input (PVIN) pin provides power to the internal MOSFETs for the switch mode regulator section of the MIC4950. The input supply operating range is from 2.7V to 5.5V. A low-ESR ceramic capacitor of at least 10µF is required for bypass from PVIN to (Power) GND. See the "Applications Information" section for further details.

AVIN

The analog power input (AVIN) pin provides power to the internal control and analog supply circuitry. Careful layout is important to ensure that high-frequency switching noise caused by PVIN is reduced before reaching AVIN. Always place a 1µF minimum ceramic capacitor very close to the IC between AVIN and AGND pins. For additional high-frequency switching noise attenuation, RC filtering can be used (R = 10Ω).

EN

A logic high signal on the enable (EN) pin activates the output of the switch. A logic low on the EN pin deactivates the output and reduces the supply current to the nominal 0.01µA. Do not leave this pin floating.

SW

The switch (SW) pin connects directly to one side of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes, whenever possible, to avoid unwanted injection of noise.

PGND

The power ground (PGND) is the ground return terminal for the high current in the switching node SW. The current loop for the PGND should be as short as possible and kept separate from the AGND net whenever applicable.

AGND

The analog ground (AGND) is the ground return terminal for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the "PCB Layout Recommendations" section for further details.

PG

The power-is-good (PG) pin is an open-drain output that indicates logic high when the output voltage is typically above 88% of its steady-state voltage. A pull-up resistor of 10kΩ or greater should be connected from PG to VOUT.

FB

To program the output voltage, an external resistive divider network is connected to this pin from the output voltage to AGND, as shown in the Typical Application circuit on page 1, and is compared to the internal 0.625V reference within the regulation loop. Equation 1 is used to program the output voltage:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 1}$$

Table 1 lists recommended feedback resistor values.

Table 1. Recommended Feedback Resistor Values

V_{OUT}	R1	R2
1.0V	120kΩ	180kΩ
1.2V	274kΩ	294kΩ
1.5V	316kΩ	226kΩ
1.8V	301kΩ	160kΩ
2.5V	316kΩ	105kΩ
3.3V	309kΩ	71.5kΩ

The feedforward capacitor (C_F in the Typical Application schematic) is typically in the range 22pF to 39pF. The MIC4950 features an internal ripple injection network, whose current is injected into the FB node and integrated by C_F, thus the waveform at FB is approximately a triangular ripple. The size of C_F dictates the amount of ripple amplitude at the FB node. Smaller values of C_F yield higher FB ripple amplitude and better stability, but also somewhat degrade line regulation and transient response.

Hyper Speed Control™

MIC4950 uses an ON- and OFF-time proprietary ripple-based control loop, which features three different timers:

- Minimum ON Time
- Maximum ON Time
- Minimum OFF Time

When the required duty cycle is very low, the required OFF time is typically far from the Minimum OFF Time limit (about 176 ns typ). In this case, the MIC4950 operates by delivering at each switching cycle a determined ON time (dependent on the input voltage). A new ON time is invoked by the error comparator when the FB voltage falls below the regulation threshold. In this mode the MIC4950 operates as an adaptive Constant-ON-Time ripple controller, with nearly constant switching frequency. Regulation takes place by controlling the valley of the FB ripple waveform.

When higher duty cycles are required, regulation can no longer be maintained by decreasing the OFF time below the Minimum OFF Time limit. When this limit is reached, then the OFF Time is no longer reduced, and the MIC4950 smoothly transitions to an ON-time modulation mode. In the ON-time modulation region, frequency reduces with the increase of the required ON-time/duty cycle, and regulation finally takes place on the peak of the FB ripple waveform.

Note that because of the shift of the regulation threshold between different modes, line regulation might suffer when the input voltage and/or duty cycle variations force the MIC4950 to switch form one regulation mode to the other. In applications where wide input voltage variations are expected, ensure that the line regulation is adequate for the intended application.

Applications Information

The MIC4950 is a highly efficient, 5A synchronous buck regulator ideally suited for supplying processor core and I/O voltages from a 5V or 3.3V bus.

Input Capacitor

A 10µF ceramic capacitor or greater should be placed close to the PVIN pin and PGND pin for bypassing. A X5R or X7R temperature rating is recommended for the input capacitor. Take into account C versus bias effect to estimate the effective capacitance and the input ripple at the V_{IN} voltage.

Output Capacitor

The MIC4950 is designed for use with a 10µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response. A low equivalent-series resistance (ESR) ceramic output capacitor is recommended based on performance, size, and cost. Ceramic capacitors with X5R or X7R temperature ratings are recommended.

Inductor Selection

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)
- Core losses

The MIC4950 is designed for use with a 1µH to 2.2µH inductor. For faster transient response, a 1µH inductor will yield the best result. For lower output ripple, a 2.2µH inductor is recommended.

Inductor current ratings are generally given in two methods: permissible DC current, and saturation current. Permissible DC current can be rated for a 20°C to 40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Make sure that the nominal current of the application is well within the permissible DC current ratings of the inductor, also depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are a very important contribution to the total inductor core loss and temperature increase in high-frequency DC-DC converters, since core losses increase with at least the square of the excitation frequency. For more accurate core loss estimation, refer to manufacturers' datasheets or websites.

When saturation current is specified, make sure that there is enough design margin, so that the peak current does not cause the inductor to enter saturation.

Also pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate even in current limit operation, otherwise the current might instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic.

Peak current can be calculated in Equation 2:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \quad \text{Eq. 2}$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the "Efficiency Considerations" subsection.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied (see the Typical Characteristics curves):

$$Efficiency\% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100 \quad \text{Eq. 3}$$

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the ON cycle. Power loss is equal to the high-side MOSFET R_{DSON} multiplied by the switch current squared. During the OFF cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required to drive the gates on and off at high frequency and the switching transitions make up the switching losses.

At the higher currents for which the MIC4950 is designed, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In this case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 4.

$$P_{DCR} = I_{OUT}^2 \times DCR \quad \text{Eq. 4}$$

From that, the loss in efficiency due to inductor DCR and core losses (P_{CORE}) can be calculated as in Equation 5.

$$\text{EfficiencyLoss}(\%) = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR} + P_{CORE}}\right)\right] \times 100 \quad \text{Eq. 5}$$

External Ripple Injection

The MIC4950 control loop is ripple-based, and relies on an internal ripple injection network to generate enough ripple amplitude at the FB pin when negligible output voltage ripple is present. The internal ripple injection network is typically sufficient when recommended R1-R2 and C_F values are used. The FB ripple amplitude should fall in the 20mV to 100mV range.

If significantly lower divider resistors and/or higher C_F values are used, the amount of internal ripple injection may not be sufficient for stable operation. In this case, external ripple injection is needed. This is accomplished by connecting a series R_{inj}-C_{inj} circuit between the SW and the FB pins, as shown in Figure 1.

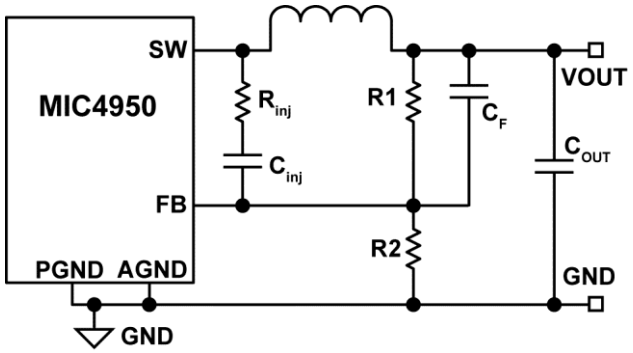


Figure 1. External Ripple Injection

The injected ripple is calculated using Equation 6,

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad \text{Eq. 6}$$

with K_{div} given by Equation 7

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \quad \text{Eq. 7}$$

and:

V_{IN} = Power stage input voltage

$D = V_{OUT}/V_{IN}$ = Duty cycle

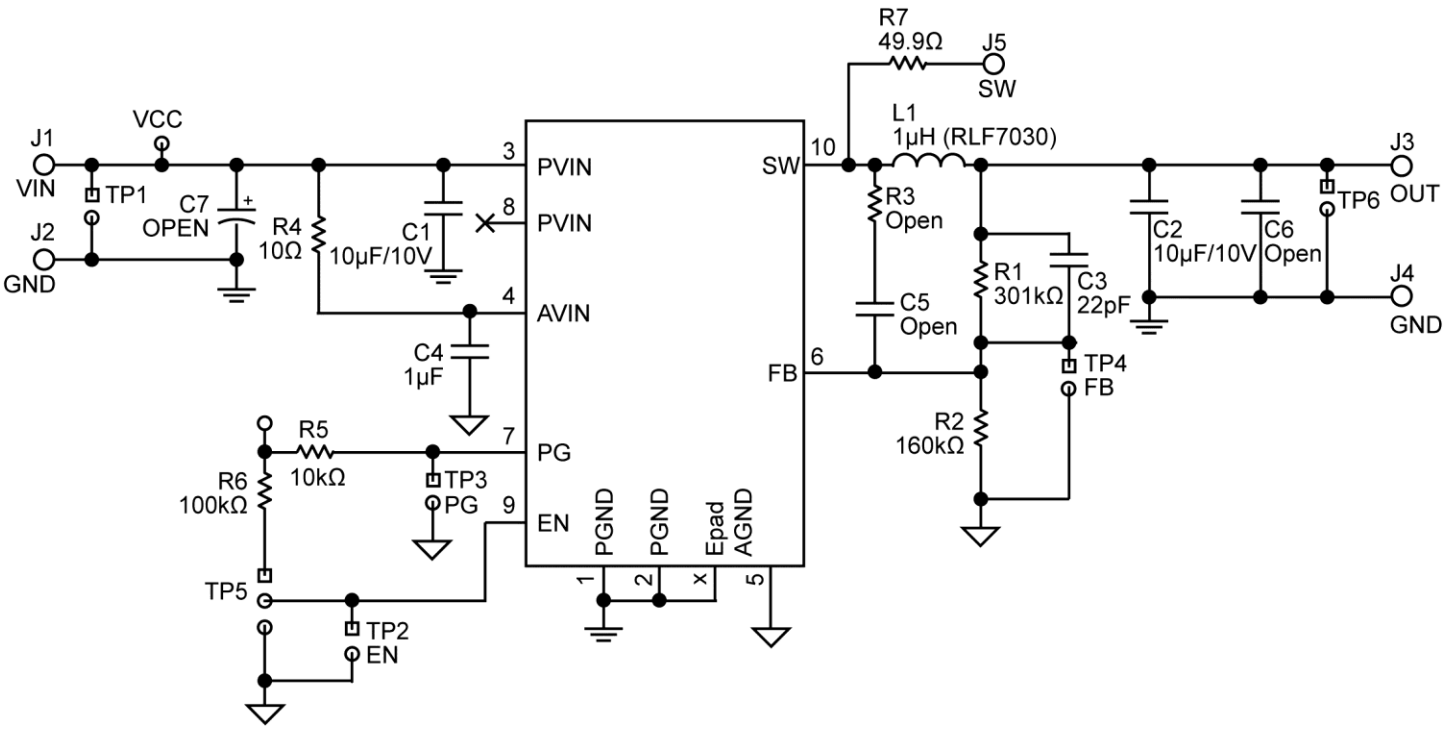
f_{SW} = Switching frequency

$\tau = (R1//R2//R_{inj}) \times C_F$

In Equations 6 and 7, it is assumed that the time constant associated with C_F must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \quad \text{Eq. 8}$$

Evaluation Board Circuit



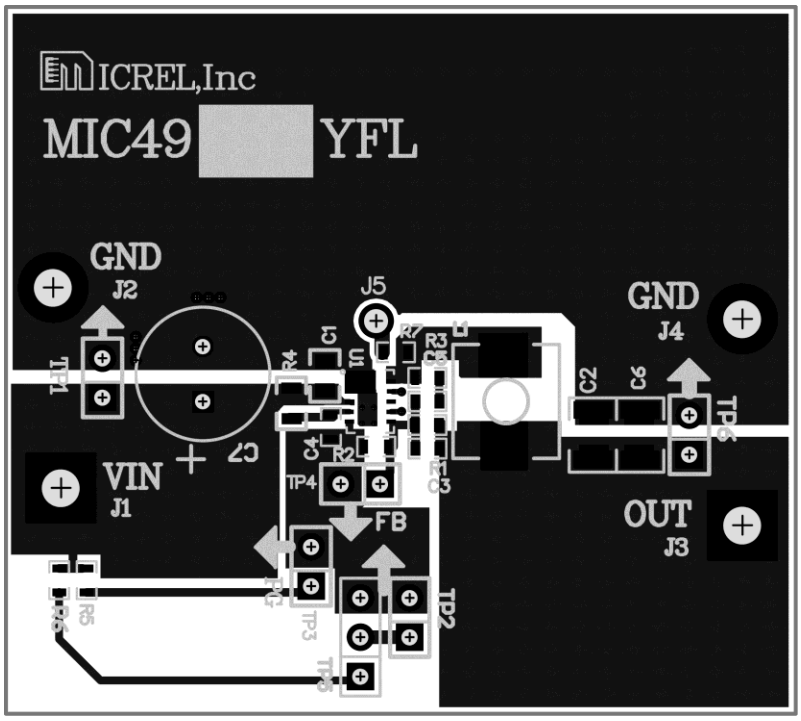
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2	C2012X5R1A106M125AB	TDK[7]	Ceramic Capacitor, 10µF, 10V, X5R, Size 0805	2
	GRM219R61A106ME44	Murata[8]		
C3	C1608C0G1H220J080AA	TDK	Ceramic Capacitor, 22pF, 50V, C0G, Size 0603	1
	GRM1885C1H220JA01	Murata		
C4	C1608X5R1A105M080AC	TDK	Ceramic Capacitor, 1µF, 10V, X5R, Size 0603	1
	GRM185R61A105ME26	Murata		
C5			DNP, Size 0603	0
C6			DNP, Size 1210	0
C7			DNP, Radial, 8mm diameter polarized capacitor	0
L1	RLF7030T-1R0N6R4	TDK	1µH, 6.4A, 7.3mΩ, L7.3mm x W6.8mm x H3.2mm	1
	CLF7045T-1R0N	TDK	1µH, 5.2A, 9.6mΩ, L7.2mm x W6.9mm x H4.5mm	
	CDRH8D43RT125NP-1R0NC	Sumida[9]	1µH, 7.5A, 7.8mΩ, L8.5mm x W8.3mm x H4.5 mm	
R1	CRCW06033013FK	Vishay[10]	Resistor, 301kΩ, Size 0603	1
R2	CRCW06031603FK	Vishay	Resistor, 160kΩ, Size 0603	1
R3			DNP, Size 0603	0
R4	CRCW060310R0FK	Vishay	Resistor, 10Ω, Size 0603	1
R5	CRCW06031002FK	Vishay	Resistor, 10kΩ, Size 0603	1
R6	CRCW06031003FK	Vishay	Resistor, 100kΩ, Size 0603	1
R7	CRCW060349R9FK	Vishay	Resistor, 49.9Ω, Size 0603, for monitoring SW node only	1
U1	**MIC4950YFL**	**Micrel, Inc.**[11]	**Hyper Speed Control™ 5A Buck Regulator**	**1**

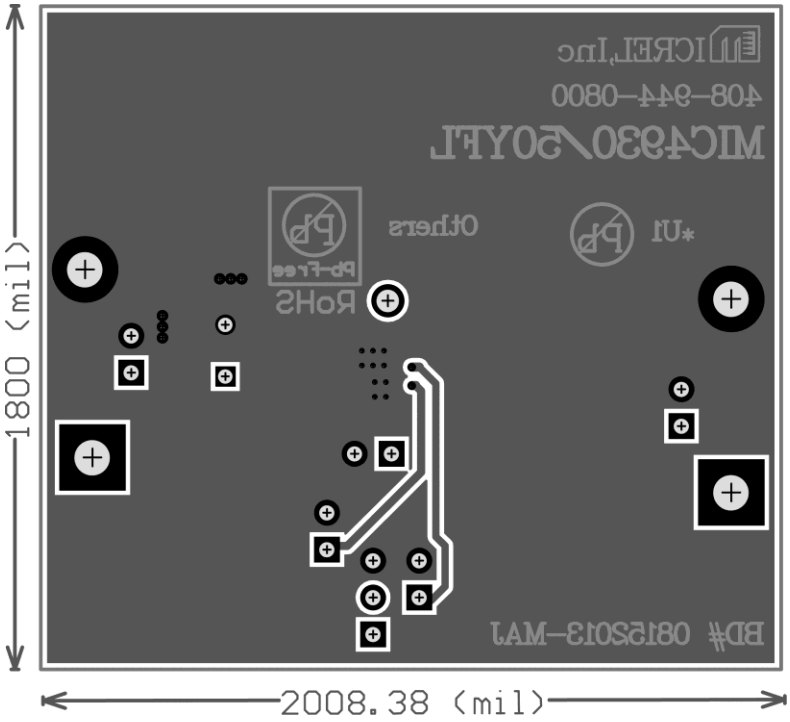
Notes:

7. TDK: www.tdk.com.
8. Murata: www.murata.com.
9. Sumida: www.sumida.com.
10. Vishay: www.vishay.com.
11. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

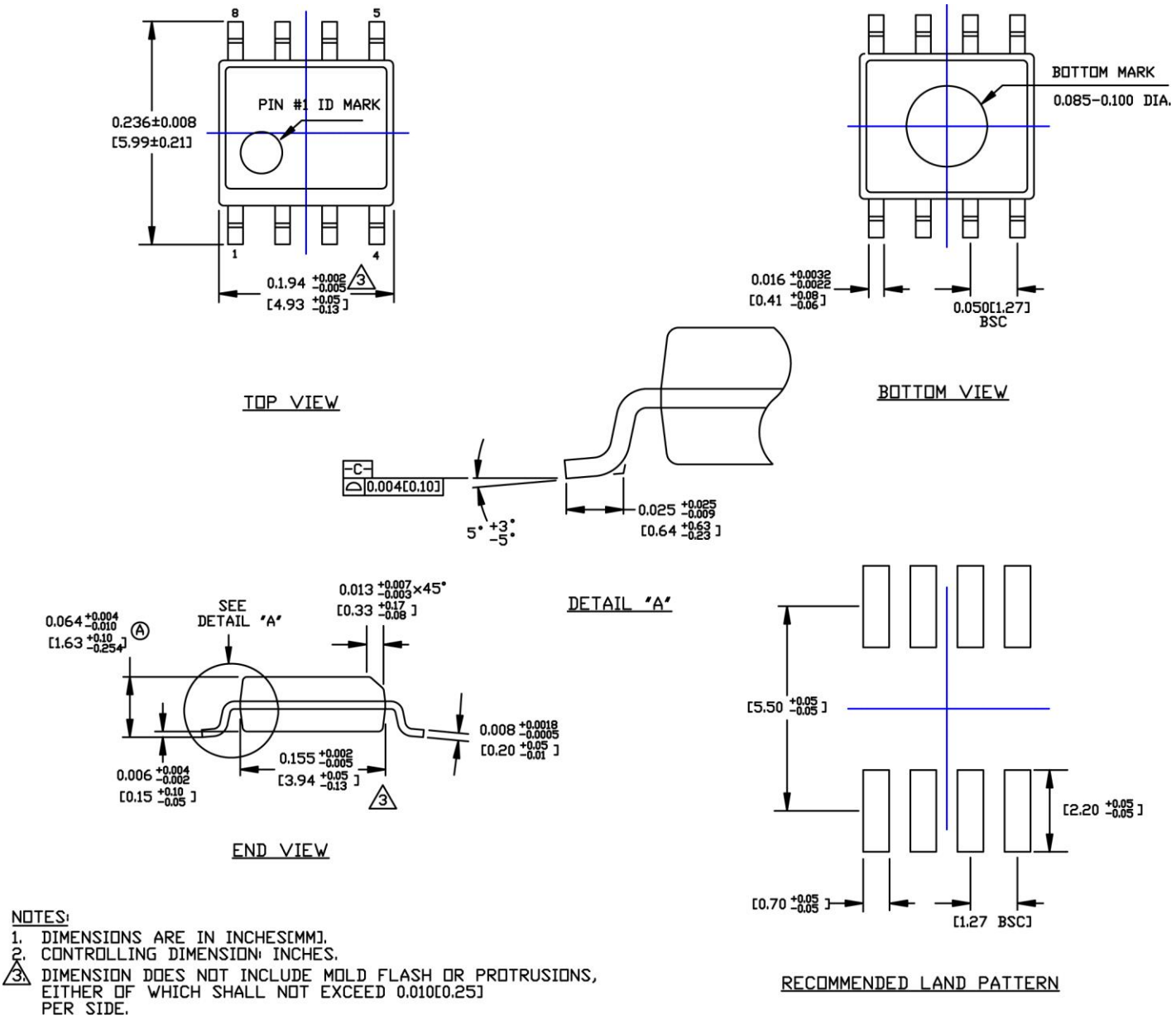


Top Layer



Bottom Layer

Package Information and Recommended Landing Pattern[12]

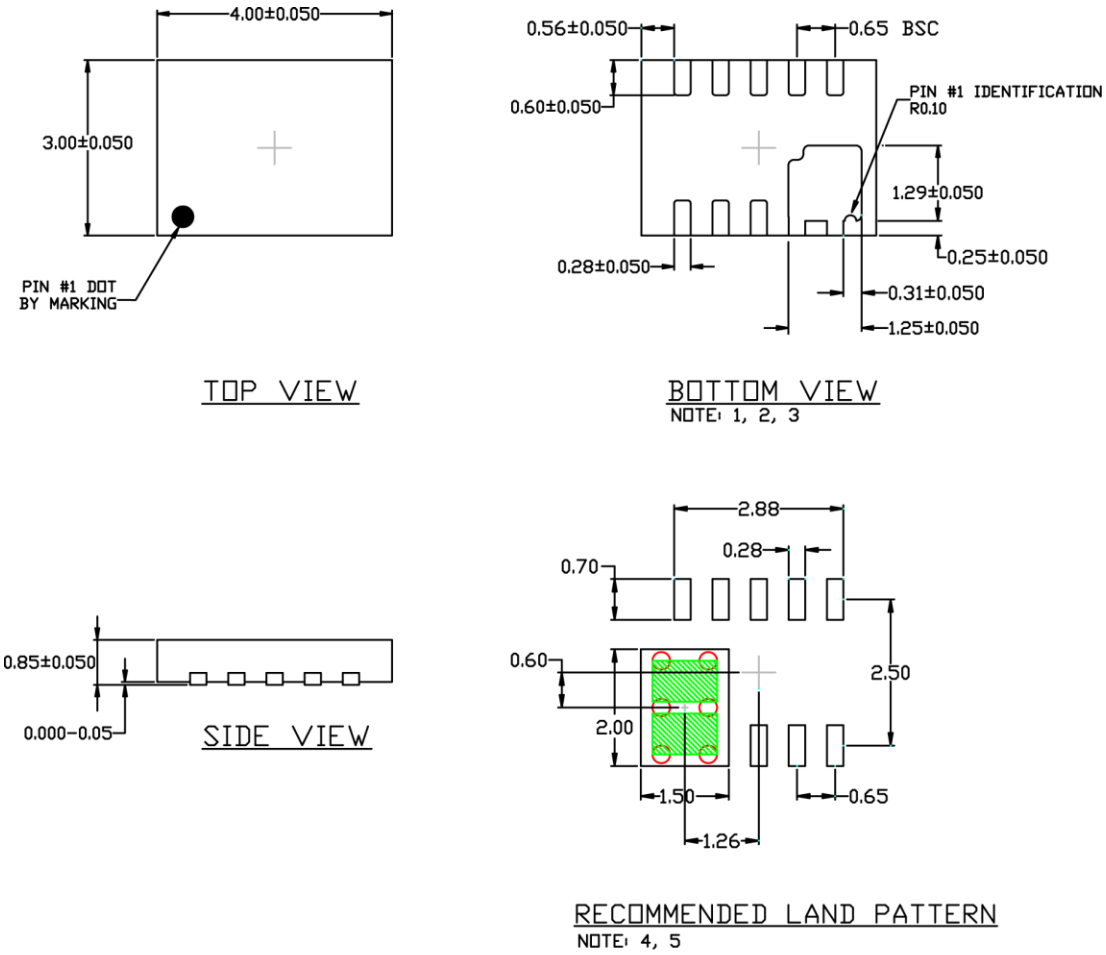


8-Pin SOIC (FM)

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information Recommended Landing Pattern[12] (Continued)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) REPRESENT STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.85X0.87 MM, 1.07 MM PITCH SPACING
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 – 0.35 MM RECOMMENDED DIAMETER, 0.80MM PITCH SPACING

10-Pin DFN 3mm x 4mm (FL)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com