

## FEATURES

- Differential D, clock and Q
- Extended 100E VEE range of -4.2V to -5.5V
- VBB output for single-ended use
- 1100MHz min. toggle frequency
- Edge-triggered asynchronous set and reset
- Fully compatible with Motorola MC10E/100E431
- Available in 28-pin PLCC package

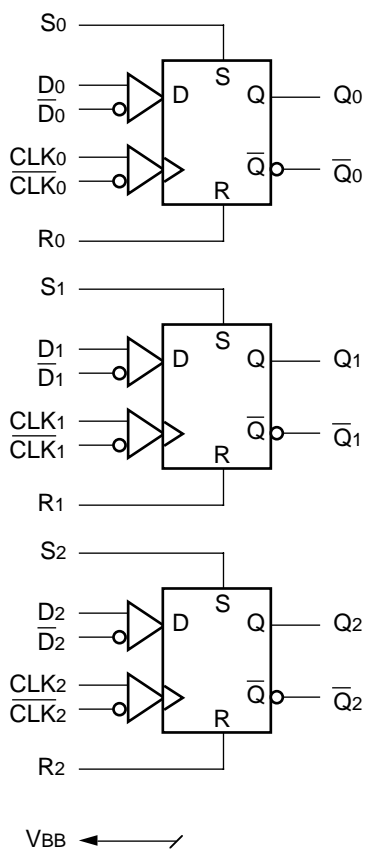
## DESCRIPTION

The SY10/100E431 are 3-bit flip-flops with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduces the metastability susceptibility window.

## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D[0:2], $\bar{D}$ [0:2]	Differential Data Inputs
CLK[0:2], $\bar{CLK}$ [0:2]	Differential Clock Inputs
S[0:2]	Edge Triggered Set Inputs
R[0:2]	Edge Triggered Reset Inputs
VBB	VBB Reference Output
Q[0:2], $\bar{Q}$ [0:2]	Differential Data Outputs
Vcco	Vcc to Output

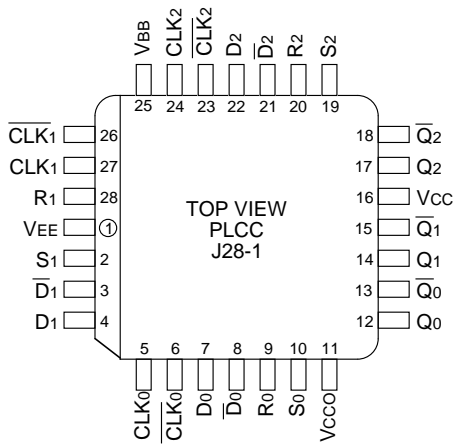
## TRUTH TABLE<sup>(1)</sup>

D <sub>n</sub>	CLK <sub>n</sub>	R <sub>n</sub>	S <sub>n</sub>	Q <sub>n</sub>
L	Z	L	L	L
H	Z	L	L	H
X	L	Z	L	L
X	L	L	Z	H

**NOTE:**

1. Z = LOW-to-HIGH transition.

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E431JC	J28-1	Commercial	SY10E431JC	Sn-Pb
SY10E431JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E431JC	Sn-Pb
SY100E431JC	J28-1	Commercial	SY100E431JC	Sn-Pb
SY100E431JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E431JC	Sn-Pb
SY10E431JZ <sup>(3)</sup>	J28-1	Commercial	SY10E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E431JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E431JZ <sup>(3)</sup>	J28-1	Commercial	SY100E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E431JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E431JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**DC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
VBB	Output Reference Voltage										V	—
	10E	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19		
	100E	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26		
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I <sub>EE</sub>	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		
V <sub>CMR</sub>	Common Mode Range	-1.5	—	0	-1.5	—	0	-1.5	—	0	V	1

**Notes:**

- V<sub>CMR</sub> is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V<sub>CMR</sub> range and the input swing is greater than V<sub>PP</sub> (min.) and <1V.

**AC ELECTRICAL CHARACTERISTICS**

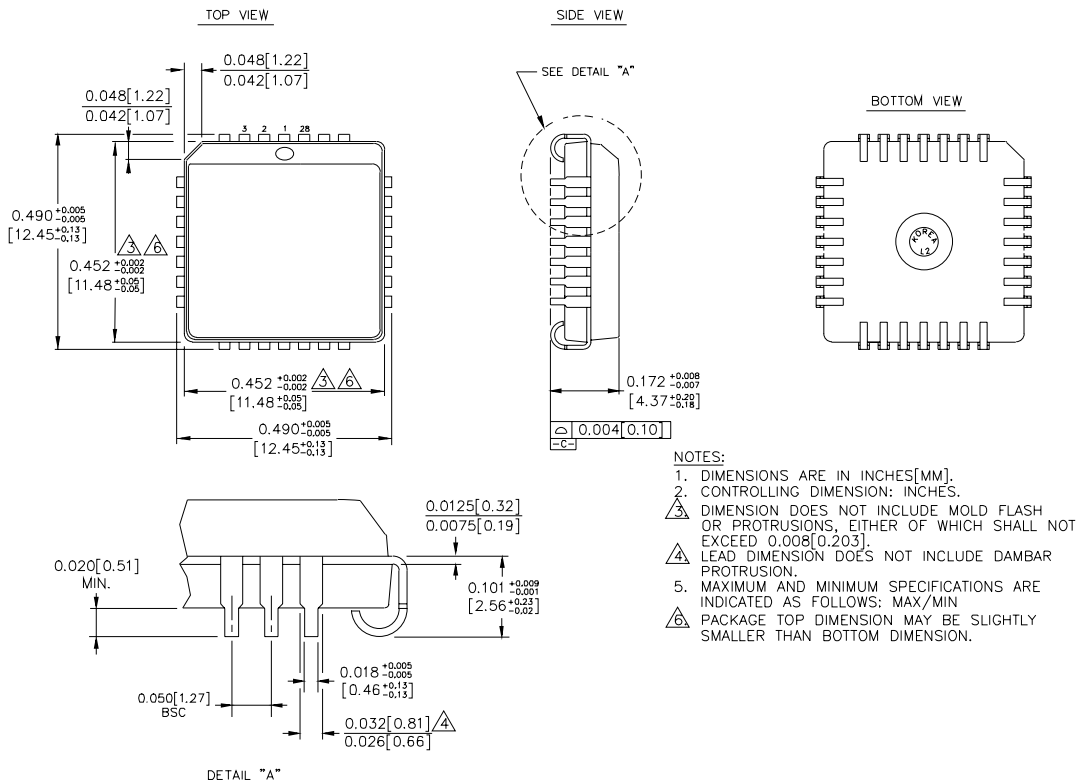
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f <sub>MAX</sub>	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t <sub>PD</sub>	Propagation Delay to Output										ps	—
	CLK (Diff)	450	600	750	450	600	750	450	600	750		
	CLK (SE)	400	600	800	400	600	800	400	600	800		
	R	550	725	925	550	725	925	550	725	925		
t <sub>S</sub>	Set-up Time										ps	1 1
	D	200	0	—	200	0	—	200	0	—		
	R	1000	700	—	1000	700	—	1000	700	—		
	S	1000	700	—	1000	700	—	1000	700	—		
t <sub>H</sub>	Hold Time, D	200	0	—	200	0	—	200	0	—	ps	—
t <sub>PW</sub>	Minimum Pulse Width, CLK	400	—	—	400	—	—	400	—	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	2
V <sub>PP</sub> (AC)	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	3
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	275	450	650	275	450	650	275	450	650	ps	—

**Notes:**

- These set-up times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
- Within-device skew is defined as identical transitions on similar paths through a device.
- Minimum input swing for which AC parameters are guaranteed.

**28-PIN PLCC (J28-1)**



Rev. 03

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