

Features

- Generates clock signals at power-up per user defined custom OTP (One Time Programmable) configuration
- Operates from a single crystal resonator, clock oscillator or voltage controlled oscillator
- Four independently programmable clock synthesizers generate any clock rate from 1 kHz to 720 MHz
- Precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- General purpose synthesizers generate a wide range of digital bus clocks
- Supports programmable frequency offsets for clock margining; or for use as a digitally controlled oscillator
- Eight LVPECL outputs; max rate 720 MHz
- Four LVCMOS outputs; max rate 177.5 MHz

Ordering Information

ZL30230GGG	100 Pin LBGGA	11mmx11mm Trays
ZL30230GGG2	100 Pin LBGGA*	11mmx11mm Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Eight outputs configurable as LVCMOS at 3.3/2.5/1.8 or 1.5 V, max rate 160 MHz; or LVDS/LVPECL/HCSL, max rate 350 MHz
- Dynamically Configurable via SPI/I2C interface

Applications

- Timing for NPU's, FPGAs, Ethernet switches and PCIe switches
- Timing for 10 Gigabit CDRs, Rapid-IO, PCIe, Serial MII, Star Fabric, Fibre Channel, XAUI
- Processor clock, Processor bus clock, SDRAM clock, DDR clock

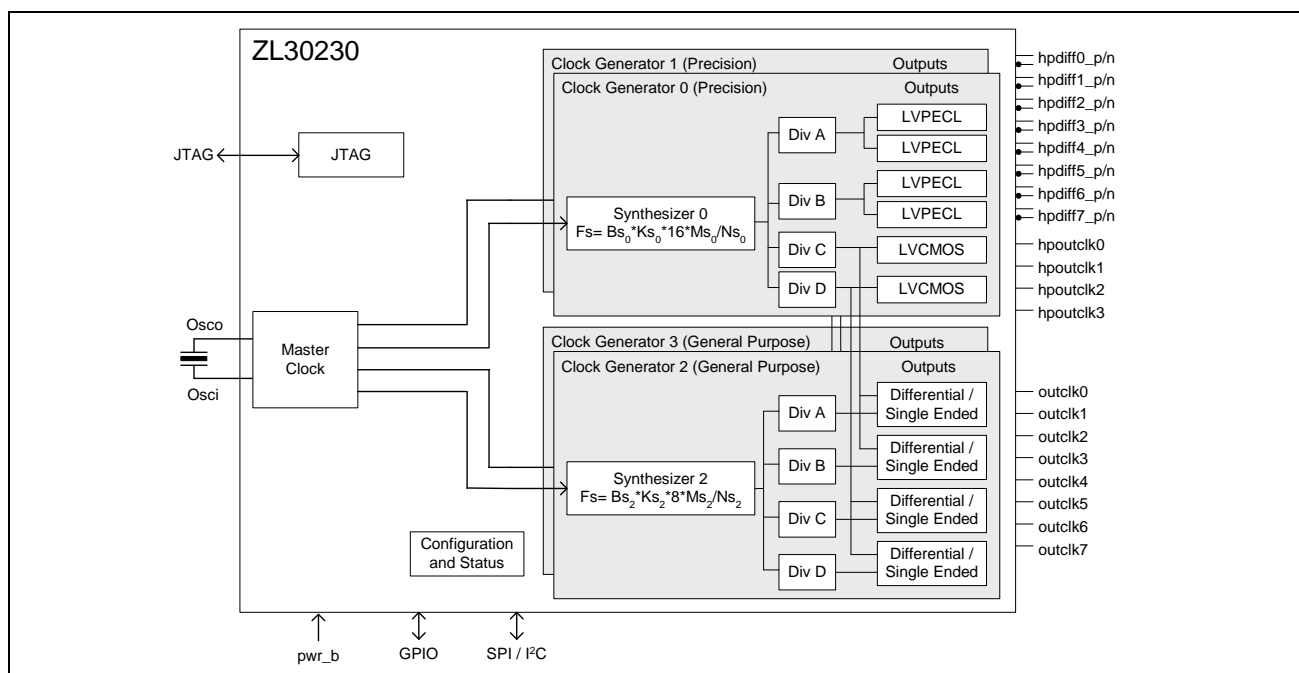


Figure 1 - Functional Block Diagram

Description

The ZL30230 Four Channel Universal Clock Generator, part of Zarlink's ClockCenter platform of Free Run Clock devices, delivers industry leading performance for a range of free run applications. The free run synchronization solution allows designers to replace multiple, costly components with a highly integrated and programmable, singlechip solution.

The ZL30230 device generates up to 20 clocks from a single crystal, allowing designers to replace numerous oscillators traditionally used to provide timing for various components with one chip.

Change Summary

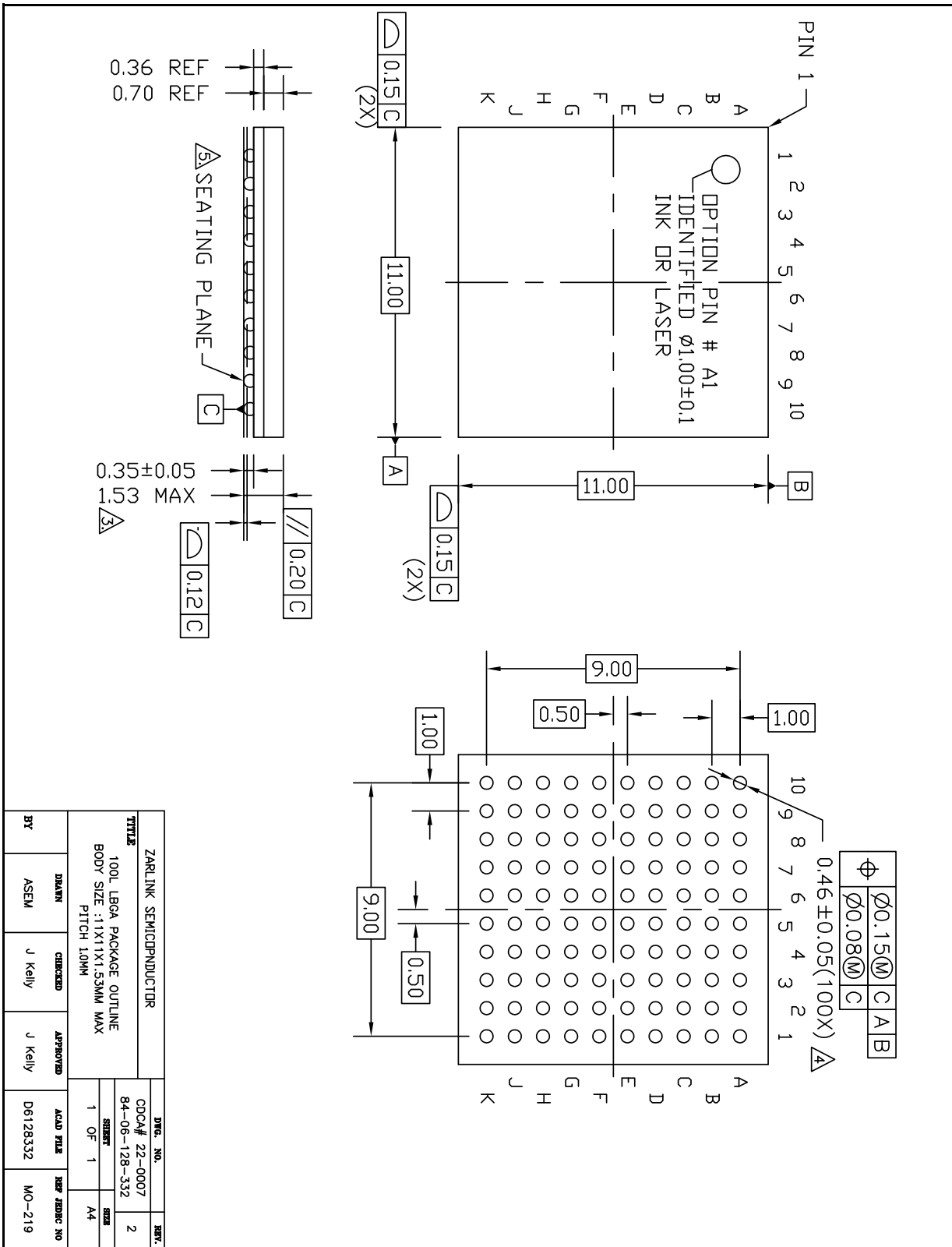
Below are the changes from the June 2011 issue to the July 2011 issue.

Page	Item	Change
1	Features	Added OTP feature.

Below are the changes from the January 2011 issue to the June 2011 issue.

Page	Item	Change
1	Ordering Information	Corrected package description in ordering information to LBGA.
3	Mechanical Drawing	Replaced drawing to reflect correct package description.

Mechanical Drawing



ZARLINK SEMICONDUCTOR		DRAWING NO.		REV.	
TITLE		COCOA# 22-0007		2	
100L LBGA PACKAGE OUTLINE		84-06-128-332			
BODY SIZE :11X11X1.53MM MAX		SHEET		SIZE	
PITCH 10MM		1 OF 1		A4	
BY	DRAWN	CHECKED	APPROVED	ACAD FILE	REV. HISTORY NO
ASEM	J Kelly	J Kelly	J Kelly	D6128332	MO-219



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