

## Super Charge Pump DC-to-DC Voltage Converter

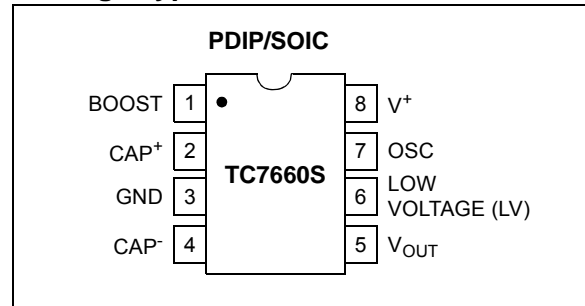
### Features

- Oscillator boost from 10 kHz to 45 kHz
- Converts +5V Logic Supply to  $\pm 5V$  System
- Wide Input Voltage Range: +1.5V to +12V
- Efficient Voltage Conversion (99.9%, typical)
- Excellent Power Efficiency (98%, typical)
- Low Power Consumption: 80  $\mu A$  (typical) @  $V_{IN} = 5V$
- Low Cost and Easy to Use
  - Only Two External Capacitors Required
- Available in 8-Pin Small Outline (SOIC) and 8-Pin PDIP Packages
- Improved ESD Protection (10 kV HBM)
- No External Diode Required for High-Voltage Operation

### Applications

- RS-232 Negative Power Supply
- Simple Conversion of +5V to  $\pm 5V$  Supplies
- Voltage Multiplication  $V_{OUT} = \pm n V^+$
- Negative Supplies for Data Acquisition Systems and Instrumentation

### Package Types



### General Description

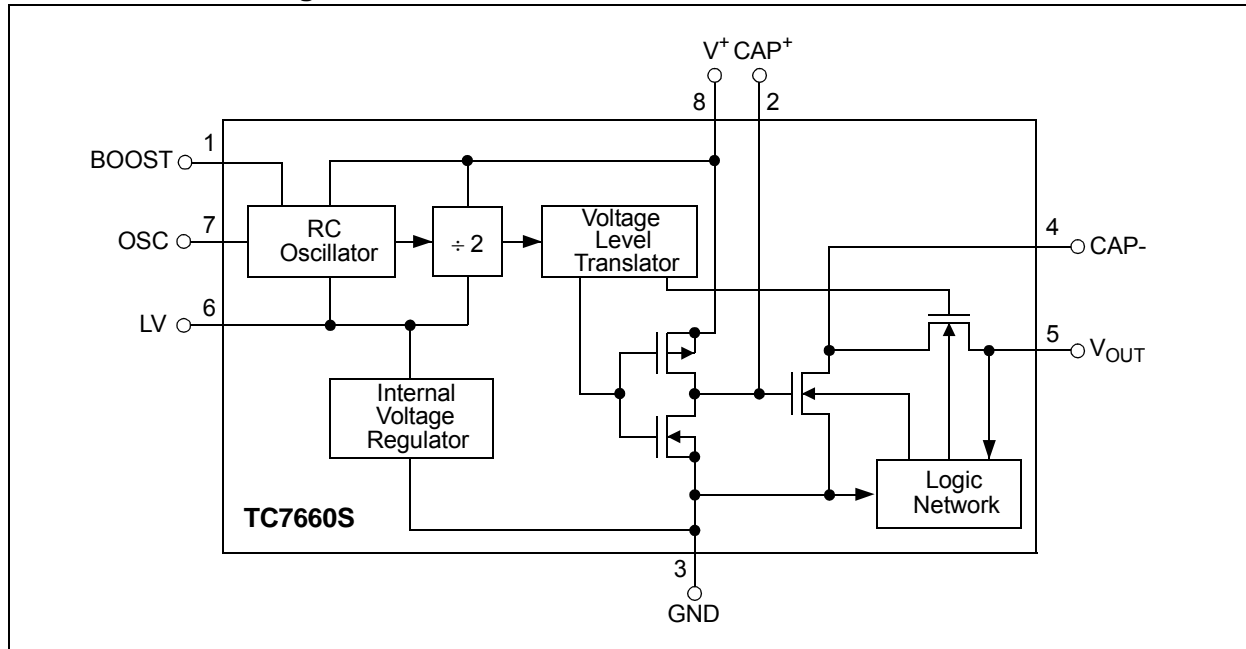
The TC7660S device is a pin-compatible replacement for the industry standard 7660 charge pump voltage converter. It converts a +1.5V to +12V input to a corresponding -1.5V to -12V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and electromagnetic interference (EMI). Added features include an extended supply range to 12V, and a frequency boost pin for higher operating frequency, allowing the use of smaller external capacitors.

The on-board oscillator operates at a nominal frequency of 10 kHz. Frequency is increased to 45 kHz when pin 1 is connected to V<sup>+</sup>. Operation below 10 kHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground (with pin 1 open).

The TC7660S is available in 8-Pin PDIP and 8-Pin Small Outline (SOIC) packages in commercial and extended temperature ranges.

# TC7660S

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage .....	+13V
LV, Boost, and OSC Inputs Voltage: (Note 1)	
.....	-0.3V to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> < 5.5V
.....	(V <sup>+</sup> - 5.5V) to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> > 5.5V
Current into LV .....	20 μA for V <sup>+</sup> > 3.5V
Output Short Duration (V <sub>SUPPLY</sub> ≤ 5.5V).....	Continuous
Package Power Dissipation: (T <sub>A</sub> ≤ +70°C) (Note 2)	
8-Pin PDIP .....	730 mW
8-Pin SOIC .....	470 mW
Lead Temperature (Soldering, 10s) .....	+300°C

**Notice†:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Connecting any input terminal to voltages greater than V<sup>+</sup> or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the TC7660S.

**2:** Derate linearly above +50°C by 5.5 mW/°C.

## ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, specifications measured over operating temperature range with V<sup>+</sup> = 5V, C<sub>OSC</sub> = 0, refer to test circuit in Figure 4-1.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current (Boost pin OPEN or GND)	I <sup>+</sup>	—	80	160	μA	R <sub>L</sub> = ∞
		—	—	180		0°C ≤ T <sub>A</sub> ≤ +70°C
		—	—	180		-40°C ≤ T <sub>A</sub> ≤ +85°C
		—	—	200		-55°C ≤ T <sub>A</sub> ≤ +125°C
Supply Current (Boost pin = V <sup>+</sup> )	I <sup>+</sup>	—	—	300	μA	0°C ≤ T <sub>A</sub> ≤ +70°C
		—	—	350		-40°C ≤ T <sub>A</sub> ≤ +85°C
		—	—	400		-55°C ≤ T <sub>A</sub> ≤ +125°C
Supply Voltage Range, High	V <sub>H</sub> <sup>+</sup>	3.0	—	12	V	Min. ≤ T <sub>A</sub> ≤ Max, R <sub>L</sub> = 10 kΩ, LV Open
Supply Voltage Range, Low	V <sub>L</sub> <sup>+</sup>	1.5	—	3.5	V	Min. ≤ T <sub>A</sub> ≤ Max, R <sub>L</sub> = 10 kΩ, LV to GND
Output Source Resistance	R <sub>OUT</sub>	—	60	100	Ω	I <sub>OUT</sub> = 20 mA
		—	70	120		I <sub>OUT</sub> = 20 mA, 0°C ≤ T <sub>A</sub> ≤ +70°C
		—	70	120		I <sub>OUT</sub> = 20 mA, -40°C ≤ T <sub>A</sub> ≤ +85°C
		—	105	150		I <sub>OUT</sub> = 20 mA, -55°C ≤ T <sub>A</sub> ≤ +125°C
		—	—	250		V <sup>+</sup> = 2V, I <sub>OUT</sub> = 3 mA, LV to GND 0°C ≤ T <sub>A</sub> ≤ +70°C
		—	—	400		V <sup>+</sup> = 2V, I <sub>OUT</sub> = 3 mA, LV to GND -55°C ≤ T <sub>A</sub> ≤ +125°C
Oscillator Frequency	f <sub>OSC</sub>	—	10	—	kHz	Pin 7 open, Pin 1 open or GND
		—	45	—		Boost Pin = V <sup>+</sup>
Power Efficiency	P <sub>EFF</sub>	96	98	—	%	R <sub>L</sub> = 5 kΩ; Boost Pin Open
		95	98	—		T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub> ; Boost Pin Open
		—	88	—		Boost Pin = V <sup>+</sup>

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## ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, specifications measured over operating temperature range with  $V^+ = 5V$ ,  $C_{OSC} = 0$ , refer to test circuit in [Figure 4-1](#).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Voltage Conversion Efficiency	$V_{OUTEFF}$	99	99.9	—	%	$R_L = \infty$
Oscillator Impedance	$Z_{OSC}$	—	1	—	M $\Omega$	$V^+ = 2V$
		—	100	—	k $\Omega$	$V^+ = 5V$

## TEMPERATURE SPECIFICATIONS

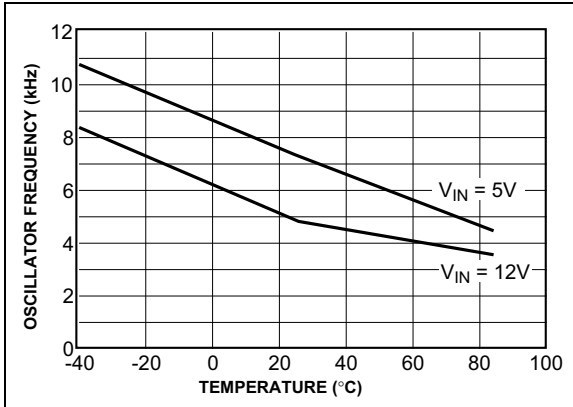
**Electrical Characteristics:** Unless otherwise noted, specifications measured over operating temperature range with  $V^+ = 5V$ ,  $C_{OSC} = 0$ , refer to test circuit in [Figure 4-1](#).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	0	—	+70	$^{\circ}C$	C suffix
	$T_A$	-40	—	+85	$^{\circ}C$	E suffix
	$T_A$	-40	—	+125	$^{\circ}C$	V suffix
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}C$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 8LD PDIP	$\theta_{JA}$	—	89.3	—	$^{\circ}C/W$	
Thermal Resistance, 8LD SOIC	$\theta_{JA}$	—	148.5	—	$^{\circ}C/W$	

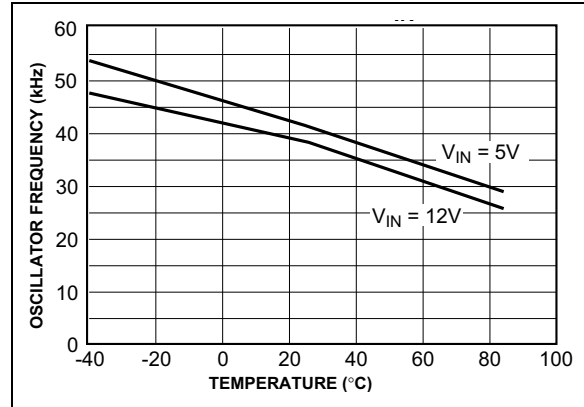
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

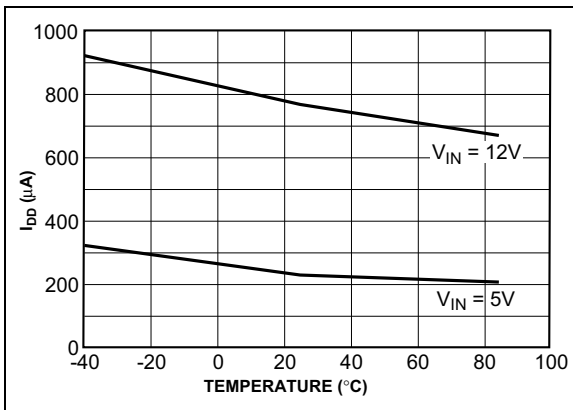
**Note:** Unless otherwise indicated,  $C_1 = C_2 = 10 \mu\text{F}$ ,  $\text{ESR}_{C1} = \text{ESR}_{C2} = 1 \Omega$ ,  $T_A = 25^\circ\text{C}$ . See Figure 4-1.



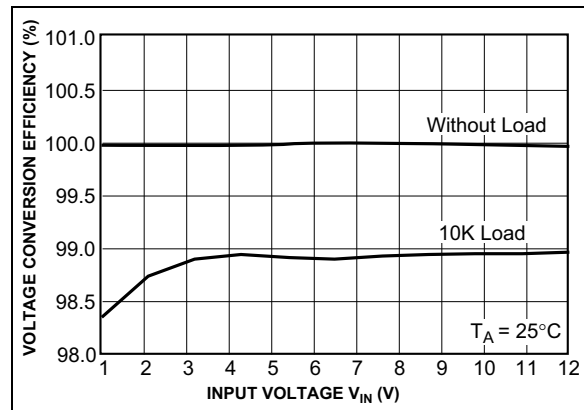
**FIGURE 2-1:** Unloaded Oscillator Frequency vs. Temperature.



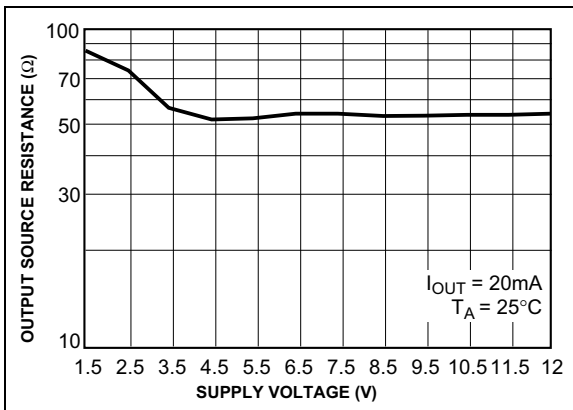
**FIGURE 2-4:** Unloaded Oscillator Frequency vs. Temperature with Boost Pin =  $V_{IN}$ .



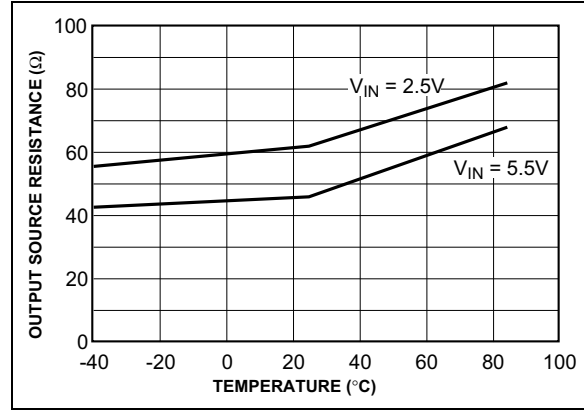
**FIGURE 2-2:** Supply Current vs. Temperature (with Boost Pin =  $V_{IN}$ ).



**FIGURE 2-5:** Voltage Conversion.



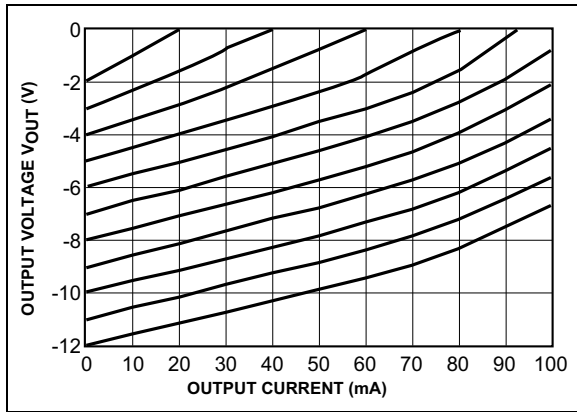
**FIGURE 2-3:** Output Source Resistance vs. Supply Voltage.



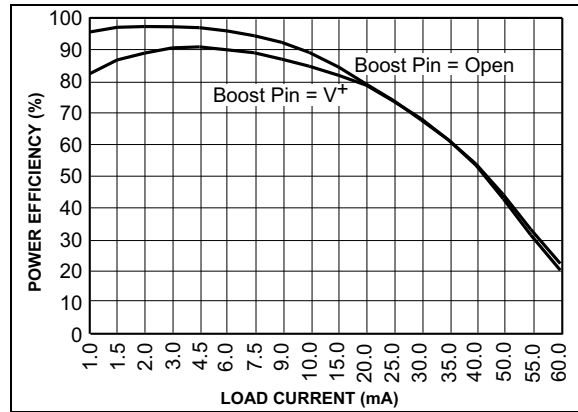
**FIGURE 2-6:** Output Source Resistance vs. Temperature.

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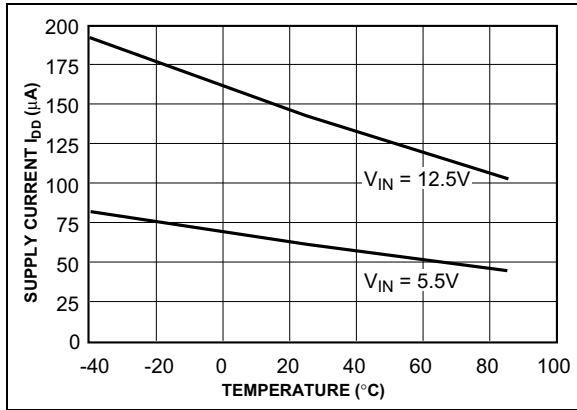
**Note:** Unless otherwise indicated,  $C_1 = C_2 = 10 \mu\text{F}$ ,  $\text{ESR}_{C1} = \text{ESR}_{C2} = 1 \Omega$ ,  $T_A = 25^\circ\text{C}$ . See Figure 4-1.



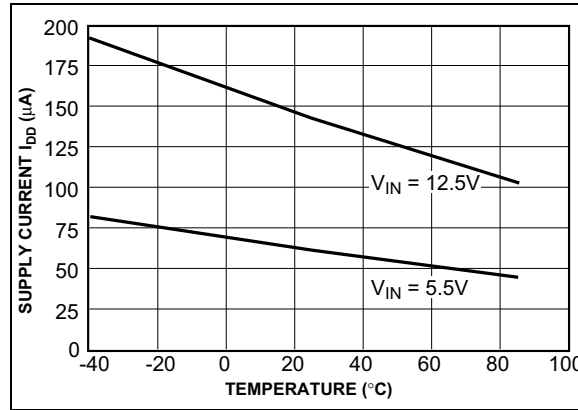
**FIGURE 2-7:** Output Voltage vs. Output Current.



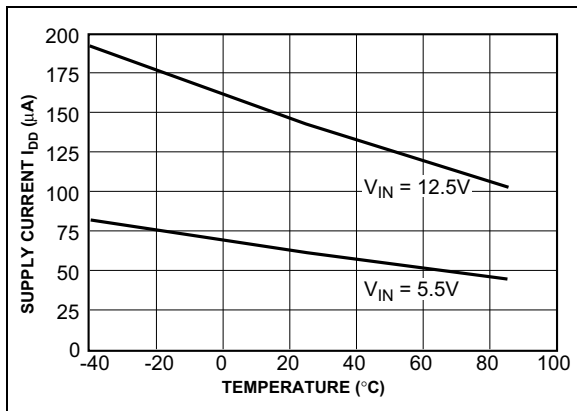
**FIGURE 2-10:** Power Conversion Efficiency vs. Load.



**FIGURE 2-8:** Supply Current vs. Temperature.



**FIGURE 2-11:** Supply Current vs. Temperature.



**FIGURE 2-9:** Supply Current vs. Temperature.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

Pin No.	Symbol	Description
1	BOOST	Switching Frequency boost pin
2	CAP <sup>+</sup>	Charge pump capacitor positive terminal
3	GND	Ground terminal
4	CAP <sup>-</sup>	Charge pump capacitor negative terminal
5	V <sub>OUT</sub>	Output voltage
6	LV	Low voltage pin. Connect to GND for V <sub>+</sub> < 3.5V
7	OSC	Oscillator control input. Bypass with an external capacitor to slow the oscillator.
8	V <sup>+</sup>	Power supply positive voltage input

### 3.1 Switching Frequency Boost Pin (Boost)

By connecting the boost pin (pin 1), the switching frequency of the charge pump is increased from 10 kHz typical to 45 kHz typical. By connecting the boost pin (pin1), to the V<sup>+</sup> pin (pin 8), the switching frequency of the charge pump is increased from 10 kHz typical to 45 kHz typical.

### 3.2 Charge Pump Capacitor (CAP<sup>+</sup>)

Positive connection for the charge pump capacitor, or flying capacitor, used to transfer charge from the input source to the output. In the voltage-inverting configuration, the charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, the charge pump capacitor is inverted and charge is transferred to the output capacitor and load.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output resistance.

### 3.3 Ground (GND)

Input and output zero volt reference.

### 3.4 Charge Pump Capacitor (CAP<sup>-</sup>)

Negative connection for the charge pump capacitor, or flying capacitor, used to transfer charge from the input to the output. Proper orientation is imperative when using a polarized capacitor.

### 3.5 Output Voltage (V<sub>OUT</sub>)

Negative connection for the charge pump output capacitor. In the voltage-inverting configuration, the charge pump output capacitor supplies the output load during the first half of the switching cycle. During the second half of the switching cycle, charge is restored to the charge pump output capacitor.

It is recommended that a low ESR capacitor be used. Additionally, larger values will lower the output ripple.

### 3.6 Low Voltage Pin (LV)

The low voltage pin ensures proper operation of the internal oscillator for input voltages below 3.5V. The low voltage pin should be connected to ground (GND) for input voltages below 3.5V. Otherwise, the low voltage pin should be allowed to float.

### 3.7 Oscillator Control Input (OSC)

The oscillator control input can be utilized to slow down or speed up the operation of the TC7660S. Refer to [Section 5.4 “Changing the TC7660S Oscillator Frequency”](#), for details on altering the oscillator frequency.

### 3.8 Power Supply (V<sup>+</sup>)

Positive power supply input voltage connection. It is recommended that a low ESR capacitor be used to bypass the power supply input to ground (GND).

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## 4.0 DETAILED DESCRIPTION

### 4.1 Theory of Operation

The TC7660S contains all the necessary circuitry to implement a voltage inverter, with the exception of two external capacitors, which may be inexpensive 10  $\mu\text{F}$  polarized electrolytic capacitors. Operation is best understood by considering Figure 4-2, which shows an idealized voltage inverter. Capacitor  $C_1$  is charged to a voltage  $V^+$  for the half cycle when switches  $S_1$  and  $S_3$  are closed. (Note that switches  $S_2$  and  $S_4$  are open during this half cycle.) During the second half cycle of operation, switches  $S_2$  and  $S_4$  are closed, with  $S_1$  and  $S_3$  open, thereby shifting capacitor  $C_1$  negatively by  $V^+$  volts. Charge is then transferred from  $C_1$  negatively by  $V^+$  volts. Charge is then transferred from  $C_1$  to  $C_2$ , such that the voltage on  $C_2$  is exactly  $V^+$  assuming ideal switches and no load on  $C_2$ .

The four switches in Figure 4-2 are MOS power switches;  $S_1$  is a P-channel device, and  $S_2$ ,  $S_3$  and  $S_4$  are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of  $S_3$  and  $S_4$  must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ( $V_{\text{OUT}} = V^+$ ), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC7660S by a logic network which senses the output voltage ( $V_{\text{OUT}}$ ) together with the level translators, and switches the substrates of  $S_3$  and  $S_4$  to the correct level to maintain necessary reverse bias.

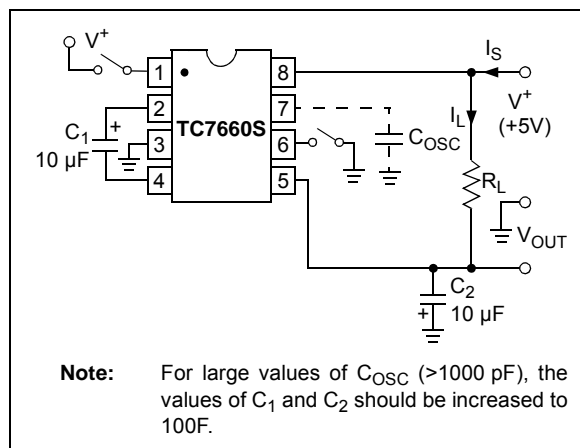


FIGURE 4-1: TC7660S Test Circuit.

The voltage regulator portion of the TC7660S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages.

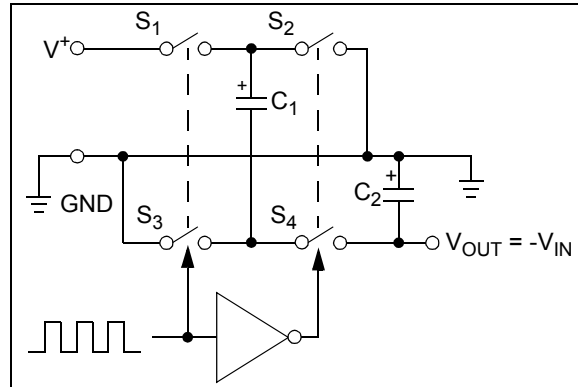


FIGURE 4-2: Ideal Charge Pump Inverter.

To improve low-voltage operation, the “LV” pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

### 4.2 Theoretical Power Efficiency Considerations

In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

- (1) The drive circuitry consumes minimal power.
- (2) The output switches have extremely low ON resistance and virtually no offset.
- (3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660S approaches these conditions for negative voltage multiplication if large values of  $C_1$  and  $C_2$  are used. Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs. The energy lost is defined by:

$$E = 1/2 C_1 (V_1^2 - V_2^2)$$

$V_1$  and  $V_2$  are the voltages on  $C_1$  during the pump and transfer cycles. If the impedances of  $C_1$  and  $C_2$  are relatively high at the pump frequency (refer to Figure 4-2) compared to the value of  $R_L$ , there will be a substantial difference in voltages  $V_1$  and  $V_2$ . Therefore, it is desirable not only to make  $C_2$  as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for  $C_1$  in order to achieve maximum efficiency of operation.

### 4.3 Dos and Don'ts

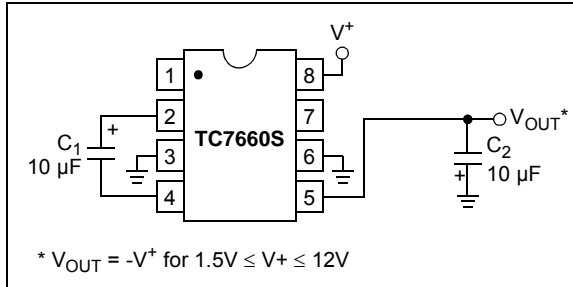
- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to  $V^+$  supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of  $C_1$  must be connected to pin 2 of the TC7660S and the + terminal of  $C_2$  must be connected to GND.



## 5.0 APPLICATIONS INFORMATION

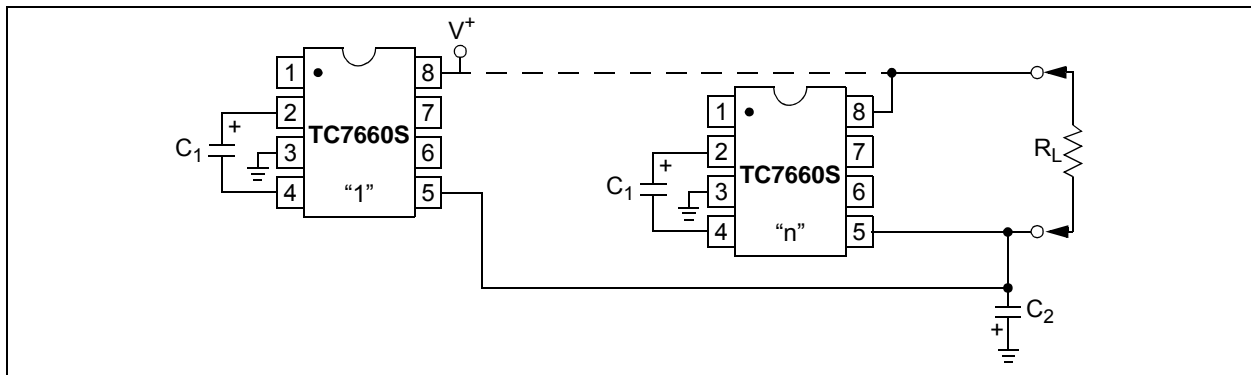
### 5.1 Simple Negative Voltage Converter

Figure 5-1 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

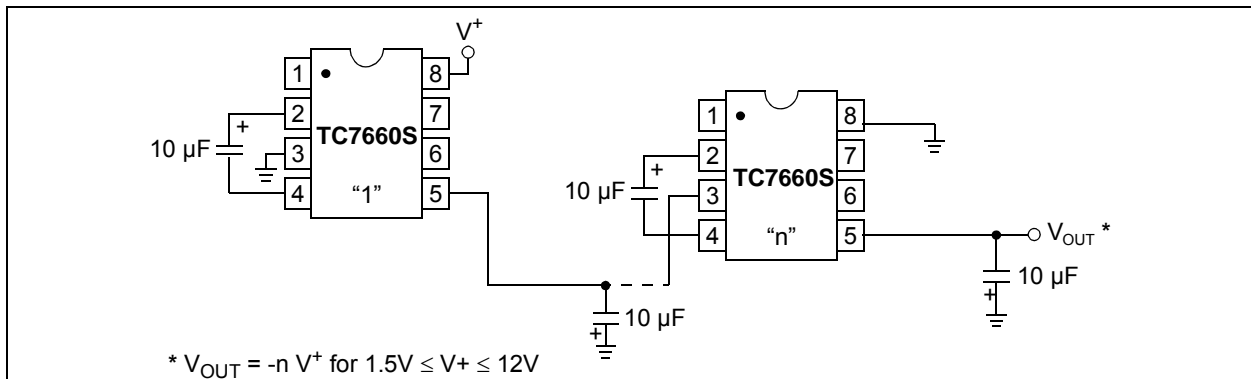


**FIGURE 5-1:** Simple Negative Converter.

The output characteristics of the circuit in Figure 5-1 are those of a nearly ideal voltage source in series with a 70Ω resistor. Thus, for a load current of -10 mA and a supply voltage of +5V, the output voltage would be -4.3V.



**FIGURE 5-2:** Paralleling Devices Lowers Output Impedance.



**FIGURE 5-3:** Increased Output Voltage By Cascading Devices.

The dynamic output impedance of the TC7660S is due, primarily, to capacitive reactance of the charge transfer capacitor ( $C_1$ ). Since this capacitor is connected to the output for only half of the cycle, the equation is:

#### EQUATION

$$X_C = \frac{2}{2fC_1} = 3.18\Omega$$

where:

$$f = 10 \text{ kHz and } C_1 = 10 \mu\text{F.}$$

### 5.2 Paralleling Devices

Any number of TC7660S voltage converters may be paralleled to reduce output resistance (Figure 5-2). The reservoir capacitor,  $C_2$ , serves all devices, while each device requires its own pump capacitor,  $C_1$ . The resultant output resistance would be approximately:

#### EQUATION

$$R_{OUT} = \frac{R_{OUT} \text{ (of TC7660S)}}{n \text{ (number of devices)}}$$

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## 5.3 Cascading Devices

The TC7660S may be cascaded as shown (Figure 5-3) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

### EQUATION

$$V_{OUT} = -n(V^+)$$

where  $n$  is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7660S  $R_{OUT}$  values.

## 5.4 Changing the TC7660S Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin, may be connected to  $V^+$  to increase oscillator frequency to 45 kHz from a nominal of 10 kHz for an input supply voltage of 5.0V. The oscillator may also be synchronized to an external clock as shown in Figure 5-4. In order to prevent possible device latch-up, a 1 k $\Omega$  resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 k $\Omega$  pull-up resistor to  $V^+$  supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be half of the clock frequency. Output transitions occur on the positive-going edge of the clock.

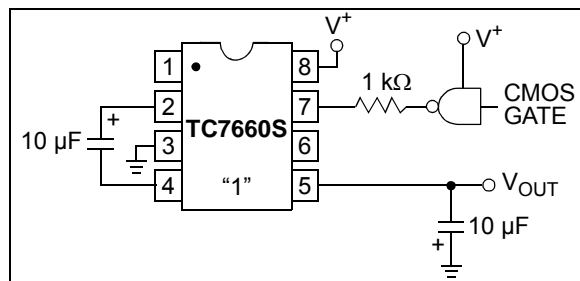


FIGURE 5-4: External Clocking.

It is also possible to increase the conversion efficiency of the TC7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor,  $C_{OSC}$ , as shown in Figure 5-5. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump ( $C_1$ ) and the reservoir ( $C_2$ ) capacitors. To overcome this, increase the values of  $C_1$  and  $C_2$  by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 ( $V^+$ ) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of  $C_1$  and  $C_2$  (from 10  $\mu$ F to 100  $\mu$ F).

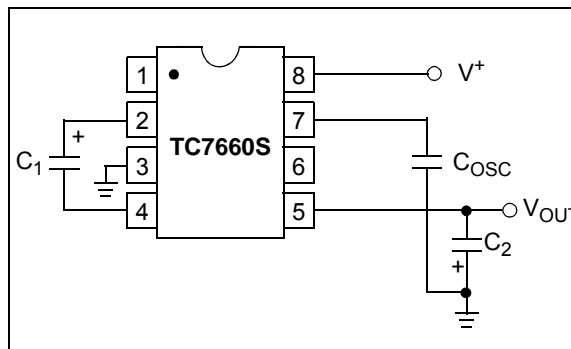


FIGURE 5-5: Lowering Oscillator Frequency.

## 5.5 Positive Voltage Multiplication

The TC7660S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 5-6. In this application, the pump inverter switches of the TC7660S are used to charge  $C_1$  to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage ( $V^+$ ) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$ , or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 5V$  and an output current of 10 mA, it will be approximately 60 $\Omega$ .

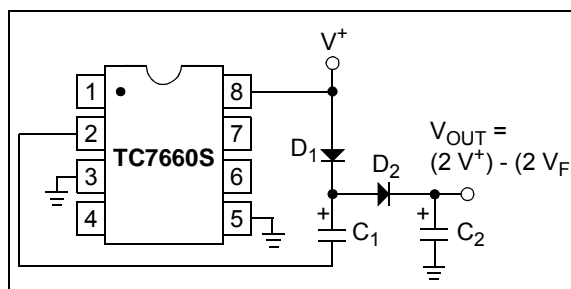
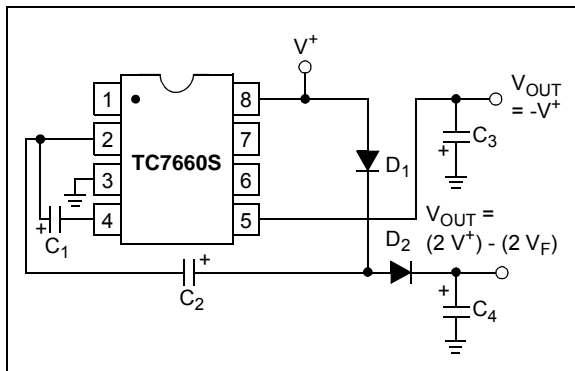


FIGURE 5-6: Positive Voltage Multiplier.

## 5.6 Combined Negative Voltage Conversion and Positive Supply Multiplication

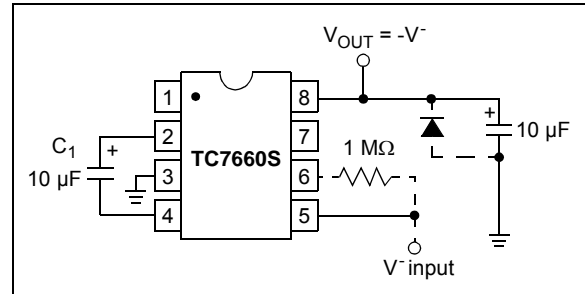
Figure 5-7 combines the functions shown in Figure 5-3 and Figure 5-6 to provide negative voltage conversion and positive voltage multiplication simultaneously. For example, this approach would be suitable for generating +9V and -5V from an existing +5V supply. In this instance, capacitors  $C_1$  and  $C_3$  perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors  $C_2$  and  $C_4$  are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.



**FIGURE 5-7:** Combined Negative Converter and Positive Multiplier.

## 5.7 Efficient Positive Voltage Multiplication/Conversion

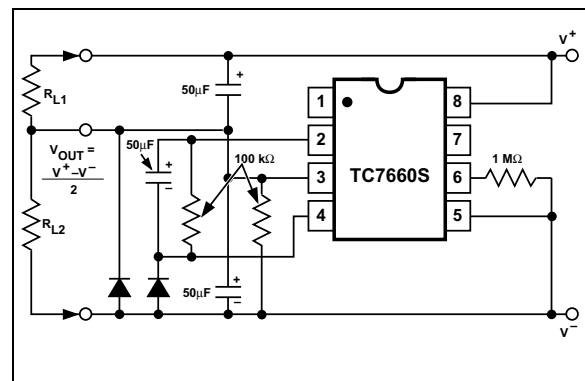
Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 5-8 shows a TC7660S transforming -5V to +5V (or +5V to +10V, etc.). The only problem is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 5-7, could be used to start this circuit up, after which it will bypass the other ( $D_1$  and  $D_2$  in Figure 5-7 would never turn on), or else the diode and resistor shown dotted in Figure 5-8 can be used to “force” the internal regulator on.



**FIGURE 5-8:** Positive Voltage Conversion.

## 5.8 Voltage Splitting

The same bidirectional characteristics used in Figure 5-8 can also be used to split a higher supply in half, as shown in Figure 5-9. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5-3, +15V can be converted (via +7.5V and -7.5V) to a nominal -15V, though with rather high series resistance ( $\sim 250\Omega$ ).



**FIGURE 5-9:** Splitting a Supply in Half.

## 5.9 Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

## 5.10 Negative Supply Generation for 4½ Digit Data Acquisition System

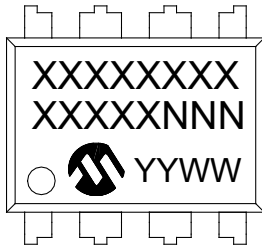
The TC7135 is a 4½ digit ADC operating from  $\pm 5V$  supplies. The TC7660S provides an inexpensive -5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

# TC7660S

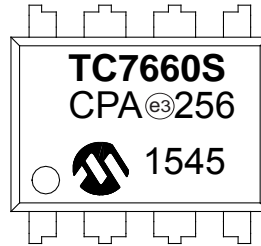
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

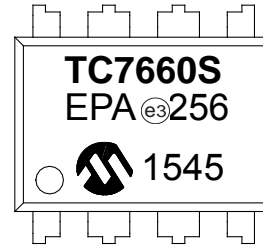
8-Lead PDIP (300 mil)



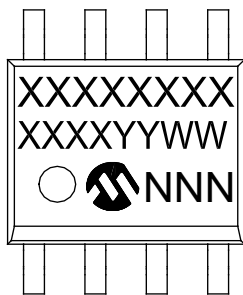
Example



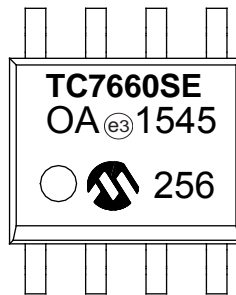
Example



8-Lead SOIC (3.90 mm)



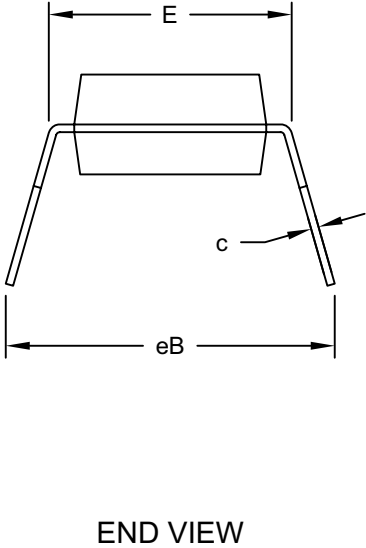
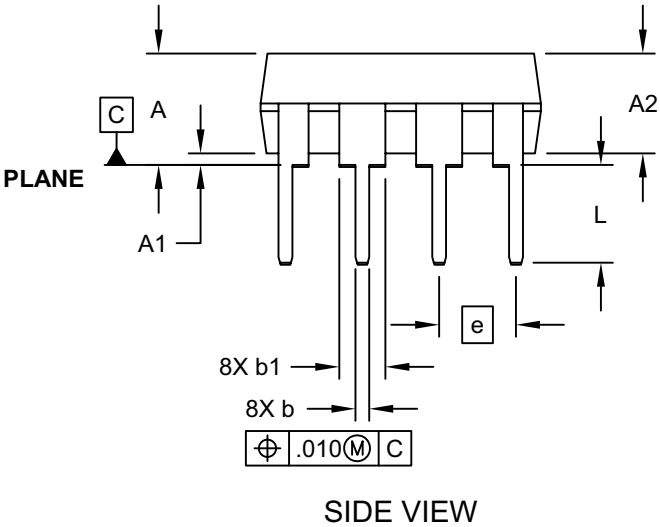
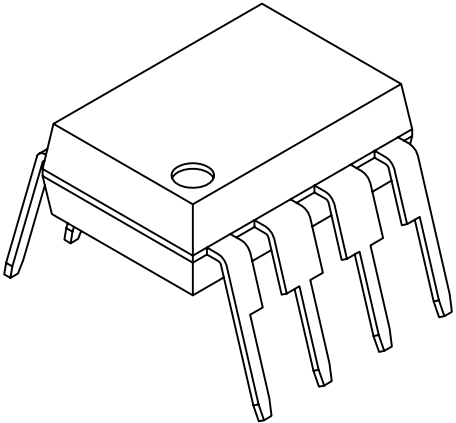
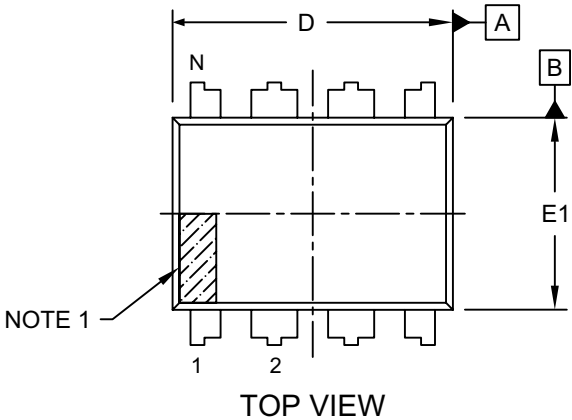
Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

## 8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



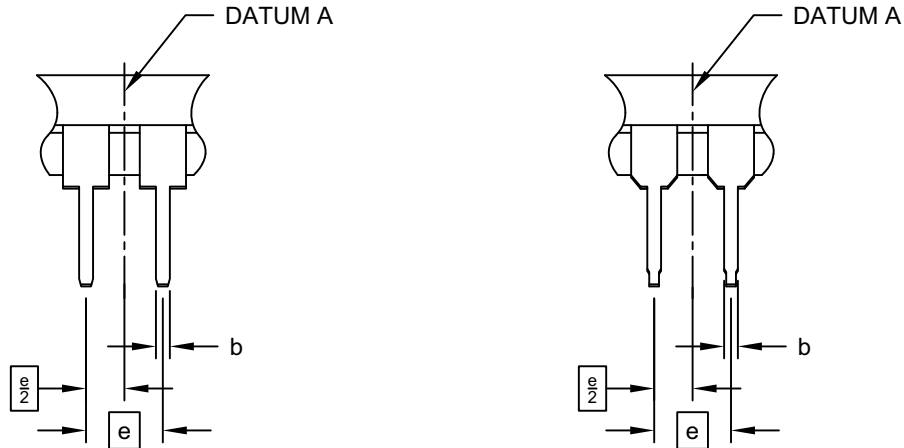
Microchip Technology Drawing No. C04-018D Sheet 1 of 2

# TC7660S

## 8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

### ALTERNATE LEAD DESIGN (VENDOR DEPENDENT)



		Units	INCHES		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		.100 BSC		
Top to Seating Plane	A	-	-		.210
Molded Package Thickness	A2	.115	.130		.195
Base to Seating Plane	A1	.015	-		-
Shoulder to Shoulder Width	E	.290	.310		.325
Molded Package Width	E1	.240	.250		.280
Overall Length	D	.348	.365		.400
Tip to Seating Plane	L	.115	.130		.150
Lead Thickness	c	.008	.010		.015
Upper Lead Width	b1	.040	.060		.070
Lower Lead Width	b	.014	.018		.022
Overall Row Spacing	§	eB	-	-	.430

**Notes:**

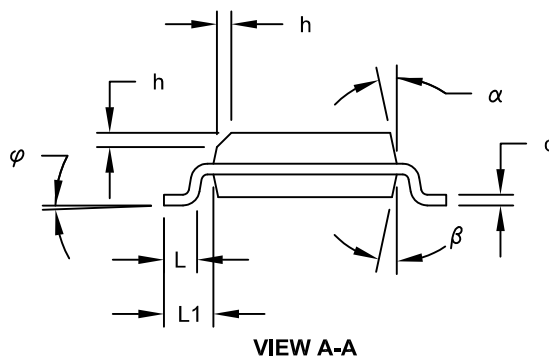
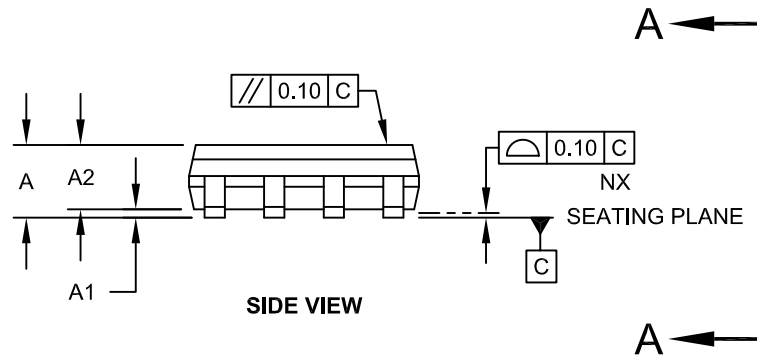
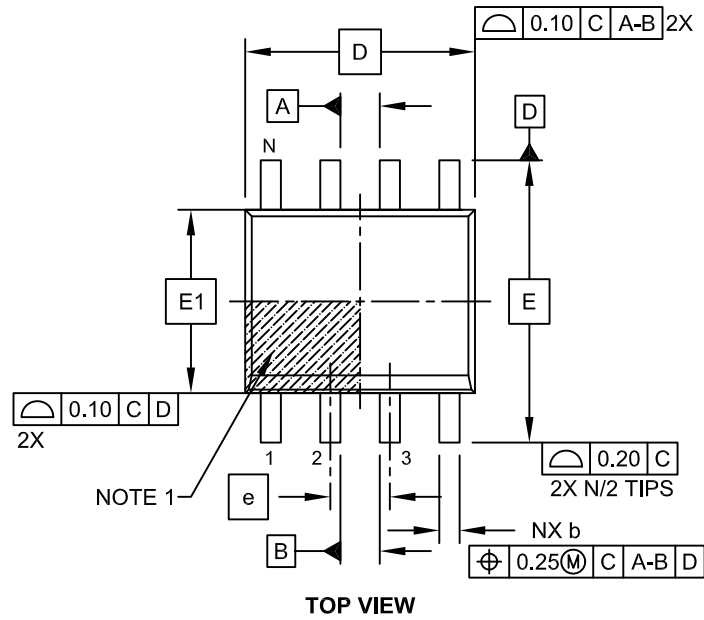
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

## 8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

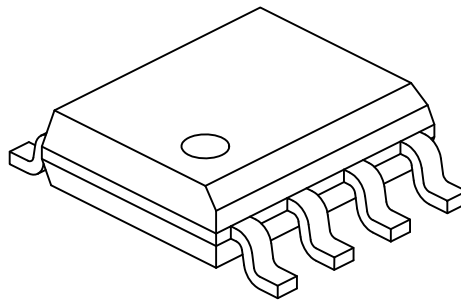


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

# TC7660S

## 8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\varphi$	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	$\alpha$	5°	-	15°
Mold Draft Angle Bottom	$\beta$	5°	-	15°

### Notes:

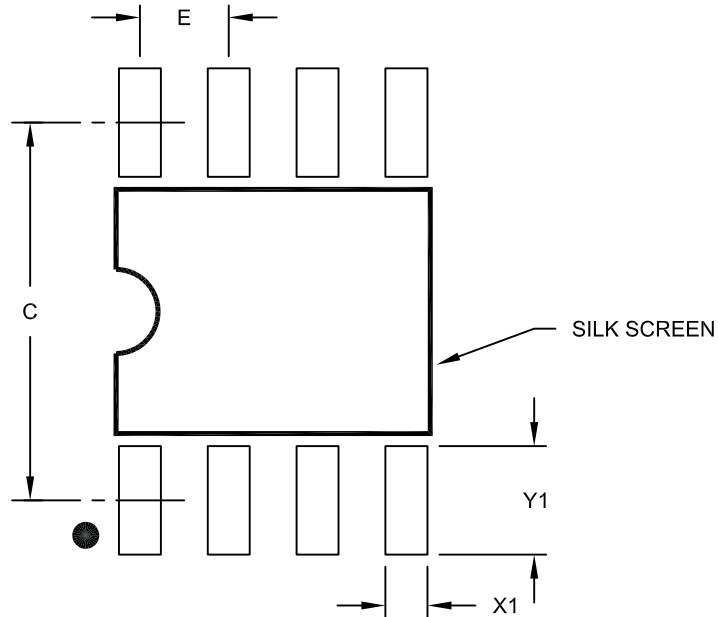
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2



## 8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

# TC7660S

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision C (November 2015)

The following is the list of modifications.

1. Updated **Section 1.0 “Electrical Characteristics”**.
2. Added **Temperature Specifications** table.
3. Updated **Product Identification System** section.
4. Minor typographical errors.

### Revision B (August 2013)

The following is the list of modifications.

1. Added Appendix A and the **“Product Identification System”** page.
2. Updated **Section 6.0 “Packaging Information”**.

### Revision A (May 2001)

- Original release of this document.

# TC7660S

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>[X]<sup>(1)</sup></u>	
Device	Temperature Range	Package	Tape and Reel Option	
<b>Device:</b>	TC7660S: DC-to-DC Voltage Converter			<b>Examples:</b> a) TC7660SCPA: Commercial temperature, PDIP package a) TC7660SCPA: Commercial temperature, PDIP package a) TC7660SEPA: Extended temperature, PDIP package b) TC7660SCOA: Commercial temperature, SOIC package c) TC7660SCOA713: Tape and Reel, Commercial temperature, SOIC package d) TC7660SEOA: Extended temperature, SOIC package e) TC7660SEOA713: Tape and Reel, Extended temperature, SOIC package f) TC7660SEOA723: Reverse Tape and Reel, Extended temperature, SOIC package  <b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
<b>Temperature Range:</b>	C = 0°C to +70°C (Commercial)			
	E = -40°C to +85°C (Extended)			
	V = -40°C to +125°C (Various)			
<b>Package:</b>	PA = 8-Lead Plastic Dual In-Line - 300 mil Body (PDIP)			
	OA = 8-Lead Plastic Small Outline - Narrow, 3.90 mm Body (SOIC)			
<b>Tape and Reel</b>	Blank = Tube			
	713 = Tape and Reel (SOIC only)			
	723 = Reverse Tape and Reel (SOIC only)			

# TC7660S

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NOTES:

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