N-Channel Enhancement-Mode Vertical DMOS FETs

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

The Supertex VN2210 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		Wafer / Die Options		
	TO-39	TO-92	NW (Die in wafer form)	NJ (Die on adhesive tape)	ND (Die in waffle pack)
VN2210	VN2210N2	VN2210N3-G	VN5210NW	VN5210NJ	VN5210ND

For packaged products, -G indicates package is RoHS compliant ('Green'). TO-39 package is RoHS compliant ('Green').
Devices in Wafer / Die form are RoHS compliant ('Green').
Refer to Die Specification VF52 for layout and dimensions.

Product Summary

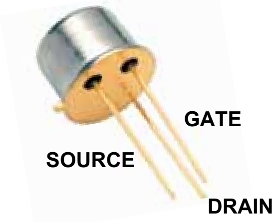
BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)
100	0.35	8.0

Absolute Maximum Ratings

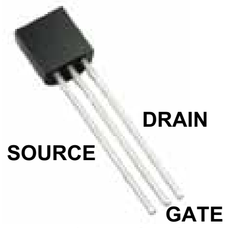
Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configurations

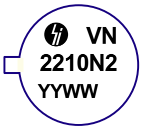


TO-39 (N2)



TO-92 (N3)

Product Marking



YY = Year Sealed
WW = Week Sealed

Package may or may not include the following marks: Si or

TO-39 (N2)

YY = Year Sealed
WW = Week Sealed
—— = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (A)	I_D (pulsed) (A)	Power Dissipation @T_C = 25°C (W)	θ_{JC} (°C/W)	θ_{JA} (°C/W)	I_{DR}† (A)	I_{DRM} (A)
TO-39	1.7	10	6.0	21	125	1.7	10
TO-92	1.2	8.0	1.0	125	170	1.2	8.0

Notes:

† *I_D (continuous) is limited by max rated T_j.*

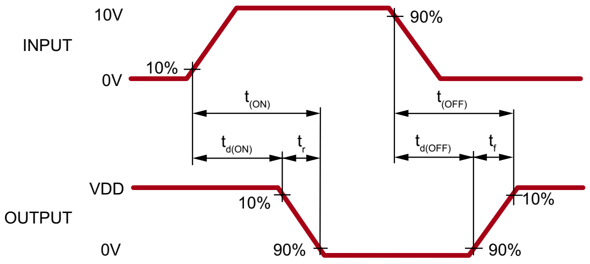
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

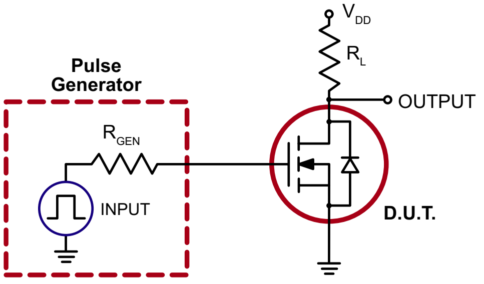
Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	100	-	-	V	V_{GS} = 0V, I_D = 10mA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	50	μA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	10	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	3.0	4.5	-	A	V_{GS} = 5.0V, V_{DS} = 25V
		8.0	17	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	0.4	0.5	Ω	V_{GS} = 5.0V, I_D = 1.0A
		-	0.27	0.35		V_{GS} = 10V, I_D = 4.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.85	1.2	%/°C	V_{GS} = 10V, I_D = 4.0A
G_{FS}	Forward transconductance	1200	-	-	mmho	V_{DS} = 25V, I_D = 2.0A
C_{ISS}	Input capacitance	-	300	500	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	125	200		
C_{RSS}	Reverse transfer capacitance	-	50	65		
$t_{d(ON)}$	Turn-on time	-	10	15	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 10Ω
t_r	Rise time	-	10	15		
$t_{d(OFF)}$	Turn-off time	-	50	65		
t_f	Fall time	-	30	50		
V_{SD}	Diode forward voltage drop	-	1.0	1.6	V	V_{GS} = 0V, I_{SD} = 4.0A
t_{rr}	Reverse recovery time	-	500	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

Notes:

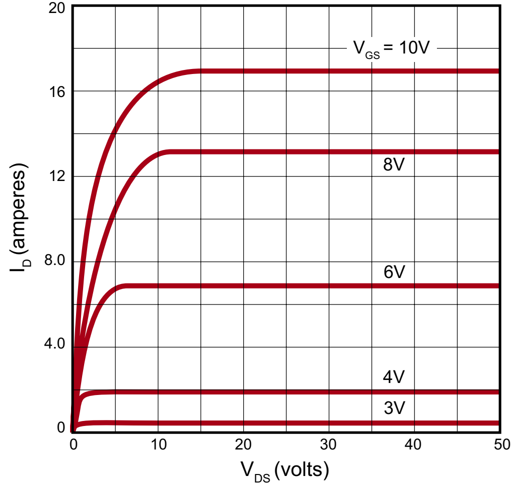
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

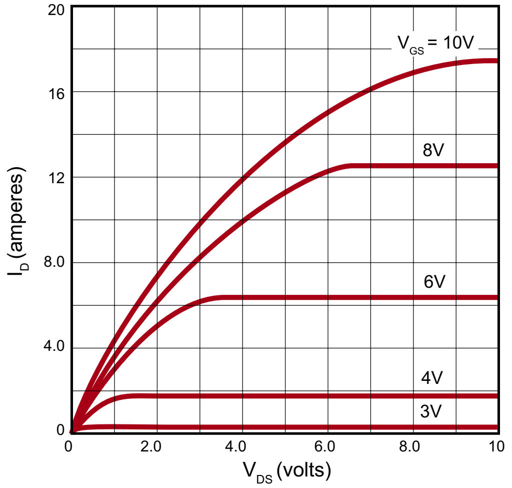
Switching Waveforms and Test Circuit

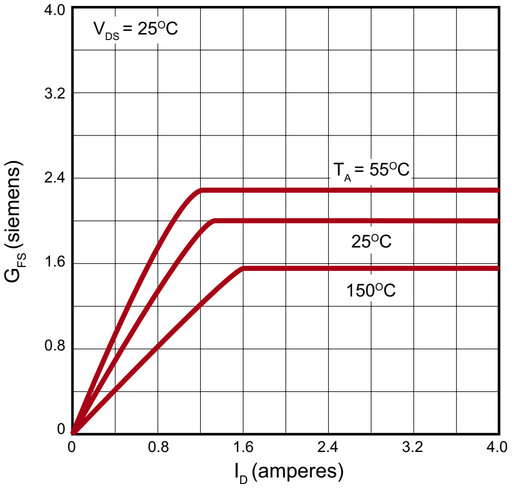


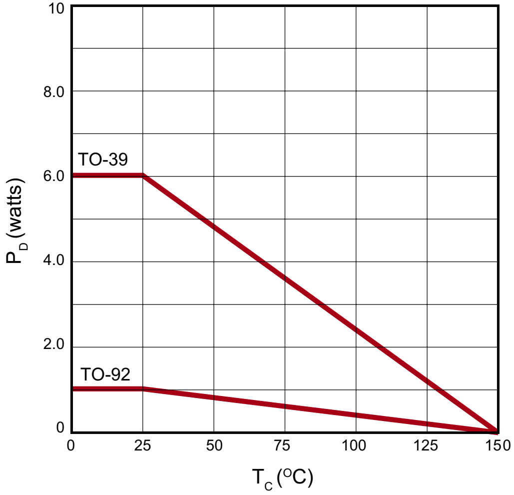


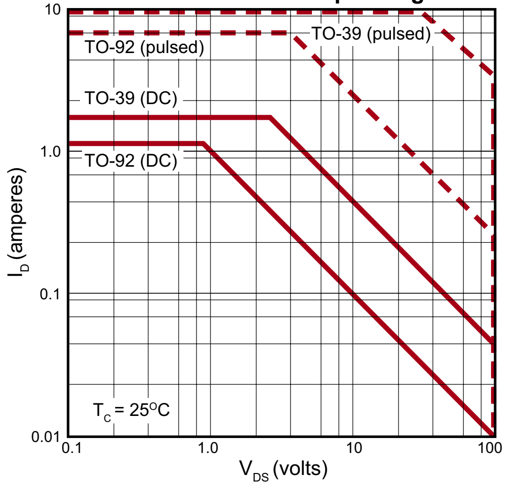
Typical Performance Curves

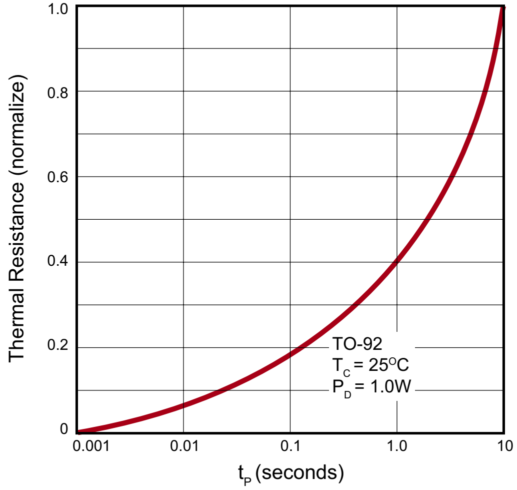

Output Characteristics


Saturation Characteristics


Transconductance vs. Drain Current

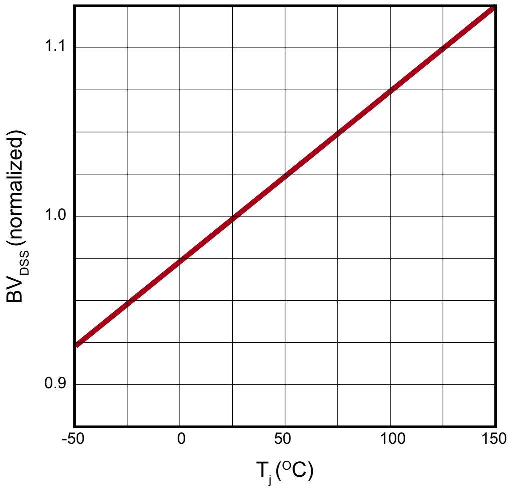

Power Dissipation vs. Case Temperature


Maximum Rated Safe Operating Area

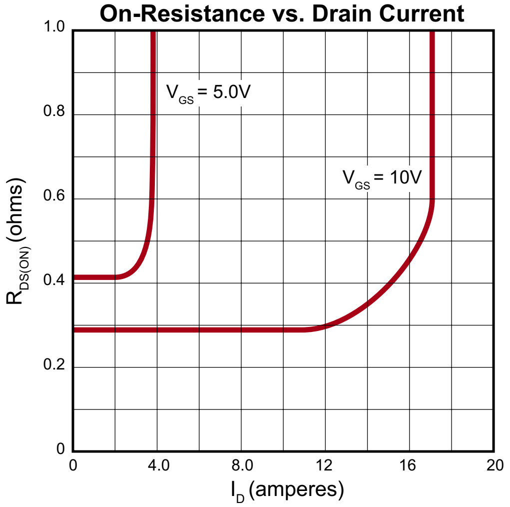

Thermal Response Characteristics

Typical Performance Curves *(cont.)*

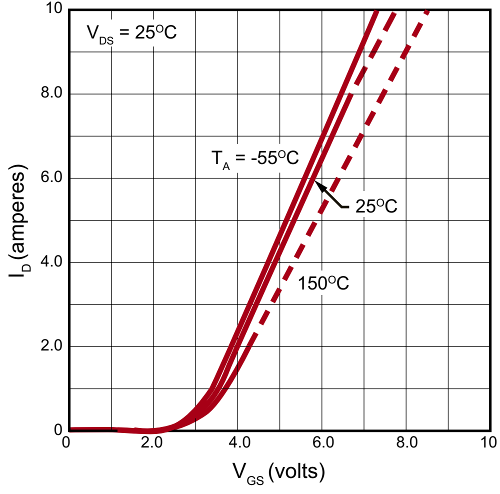
BV_{DSS} Variation with Temperature



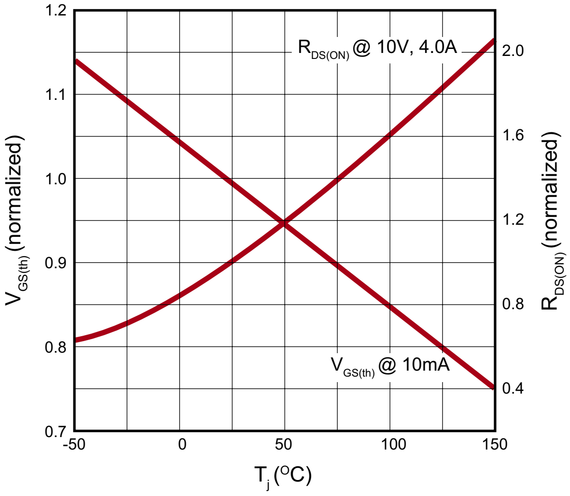
On-Resistance vs. Drain Current



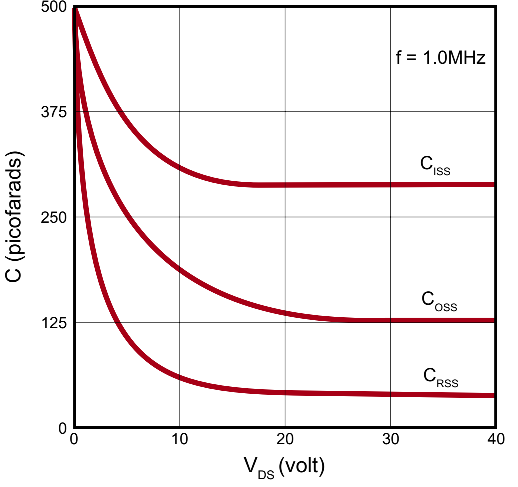
Transfer Characteristics



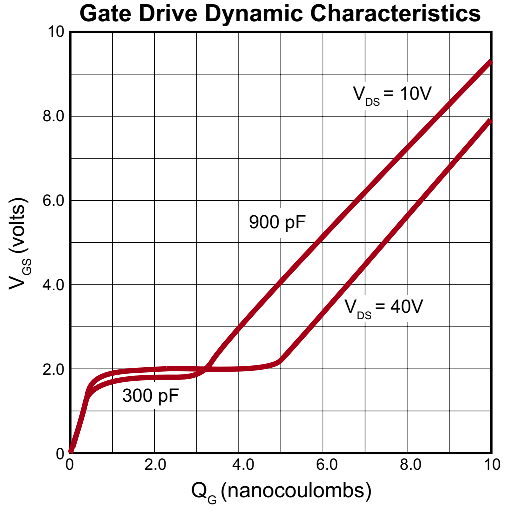
V_{GS} and RV_{DS} Variation with Temperature



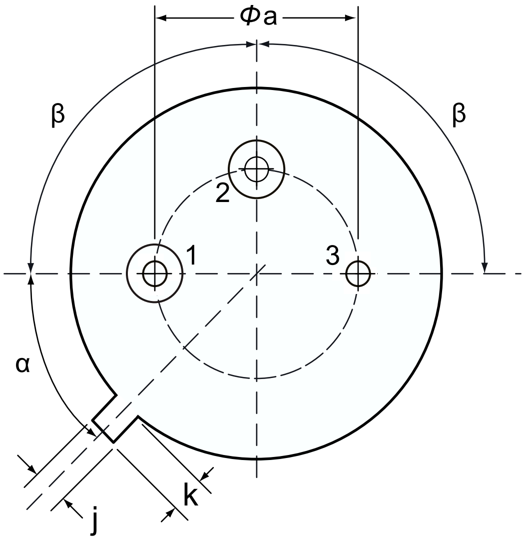
Capacitance vs. Drain-to-Source Voltage



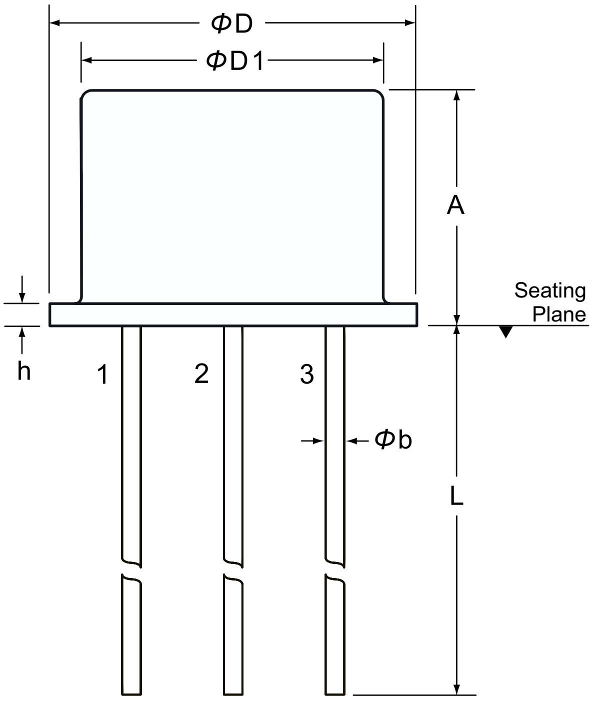
Gate Drive Dynamic Characteristics



3-Lead TO-39 Package Outline (N2)



Bottom View

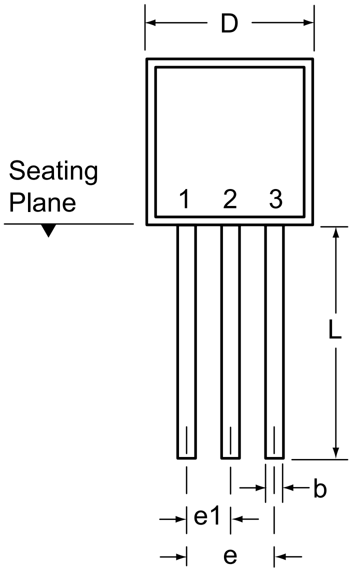


Side View

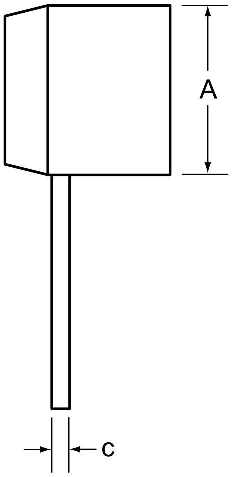
Symbol		α	β	A	Φa	Φb	ΦD	ΦD1	h	j	k	L
Dimension (inches)	MIN	45° NOM	90° NOM	.240	.190	.016	.350	.315	.009	.028	.029	.500
	NOM			-	-	-	-	-	-	-	-	-
	MAX			.260	.210	.021	.370	.335	.125	.034	.040	.560*

JEDEC Registration TO-39.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-3TO39N2, Version B052009.*

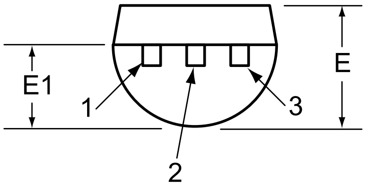
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)