DSC2031

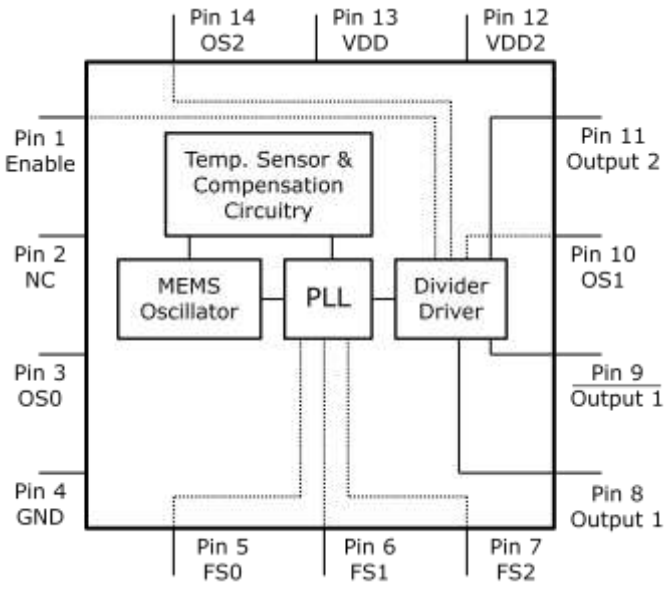
Low-Jitter Configurable Dual LVDS-CMOS Oscillator

General Description

The DSC2031 series of high performance dual output oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The two outputs are controlled by separate supply voltages to allow for independent voltage level control. The frequencies of the outputs can be identical or independently derived from a common PLL frequency source. The DSC2031 has provision for up to eight user-defined pre-programmed, pin-selectable output frequency combinations. The DSC2031 is also equipped with independent pin-selectable output drive strengths for the CMOS output to reduce EMI and noise.

DSC2031 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Industrial.

Block Diagram



Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Two Independent Outputs**
  - LVDS and CMOS
- **Pin-Selectable Configurations**
  - 3-bit Output Drive Strength (CMOS)
  - 3-bit Output Frequency Combinations
- **Short Lead Times: 2 Weeks**
- **Wide Frequency Range**
  - LVDS Output: 2.3 to 460 MHz
  - CMOS Output: 2.3 to 170 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables (tri-state) them when low
2	NC	NA	Leave unconnected or grounded
3	OS0	I	Least significant bit for output drive strength selection for CMOS
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Middle bit for frequency selection
7	FS2	I	Most significant bit for frequency selection
8	Output1+	O	Positive LVDS Output 1
9	Output1-	O	Negative LVDS Output 1
10	OS1	I	Middle bit for output drive strength selection for CMOS
11	Output 2	O	CMOS output
12	VDD2	Power	Power Supply 2 for CMOS Output
13	VDD	Power	Power Supply
14	OS2	I	Most significant bit for output drive strength selection for CMOS

Operational Description

The DSC2031 is a dual output LVDS-CMOS oscillator consisting of a MEMS resonator and a support PLL IC. The two outputs, CMOS and LVDS, are generated through independent 8-bit programmable dividers from the output of the internal PLL. Two constraints are imposed on the output frequencies: 1) $f_2=M \times f_1/N$, where M and N are even integers between 4 and 254, 2) $1.2GHz < N \times f_2 < 1.7GHz$.

The actual frequencies output by the DSC2031 are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0 – FS2) select the output frequency combination. Discera supports customer defined versions of the DSC2031. Standard frequency options are described in in the following sections.

The DSC2031 provides control of the output voltage levels of the CMOS output. VDD2 (pin 12) sets the high voltage level of Output 2 and must be equal to or less than VDD at all times to insure proper operation. VDD2 can be as low as 1.65V.

When Enable (pin 1) is floated or connected to VDD, the DSC2031 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

The DSC2031 has programmable output drive strength for CMOS output. Using three control pins (OS0-OS2), the drive strength for CMOS output (output 2) can be adjusted to match circuit board impedances to reduce power supply noise, overshoot/undershoot and EMI. Table 1 displays typical rise / fall times for the output with a 15pf load capacitance as a function of these control pins at VDD=3.3V and room temperature.

Table 1. Rise/Fall times for drive strengths

	Output Drive Strength Bits [OS2, OS1, OS0] - Default [**111**]							
	000	001	010	011	100	101	110	**111**
tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	**1.1**
tf (ns)	2.5	2.4	2.4	2	1.8	1.6	1.3	**1.3**

Output Clock Frequencies

Table 2 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code above. Customer defined combinations are available.

Table 2. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Freq Select Bits [FS2, FS1, FS0] – **Default is [111]**							
		000	001	010	011	100	101	110	**111**
J0001	f_{OUT1}	148.25	74.25	156.25	150	125	125	100	**100**
	f_{OUT2}	74.25	74.25	125	125	25	50	50	**75**
J000X	f_{OUT1}	Contact factory for additional configurations.							
	f_{OUT2}								

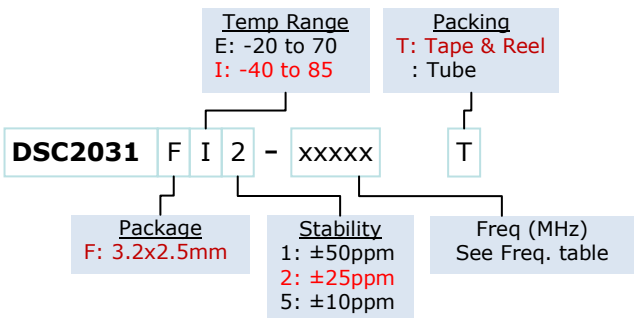
Frequency select bit are weakly tied high so if left unconnected the default setting will be [111] and the device will output the associated frequency highlighted in **Bold**.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Ordering Code

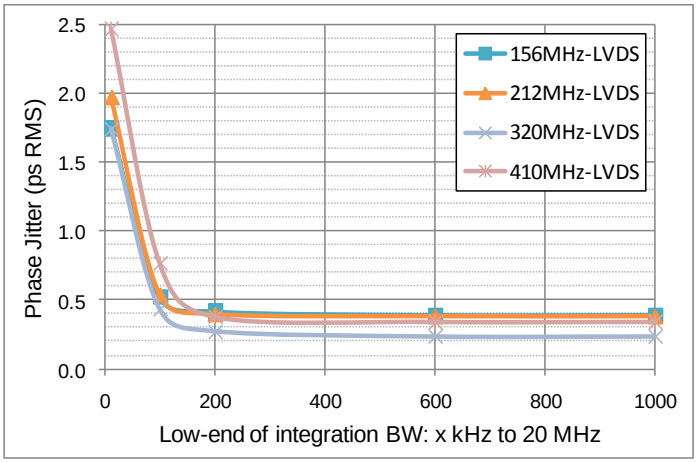


Specifications (Unless specified otherwise: T=25° C, max CMOS drive strength)

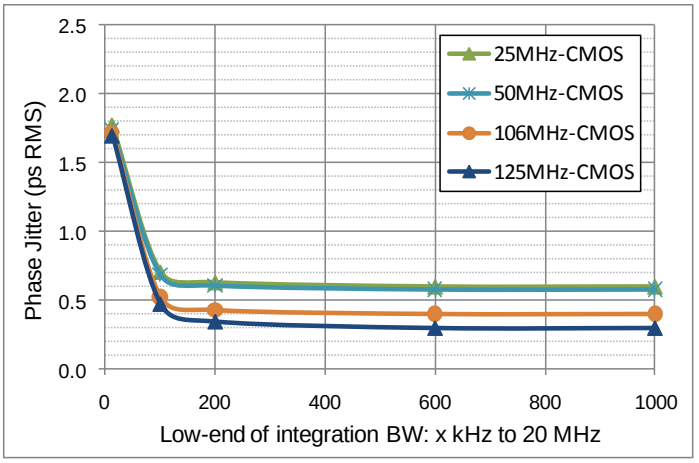
Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current[2]	I_{DD}	EN pin high – outputs are enabled LVDS: R_L=100Ω, F_{O1}=125 MHz CMOS: C_L=15pF, F_{O2}=75 MHz		49		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kΩ
LVDS Output						
Output Offset Voltage		R=100Ω Differential	1.125		1.4	V
Delta Offset Voltage					50	mV
Pk to Pk Output Swing		Single-Ended		350		mV
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=100Ω, C_L= 2pF (to GND)		200	350	ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	J_{PER}	F_{O1}=125 MHz		2.5		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.28 0.4 1.7	 2	ps_{RMS}
CMOS Output						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	I=±6mA	 0.9xV_{DD} -		 - 0.1xV_{DD}	V
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% C_L=15pf		 1.1 1.3	 2 2	ns
Frequency	f_0	Commercial/Industrial temp range	2.3		170	MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	J_{PER}	F_{O2}=125 MHz		3		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	ps_{RMS}

Notes:
1. Pin 4 V_{DD} should be filtered with 0.01uf capacitor.
2. Output is enabled if Enable pad is floated or not connected.
3. t_{su} is time to stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

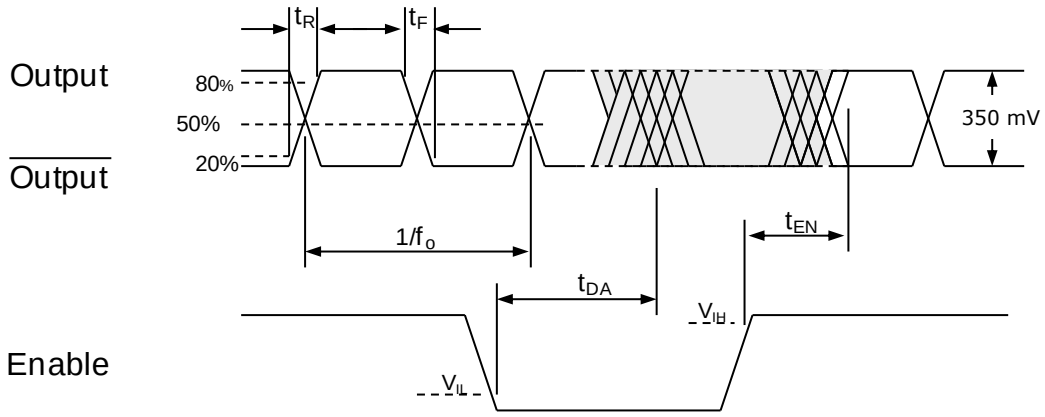


LVDS Phase jitter (integrated phase noise)

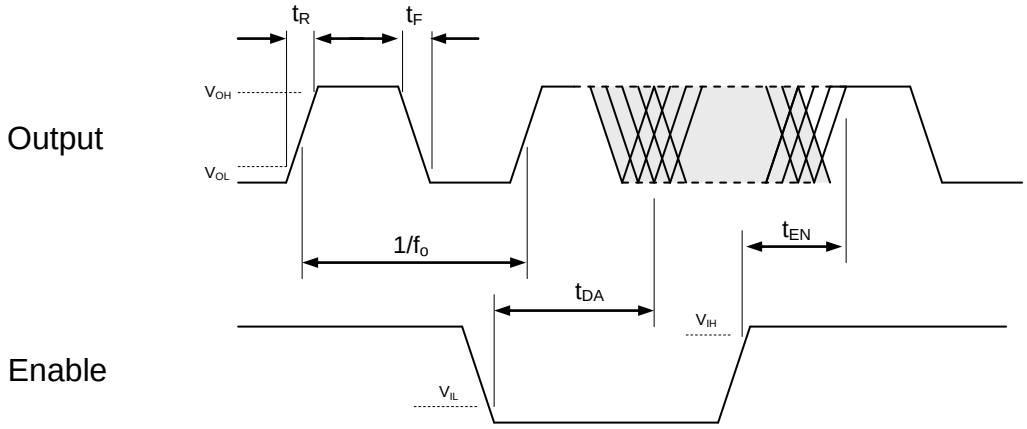


CMOS Phase jitter (integrated phase noise)

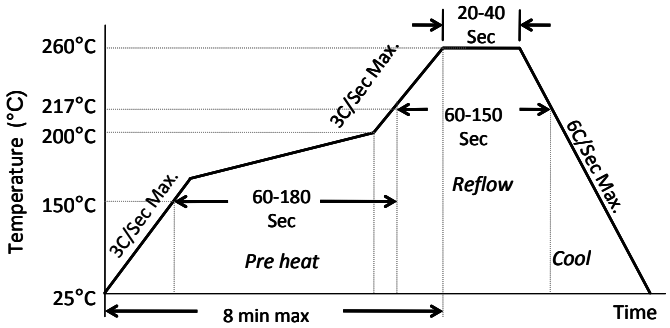
Output Waveform: LVDS



Output Waveform: CMOS



Solder Reflow Profile

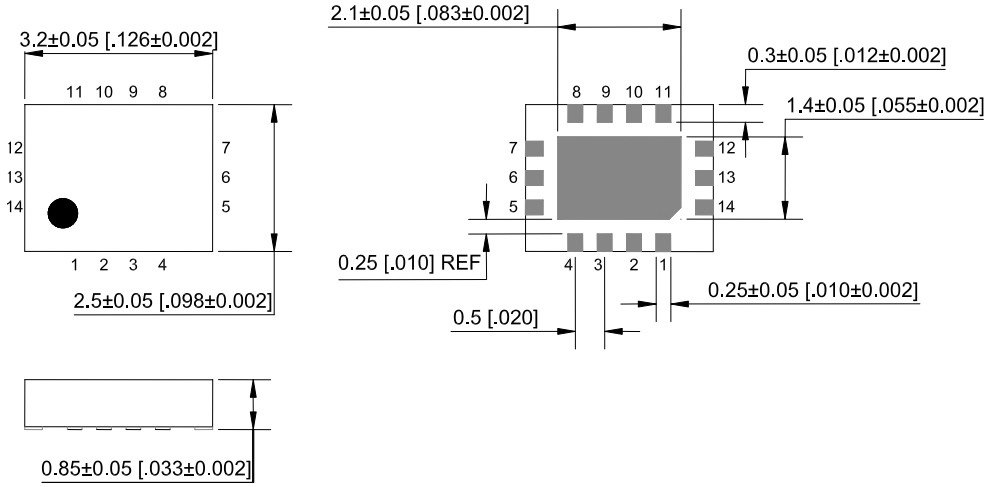


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

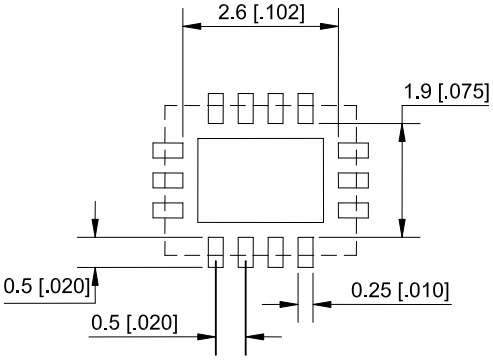
Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

External Dimensions
units: mm[inch]



Recommended
Solder Pad Layout
units: mm[inch]



Disclaimer:

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

MICREL, Inc. • **2180 Fortune Drive,** **San Jose, California 95131** • **USA**
Phone: +1 (408) 944-0800 • **Fax: +1 (408) 474-1000** • **Email: hbwhelp@micrel.com** • **www.micrel.com**