HV5812

20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid

Features

- HVCMOS® Technology for High Performance
- Operating Voltage of up to 80V
- High-speed Source Driver
- 5V CMOS Logic Circuitry
- Up to 5 MHz Data Input Rate
- Excellent Noise Immunity
- Flexible High-voltage Supplies

Applications

- Display Driver

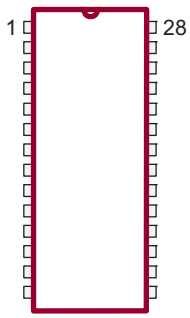
General Description

The HV5812 is a 20-channel serial-input vacuum fluorescent display driver. It combines a 20-bit CMOS shift register, data latches and control circuitry with high-voltage MOSFET outputs. The HV5812 is primarily designed for vacuum fluorescent displays.

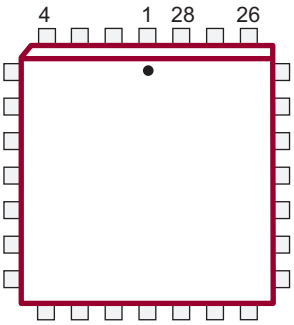
The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Data input rates are typically over 5 MHz with 5V logic supply. Especially useful for interdigit blanking, the blanking input disables the output source drives and turns on the sink drivers. Using with TTL may require external pull-up resistors to ensure an input logic high.

Package Types

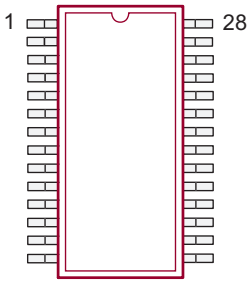
28-lead PDIP
(Top view)



28-lead PLCC
(Top view)

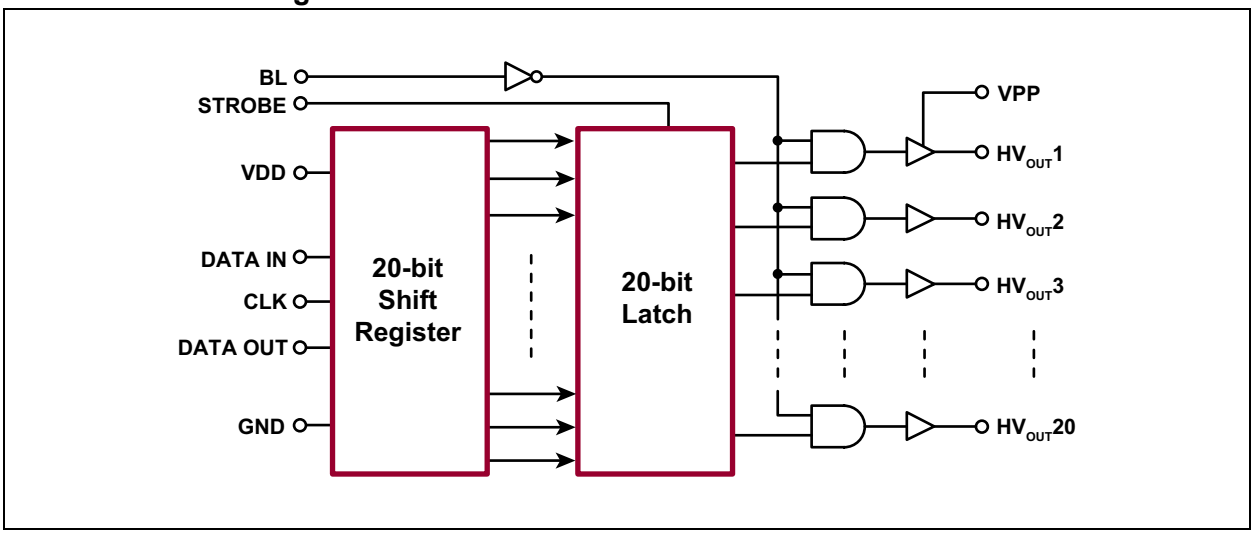


28-lead SOW
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} ..... –0.5V to +7.5V
Supply Voltage, V_{PP} ..... –0.5V to +90V
Logic Input Levels ..... –0.3V to V_{DD} +0.3V
Maximum Operating Junction Temperature ..... +125°C
Storage Temperature ..... –55°C to +150°C
Power Dissipation:
- 28-lead PDIP ..... 2000 mW
- 28-lead PLCC ..... 1900 mW
- 28-Lead SOW ..... 1700 mW

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	4.5	—	5.5	V	
Supply Voltage	V_{PP}	20	—	80	V	
Operating Junction Temperature	T_J	–40	—	+125	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions; T_A = 25°C unless otherwise indicated.

Parameter	Sym.		Min.	Typ.	Max.	Unit	Conditions
Output Leakage Current	I_{DSS}		—	–5	–15	µA	V_{OUT} = 0V, T_A = +70°C
High-level Output	V_{OH}	HV_{OUT}	78	78.5	—	V	I_{OUT} = –25 mA, V_{PP} = 80V, T_J = +25°C
			77	78	—		I_{OUT} = –25 mA, V_{PP} = 80V, T_J = +125°C
		DATA OUT	4.5	4.7	—	V	I_{OUT} = –200 µA, V_{DD} = 5V
Low-level Output	V_{OL}	HV_{OUT}	—	1.5	3	V	I_{OUT} = 1 mA, T_J = +25°C, V_{DD} = 5V
			—	2.3	4		I_{OUT} = 1 mA, T_J = +125°C, V_{DD} = 5V
		DATA OUT	—	200	250	V	I_{OUT} = +200 µA, V_{DD} = 5V
Output Pull-down Current	I_{SINK}		2	3.5	—	mA	V_{OUT} = 5V to V_{PP}, V_{DD} = 5V
High-level Logic Input Voltage	V_{IH}		3.5	—	5.3	V	V_{DD} = 5V
Low-level Logic Input Voltage	V_{IL}		–0.3	—	0.8	V	
High-level Logic Input Current	I_{IH}		—	0.05	0.5	µA	V_{IN} = V_{DD}, V_{DD} = 5V
Low-level Logic Input Current	I_{IL}		—	–0.05	–0.5	µA	V_{IN} = 0.8V, V_{DD} = 5V
Quiescent V_{DD} Supply Current	I_{DDQ}		—	100	300	µA	All outputs high, V_{DD} = 5V
			—	100	300		All outputs low, V_{DD} = 5V
Quiescent V_{PP} Supply Current	I_{PPQ}		—	10	100	µA	All outputs high, no load
			—	10	100		All outputs low, no load

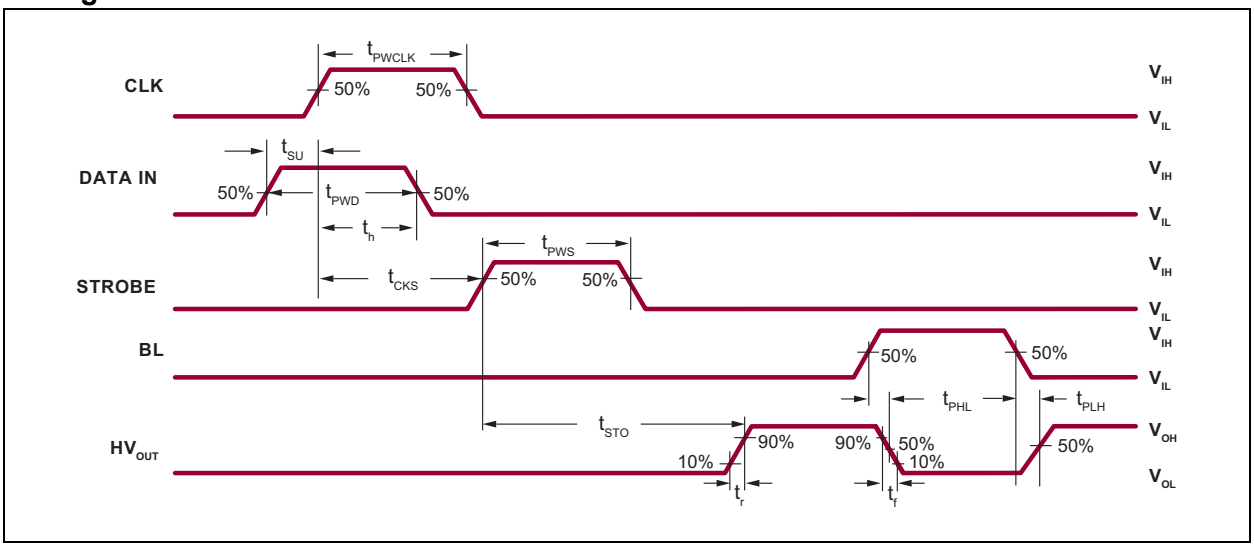
AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions; T_A = 25°C unless otherwise indicated.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Blanking to Output Delay	t_{PHL}	—	2000	—	ns	C_L = 30 pF, 50% to 50%, V_{DD}=5V
	t_{PLH}	—	1000	—		
Output Fall Time	t_r	—	1450	—	ns	C_L = 30 pF, 90% to 10%, V_{DD} = 5V
Output Rise Time	t_f	—	650	—	ns	C_L = 30 pF, 10% to 90%, V_{DD} = 5V
Data Set-up Time	t_{SU}	75	—	—	ns	See **Timing Waveforms**.
Data Hold Time	t_H	75	—	—	ns	See **Timing Waveforms**.
Minimum Data Pulse Width	t_{PWD}	150	—	—	ns	See **Timing Waveforms**.
Minimum Clock Pulse Width	t_{PWCLK}	150	—	—	ns	See **Timing Waveforms**.
Minimum Time between Clock Activation and Strobe	t_{CKS}	300	—	—	ns	See **Timing Waveforms**.
Minimum Strobe Pulse Width	t_{PWS}	100	—	—	ns	See**Timing Waveforms**.
Typical Time between Strobe Activation and Output Transition	t_{STO}	—	500	—	ns	See **Timing Waveforms**.
Maximum Clock Frequency	f_{CLK}	—	8	—	MHz	T_J = +25°C, V_{DD} = 5V
		—	5	—		T_J = +125°C, V_{DD} = 5V

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
28-lead PDIP	θ_{JA}	—	43	—	°C/W	
28-lead PLCC	θ_{JA}	—	48	—	°C/W	
28-lead SOW	θ_{JA}	—	55	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV5812 28-lead PDIP, 28-lead PLCC and 28-lead SOW are listed on Table 2-1. Refer to **Package Types** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VPP	High-voltage power rail
2	Data Out	Serial data output. Data output for cascading to the data input of the next device.
3	$HV_{OUT}20$	High-voltage output
4	$HV_{OUT}19$	High-voltage output
5	$HV_{OUT}18$	High-voltage output
6	$HV_{OUT}17$	High-voltage output
7	$HV_{OUT}16$	High-voltage output
8	$HV_{OUT}15$	High-voltage output
9	$HV_{OUT}14$	High-voltage output
10	$HV_{OUT}13$	High-voltage output
11	$HV_{OUT}12$	High-voltage output
12	$HV_{OUT}11$	High-voltage output
13	BLANKING	Blank
14	GND	Logic and high-voltage ground
15	CLOCK	Data shift register clock
16	STROBE	Strobe
17	$HV_{OUT}10$	High-voltage output
18	$HV_{OUT}9$	High-voltage output
19	$HV_{OUT}8$	High-voltage output
20	$HV_{OUT}7$	High-voltage output
21	$HV_{OUT}6$	High-voltage output
22	$HV_{OUT}5$	High-voltage output
23	$HV_{OUT}4$	High-voltage output
24	$HV_{OUT}3$	High-voltage output
25	$HV_{OUT}2$	High-voltage output
26	$HV_{OUT}1$	High-voltage output
27	Data In	Serial data input
28	VDD	Low-voltage logic power rail

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV5812:

POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove V_{PP}.
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, etc.) to a known state	3	Remove V_{DD}.
4	Apply V_{PP}. (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} during operation.

FUNCTION TABLE (Note 1)

Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	Strobe Input	Latch Contents				Blanking	Output Contents			
		I_1	I_2	I_3... I_{N-1}	I_N			I_1	I_2	I_3... I_{N-1}	I_N		I_1	I_2	I_3... I_{N-1}	I_N
H	L to H	H	R_1	R_2...R_{N-2}	R_{N-1}	R_{N-1}	—	—	—	—	—	—	—	—	—	—
L	L to H	L	R_1	R_2...R_{N-2}	R_{N-1}	R_{N-1}	—	—	—	—	—	—	—	—	—	—
X	H to L	R_1	R_2	R_3...R_{N-1}	R_N	R_N	—	—	—	—	—	—	—	—	—	—
—	—	X	X	X...X	X	X	L	R_1	R_2	R_3...R_{N-1}	R_N	—	—	—	—	—
—	—	P_1	P_2	P_3...P_{N-1}	P_N	P_N	H	P_1	P_2	P_3...P_{N-1}	P_N	L	P_1	P_2	P_3...P_{N-1}	P_N
—	—	—	—	—	—	—	—	X	X	X...X	X	H	L	L	L...L	L

Note 1: L = Low logic level
H = High logic level
X = Irrelevant
P = Present state
R = Previous state

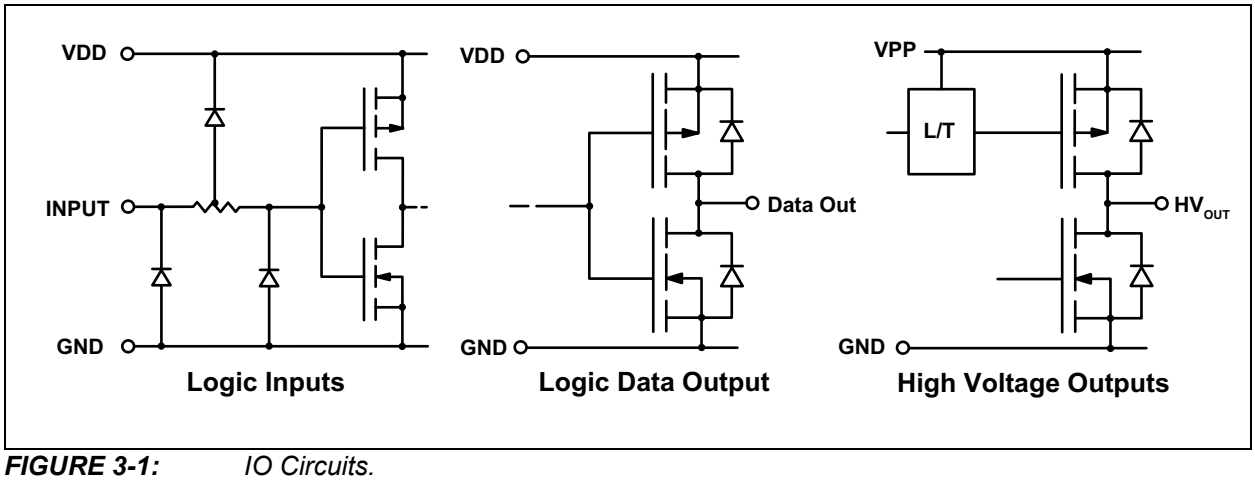


FIGURE 3-1: *IO Circuits.*

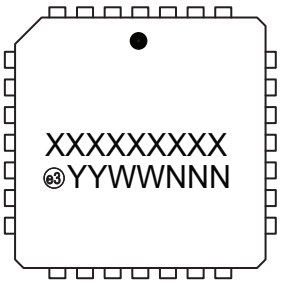
4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

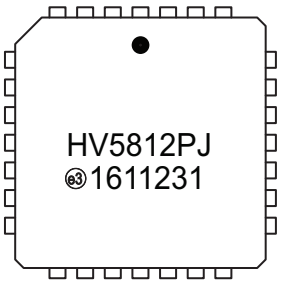
28-lead PDIP

Example

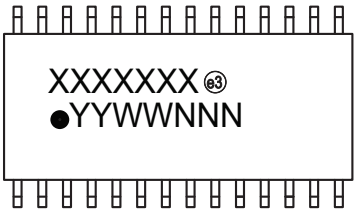
28-lead PLCC



Example



28-lead SOW



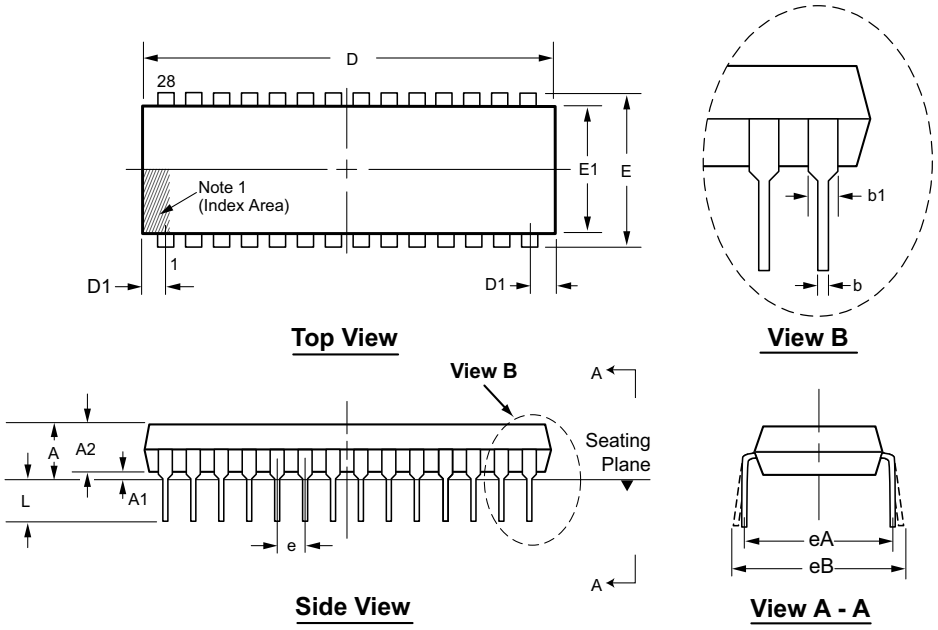
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

28-Lead PDIP (.600in Row Spacing) Package Outline (P)

1.565x.580in body, .250in height (max), .100in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

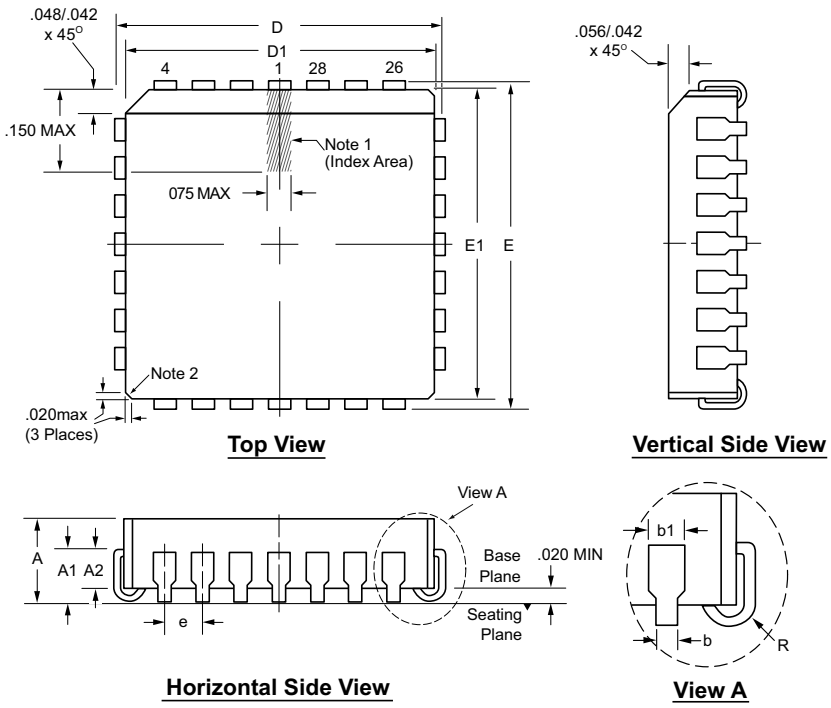
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	eA	eB	L
Dimension (inches)	MIN	.140*	.015	.125	.014	.030	1.380	.065†	.590†	.485	.100 BSC	.600 BSC	.600*	.115
	NOM	-	-	-	-	-	-	-	-	-			-	-
	MAX	.250	.055*	.195	.023†	.070	1.565	.085*	.625	.580			.700	.200

JEDEC Registration MS-011, Variation AB, Issue B, June, 1988.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

28-Lead PLCC Package Outline (PJ)

.453x.453in. body, .180in. height (max), .050in. pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

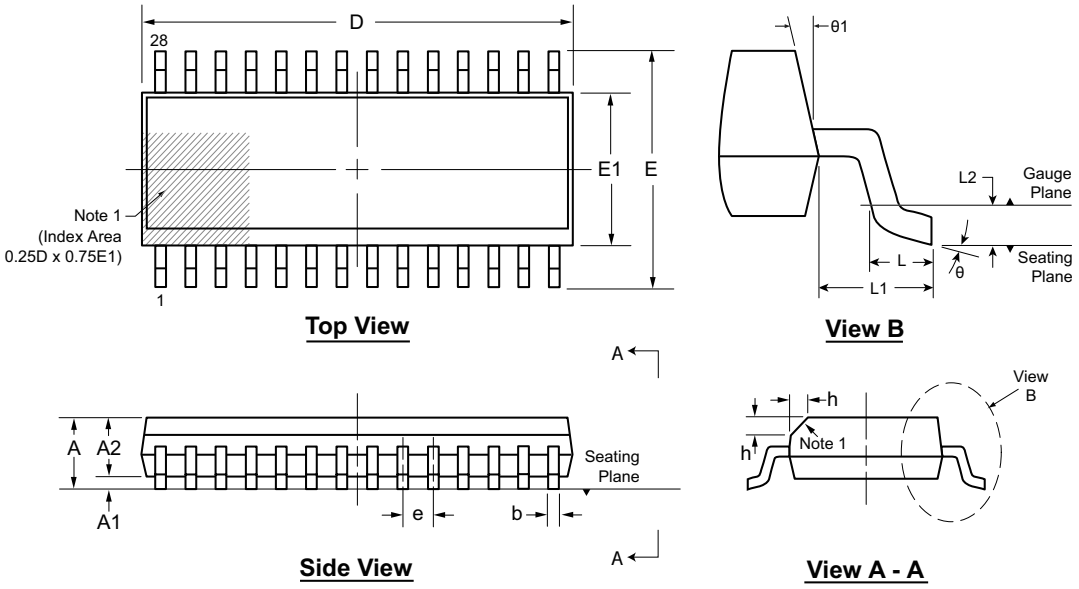
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC	.025
	NOM	.172	.105	-	-	-	.490	.453	.490	.453		.035
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456		.045

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.
Drawings not to scale.

28-Lead SOW (Wide Body) Package Outline (WG)

17.90x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	17.70*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	17.90	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	18.10*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AE, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Supertex Doc# DSFP-HV5812 to Microchip DS20005629A
- Changed the packaging quantity of 28-lead PLCC (PJ M904) from 500/Reel to 750/Reel and 28-lead SOW (WG) from 1000/Reel to 1600/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV5812	=	20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid
Packages:	P	=	28-lead PDIP
	PJ	=	28-lead PLCC
	WG	=	28-lead SOW
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	13/Tube for a P Package
		=	38/Tube for a PJ Package
		=	1600/Reel f or a WG Package
	M904	=	750/Reel for a PJ Package

Examples:

a) HV5812P-G: 20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid, 28-lead PDIP, 13/Tube

b) HV5812PJ-G: 20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid, 28-lead PLCC, 38/Tube

c) HV5812PJ-G-M904: 20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid, 28-lead PLCC, 750/Reel

d) HV5812WG-G: 20-Channel Serial-Input Vacuum Fluorescent Display Driver for Anode or Grid, 28-lead SOW, 1600/Reel

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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