MCP660/1/2/3/4/5/9

60 MHz, 6 mA Op Amps

Features

- Gain Bandwidth Product: 60 MHz (typical)
- Short Circuit Current: 90 mA (typical)
- Noise: 6.8 nV/√Hz (typical, at 1 MHz)
- Rail-to-Rail Output
- Slew Rate: 32 V/µs (typical)
- Supply Current: 6.0 mA (typical)
- Power Supply: 2.5V to 5.5V
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Driving A/D Converters
- Power Amplifier Control Loops
- Barcode Scanners
- Optical Detector Amplifier

Design Aids

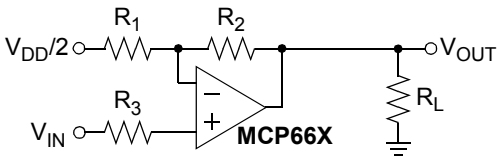
- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description

The Microchip Technology, Inc. MCP660/1/2/3/4/5/9 family of operational amplifiers (op amps) features high gain bandwidth product (60 MHz, typical) and high output short circuit current (90 mA, typical). Some also provide a Chip Select pin ($\overline{CS}$) that supports a low power mode of operation. These amplifiers are optimized for high speed, low noise and distortion, single-supply operation with rail-to-rail output and an input that includes the negative rail.

This family is offered in single (MCP661), single with $\overline{CS}$ pin (MCP663), dual (MCP662) and dual with two $\overline{CS}$ pins (MCP665), triple (MCP660), quad (MCP664) and quad with two $\overline{CS}$ pins (MCP669). All devices are fully specified from -40°C to +125°C.

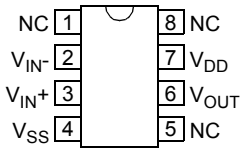
Typical Application Circuit



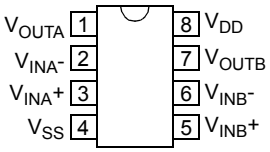
Power Driver with High Gain

Package Types

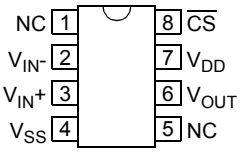
MCP661
SOIC



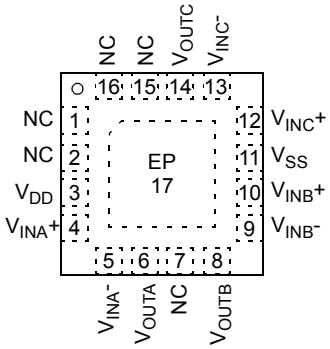
MCP662
SOIC



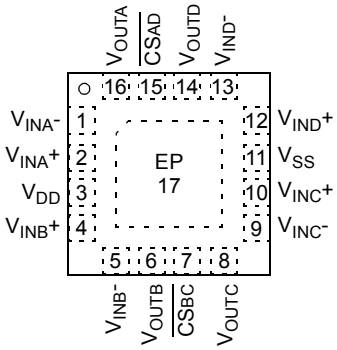
MCP663
SOIC



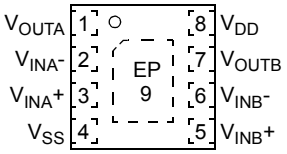
MCP660
4x4 QFN*



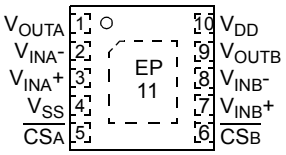
MCP669
4x4 QFN*



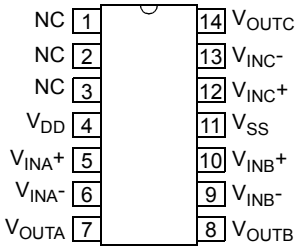
MCP662
3x3 DFN*



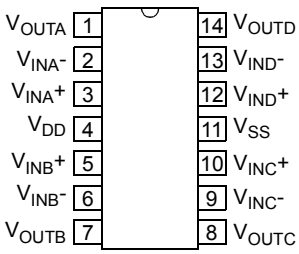
MCP665
3x3 DFN*



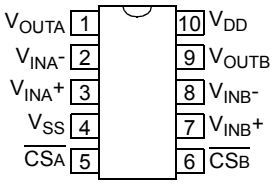
MCP660
SOIC, TSSOP



MCP664
SOIC, TSSOP



MCP665
MSOP



* Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† . V_{SS} – 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±150 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 1 kV, 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 kΩ to V_L and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Offset						
Input Offset Voltage	V_{OS}	-8	±1.8	+8	mV	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection Ratio	PSRR	61	76	—	dB	
Input Current and Impedance						
Input Bias Current	I_B	—	6	—	pA	
Across Temperature	I_B	—	130	—	pA	T_A = +85°C
Across Temperature	I_B	—	1700	5,000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±10	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||9	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Common Mode						
Common-Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.3	V	**(Note 1)**
Common-Mode Rejection Ratio	CMRR	64	79	—	dB	V_{DD} = 2.5V, V_{CM} = -0.3 to 1.2V
	CMRR	66	81	—	dB	V_{DD} = 5.5V, V_{CM} = -0.3 to 4.2V
Open Loop Gain						
DC Open Loop Gain (large signal)	A_{OL}	88	117	—	dB	V_{DD} = 2.5V, V_{OUT} = 0.3V to 2.2V
	A_{OL}	94	126	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.3V to 5.2V

Note 1: See Figure 2-5 for temperature effects.
2: The I_{SC} specifications are for design guidance only; they are not tested.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 2.5V, G = +2, 0.5V Input Overdrive
	V_{OL}, V_{OH}	V_{SS} + 50	—	V_{DD} – 50	mV	V_{DD} = 5.5V, G = +2, 0.5V Input Overdrive
Output Short Circuit Current	I_{SC}	±45	±90	±145	mA	V_{DD} = 2.5V **(Note 2)**
	I_{SC}	±40	±80	±150	mA	V_{DD} = 5.5V **(Note 2)**
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	3	6	9	mA	No Load Current

Note 1: See Figure 2-5 for temperature effects.

2: The I_{SC} specifications are for design guidance only; they are not tested.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	60	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1
Open Loop Output Impedance	R_{OUT}	—	10	—	Ω	
AC Distortion						
Total Harmonic Distortion plus Noise	THD+N	—	0.003	—	%	G = +1, V_{OUT} = 2V_{P-P}, f = 1 kHz, V_{DD} = 5.5V, BW = 80 kHz
Differential Gain, Positive Video **(Note 1)**	DG	—	0.3	—	%	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to 0.7V
Differential Gain, Negative Video **(Note 1)**	DG	—	0.3	—	%	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to -0.7V
Differential Phase, Positive Video **(Note 1)**	DP	—	0.3	—	°	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to 0.7V
Differential Phase, Negative Video **(Note 1)**	DP	—	0.9	—	°	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to -0.7V
Step Response						
Rise Time, 10% to 90%	t_r	—	5	—	ns	G = +1, V_{OUT} = 100 mV_{P-P}
Slew Rate	SR	—	32	—	V/µs	G = +1
Noise						
Input Noise Voltage	E_{ni}	—	14	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	6.8	—	nV/√Hz	f = 1 MHz
Input Noise Current Density	i_{ni}		4	—	fA/√Hz	f = 1 kHz

Note 1: These specifications are described in detail in **Section 4.3 "Distortion"**. (NTSC refers to a National Television Standards Committee signal.)

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS} (refer to Figure 1-1 and Figure 1-2).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	-0.1	—	nA	$\overline{CS}$ = 0V
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.8V_{DD}$		V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	-0.7	—	µA	$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	-2	-1	—	µA	
$\overline{CS}$ Internal Pull Down Resistor	R_{PD}	—	5	—	MΩ	
Amplifier Output Leakage	$I_{O(LEAK)}$	—	40	—	nA	$\overline{CS}$ = V_{DD}, T_A = +125°C
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Input Hysteresis	V_{HYST}	—	0.25	—	V	
$\overline{CS}$ High to Amplifier Off Time (output goes High-Z)	t_{OFF}	—	200	—	ns	G = +1 V/V, V_L = V_{SS} $\overline{CS}$ = $0.8V_{DD}$ to V_{OUT} = $0.1(V_{DD}/2)$
$\overline{CS}$ Low to Amplifier On Time	t_{ON}	—	2	10	µs	G = +1 V/V, V_L = V_{SS}, $\overline{CS}$ = $0.2V_{DD}$ to V_{OUT} = $0.9(V_{DD}/2)$

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless indicated, all limits are specified for: V_{DD} = +2.5V to +5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-3x3 DFN	θ_{JA}	—	56.7	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 10L-3x3 DFN	θ_{JA}	—	53.3	—	°C/W	**(Note 2)**
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-QFN	θ_{JA}	—	45.7	—	°C/W	

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (+150°C).

2: Measured on a standard JC51-7, four layer printed circuit board with ground plane and vias.

1.3 Timing Diagram

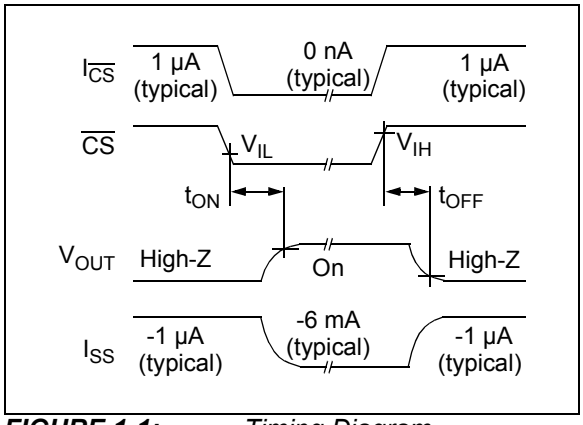


FIGURE 1-1: *Timing Diagram.*

1.4 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-2. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

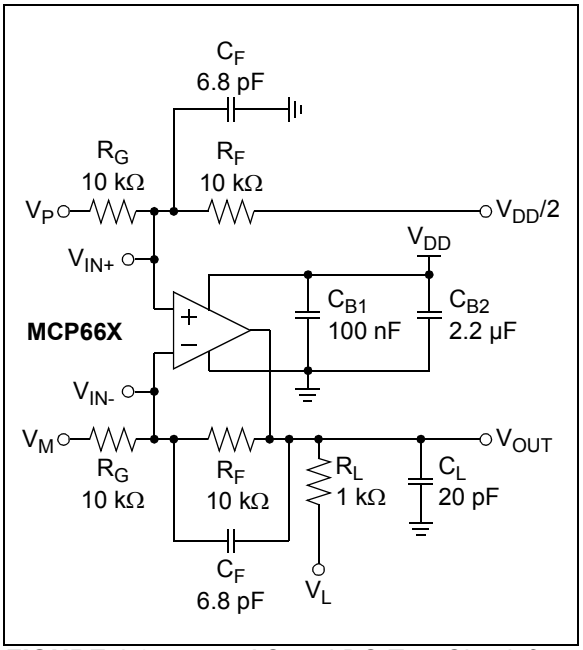


FIGURE 1-2: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.1 DC Signal Inputs

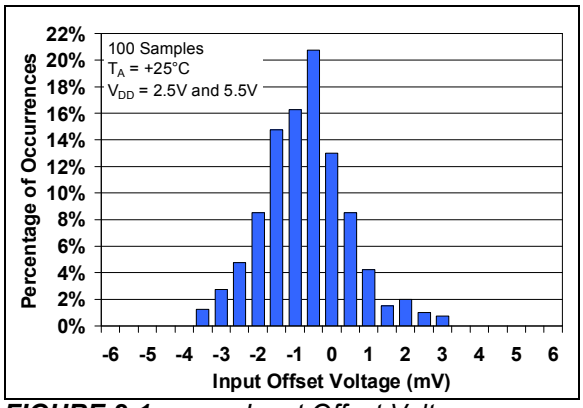


FIGURE 2-1: *Input Offset Voltage.*

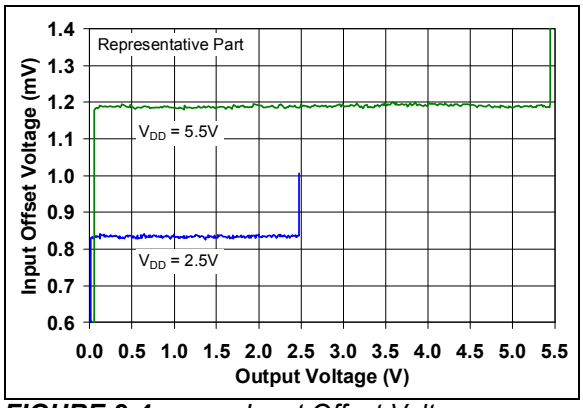


FIGURE 2-4: *Input Offset Voltage vs. Output Voltage.*

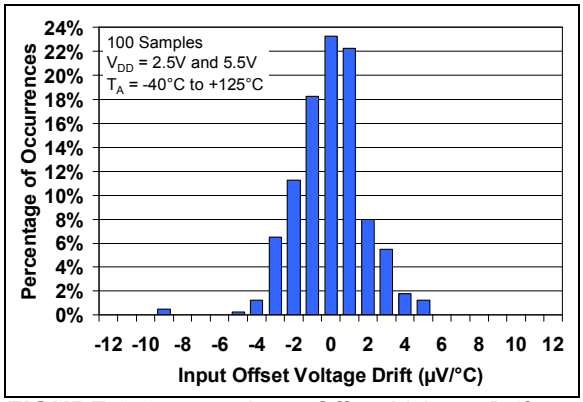


FIGURE 2-2: *Input Offset Voltage Drift.*

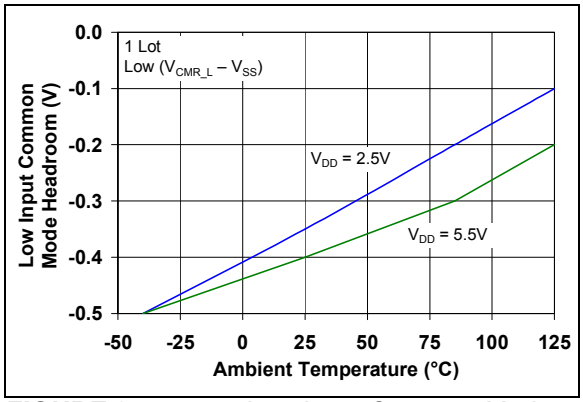


FIGURE 2-5: *Low Input Common Mode Voltage Headroom vs. Ambient Temperature.*

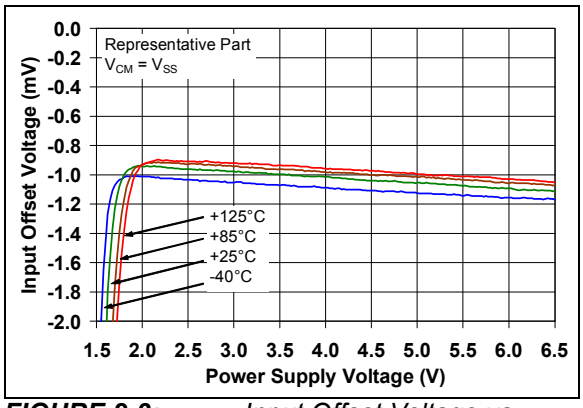


FIGURE 2-3: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = 0V.*

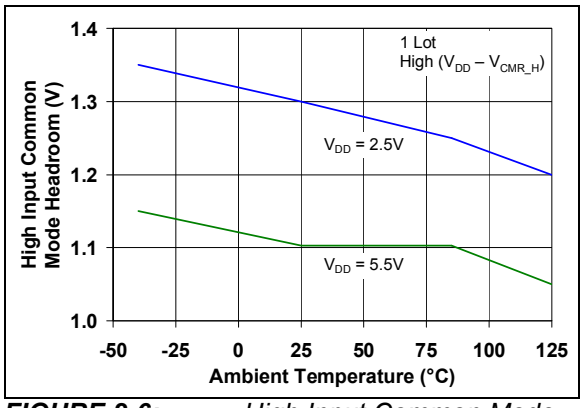


FIGURE 2-6: *High Input Common Mode Voltage Headroom vs. Ambient Temperature.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

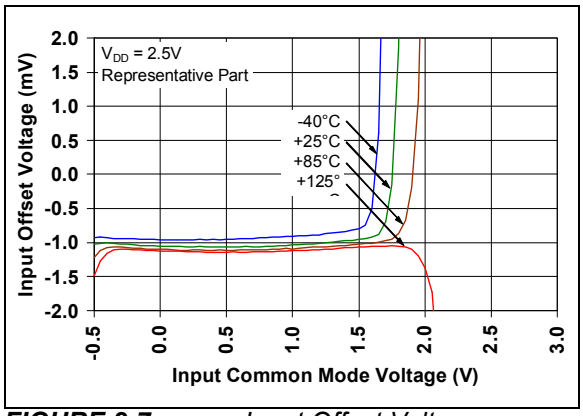


FIGURE 2-7: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 2.5V.*

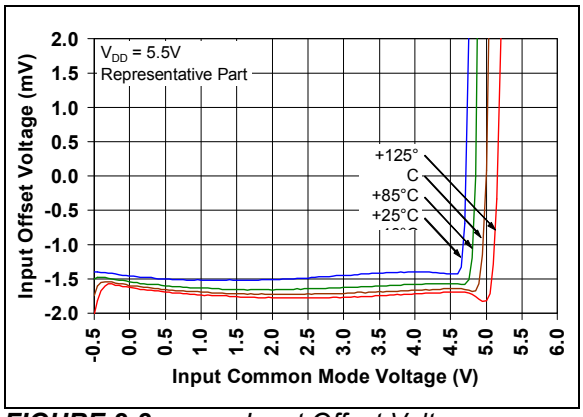


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 5.5V.*

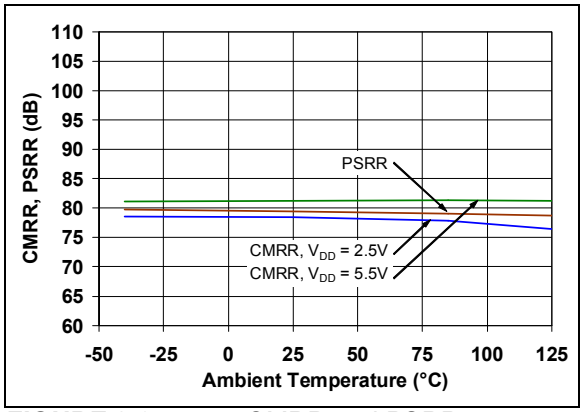


FIGURE 2-9: *CMRR and PSRR vs. Ambient Temperature.*

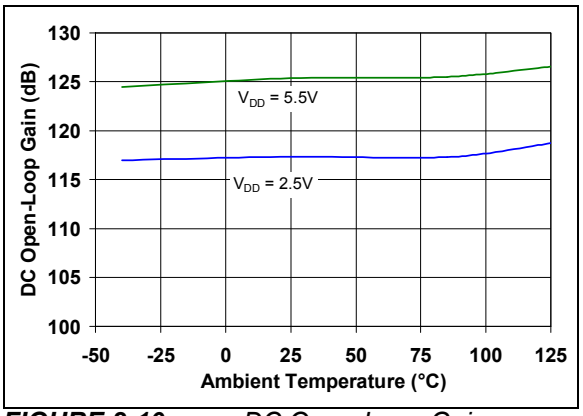


FIGURE 2-10: *DC Open-Loop Gain vs. Ambient Temperature.*

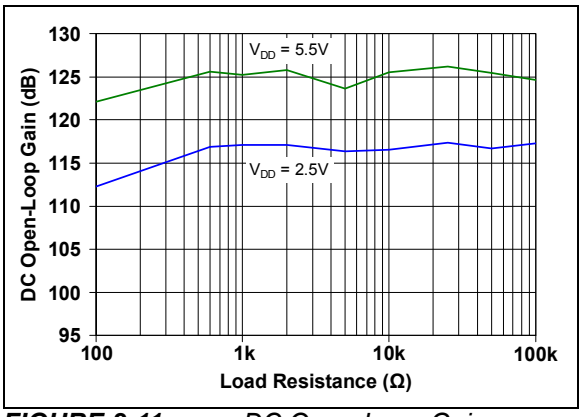


FIGURE 2-11: *DC Open-Loop Gain vs. Load Resistance.*

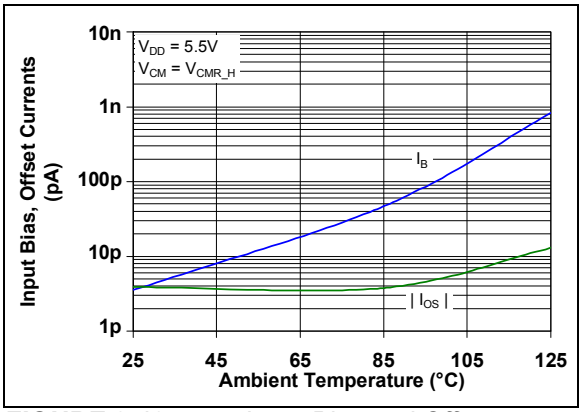


FIGURE 2-12: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = +5.5V.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

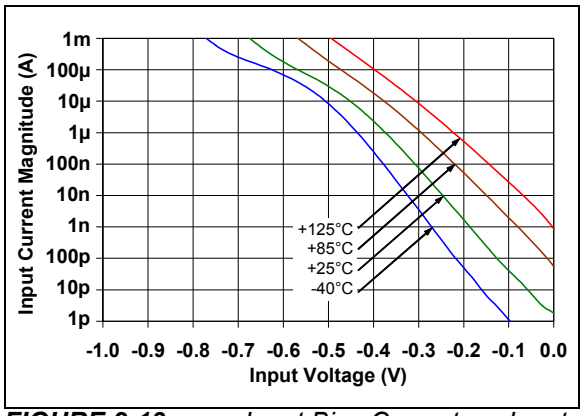


FIGURE 2-13: *Input Bias Current vs. Input Voltage (below V_{SS}).*

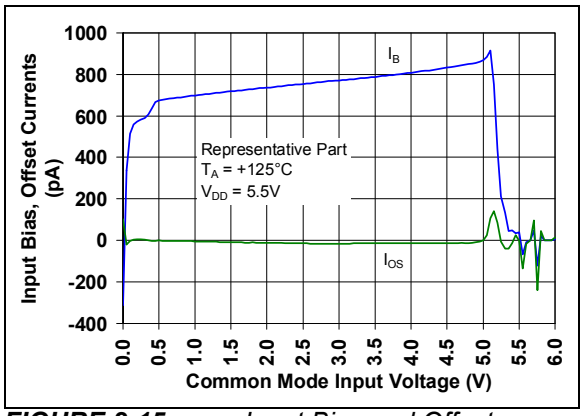


FIGURE 2-15: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

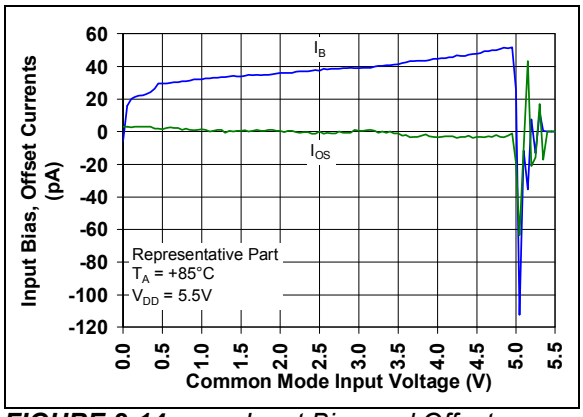


FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.2 Other DC Voltages and Currents

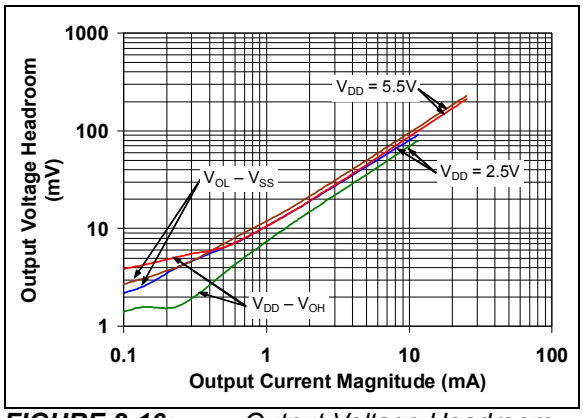


FIGURE 2-16: *Output Voltage Headroom vs. Output Current.*

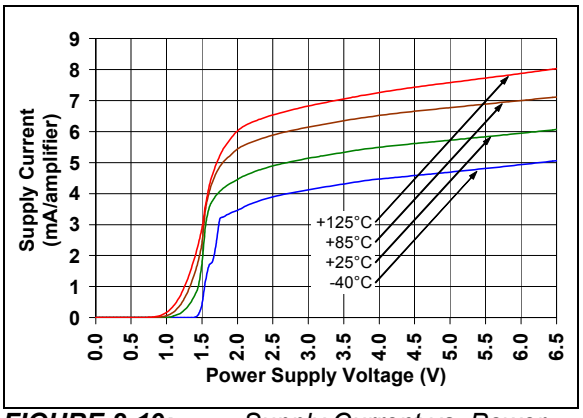


FIGURE 2-19: *Supply Current vs. Power Supply Voltage.*

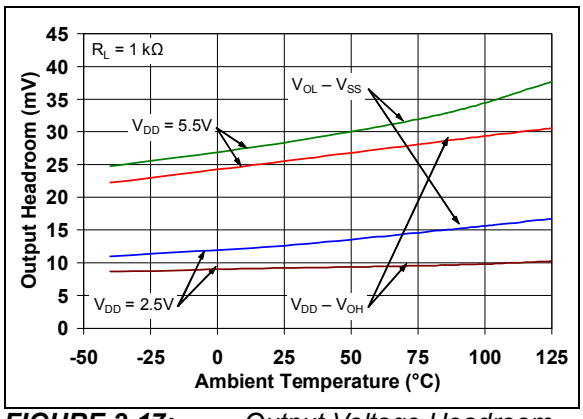


FIGURE 2-17: *Output Voltage Headroom vs. Ambient Temperature.*

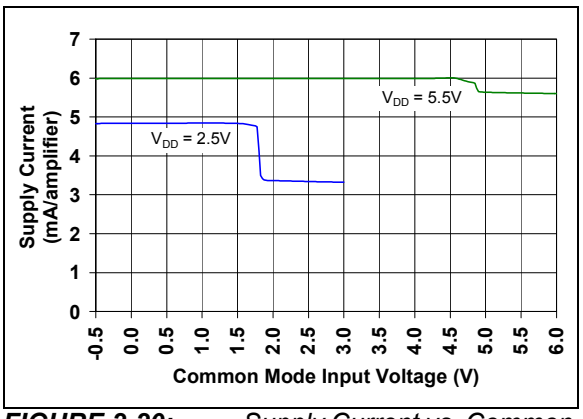


FIGURE 2-20: *Supply Current vs. Common Mode Input Voltage.*

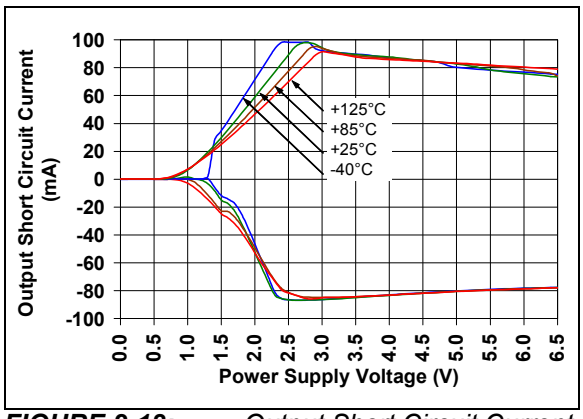


FIGURE 2-18: *Output Short Circuit Current vs. Power Supply Voltage.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.3 Frequency Response

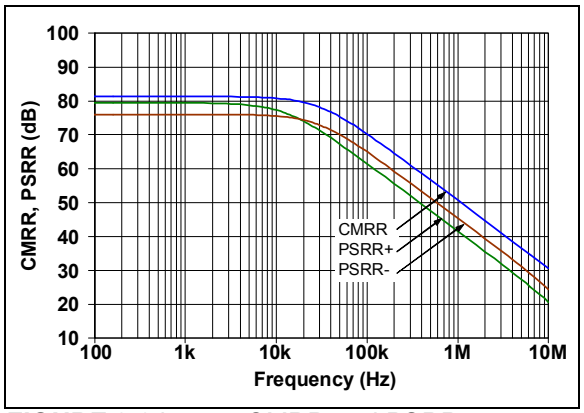


FIGURE 2-21: *CMRR and PSRR vs. Frequency.*

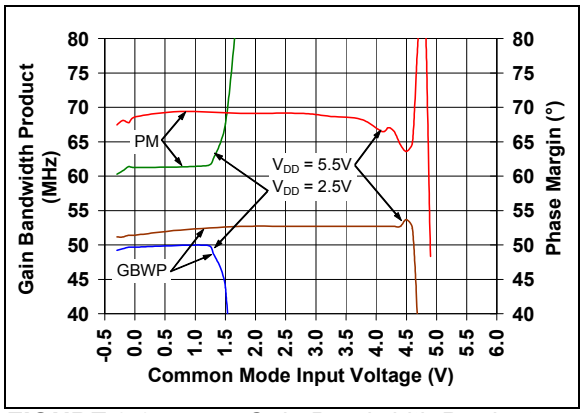


FIGURE 2-24: *Gain Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.*

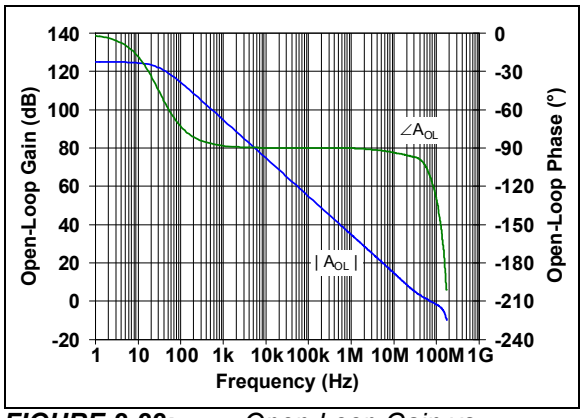


FIGURE 2-22: *Open-Loop Gain vs. Frequency.*

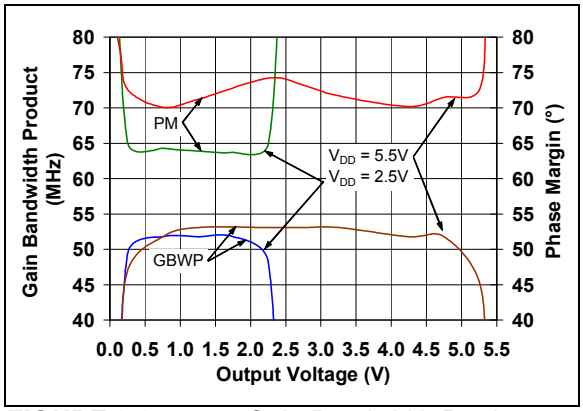


FIGURE 2-25: *Gain Bandwidth Product and Phase Margin vs. Output Voltage.*

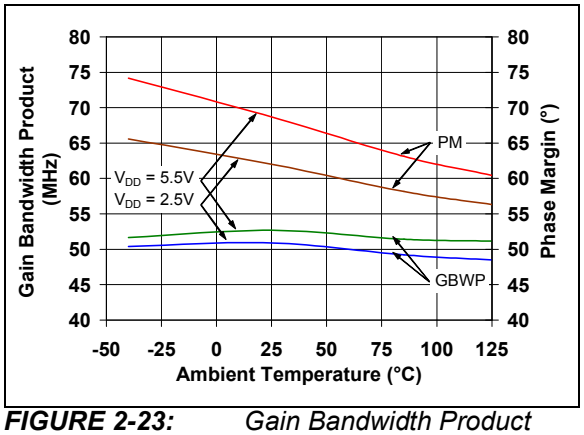


FIGURE 2-23: *Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

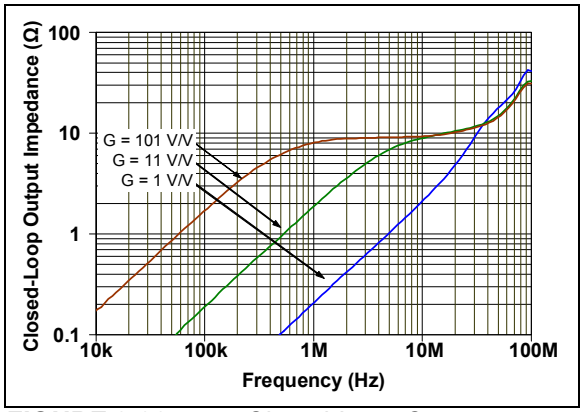


FIGURE 2-26: *Closed-Loop Output Impedance vs. Frequency.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

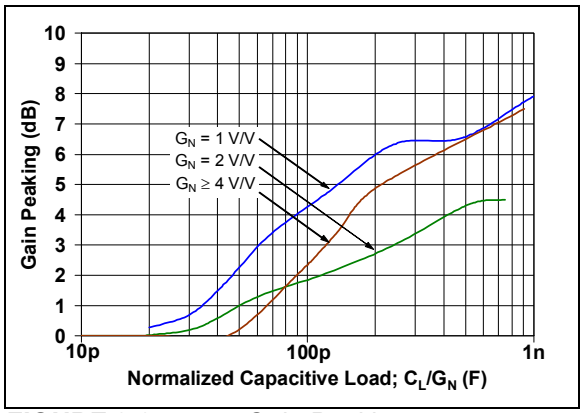


FIGURE 2-27: *Gain Peaking vs. Normalized Capacitive Load.*

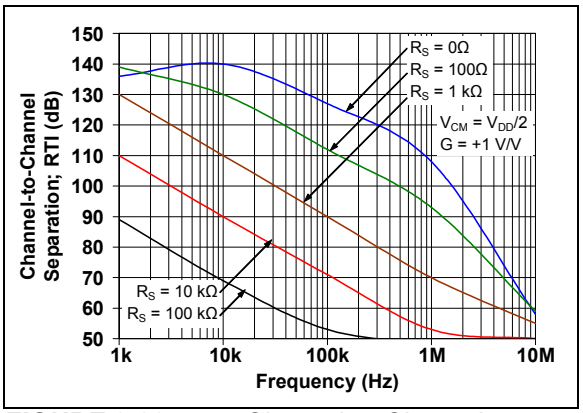


FIGURE 2-28: *Channel-to-Channel Separation vs. Frequency.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.4 Noise and Distortion

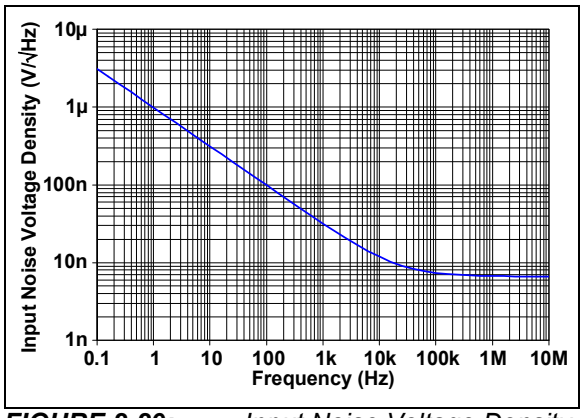


FIGURE 2-29: *Input Noise Voltage Density vs. Frequency.*

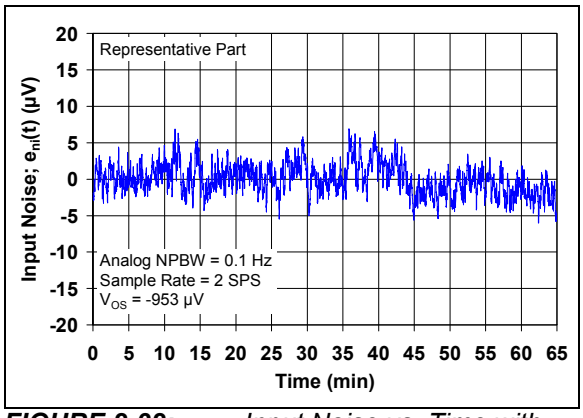


FIGURE 2-32: *Input Noise vs. Time with 0.1 Hz Filter.*

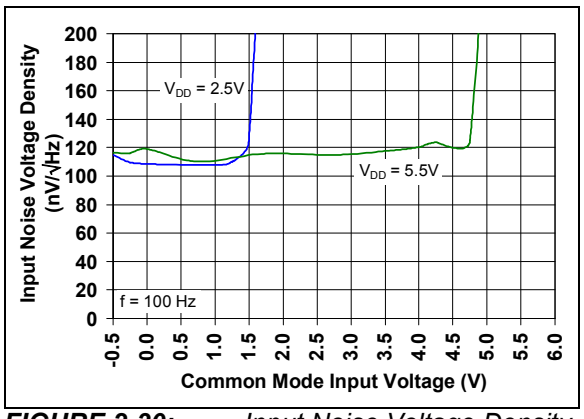


FIGURE 2-30: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 100 Hz.*

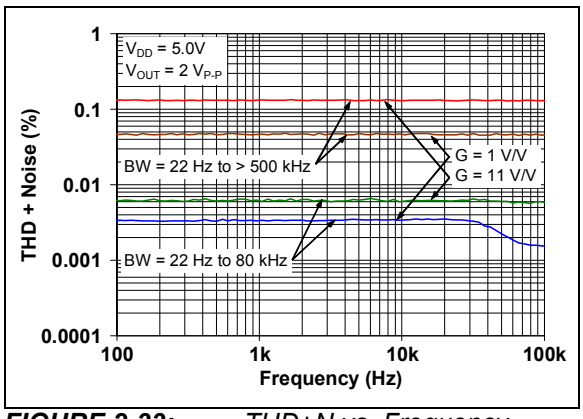


FIGURE 2-33: *THD+N vs. Frequency.*

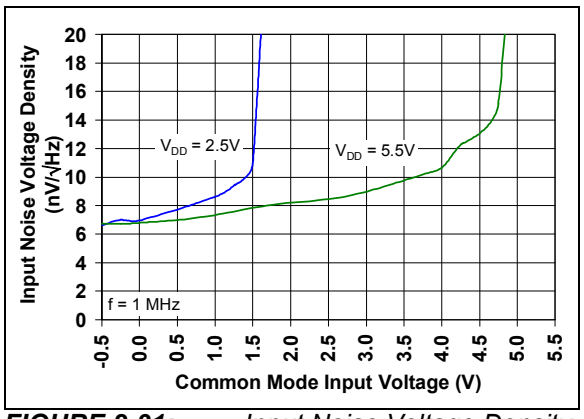


FIGURE 2-31: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 1 MHz.*

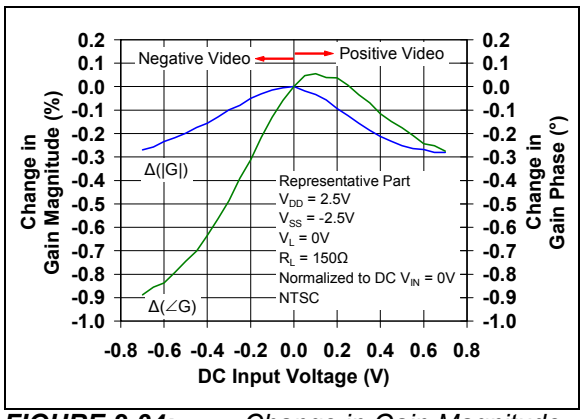


FIGURE 2-34: *Change in Gain Magnitude and Phase vs. DC Input Voltage.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.5 Time Response

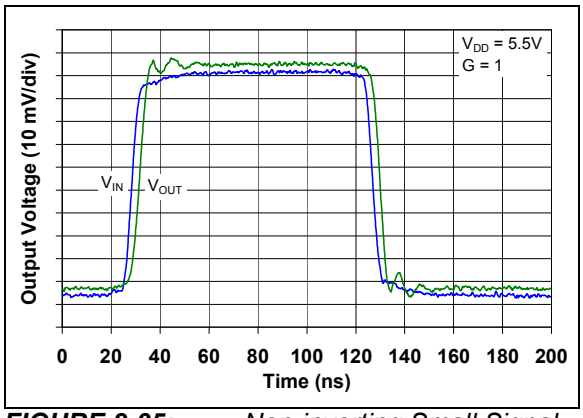


FIGURE 2-35: *Non-inverting Small Signal Step Response.*

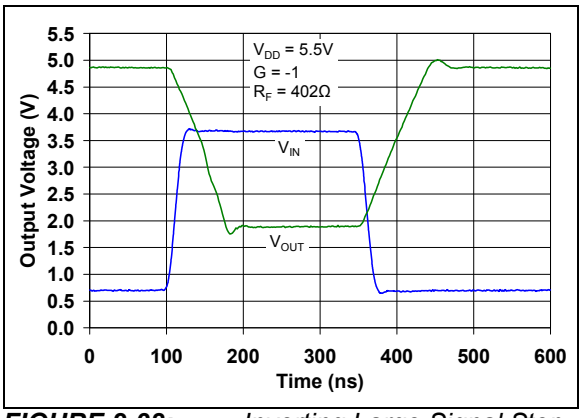


FIGURE 2-38: *Inverting Large Signal Step Response.*

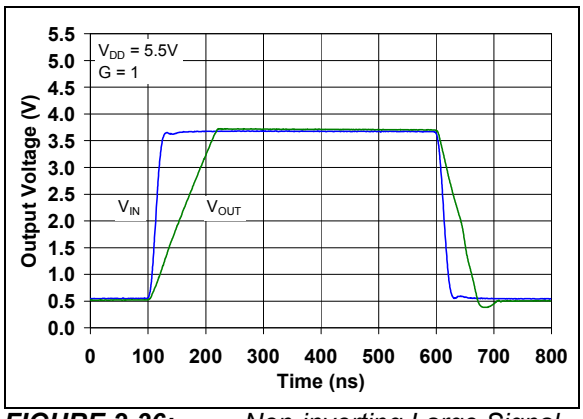


FIGURE 2-36: *Non-inverting Large Signal Step Response.*

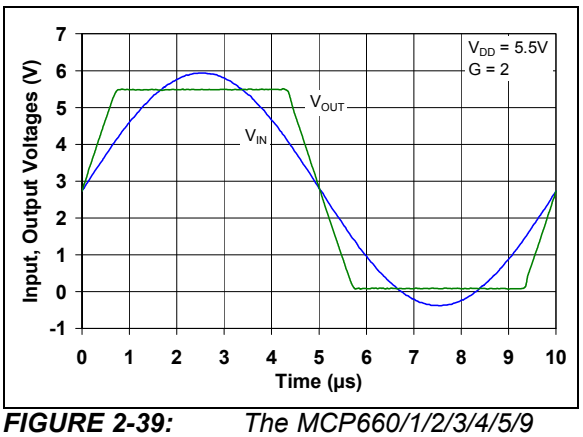


FIGURE 2-39: *The MCP660/1/2/3/4/5/9 family shows no input phase reversal with overdrive.*

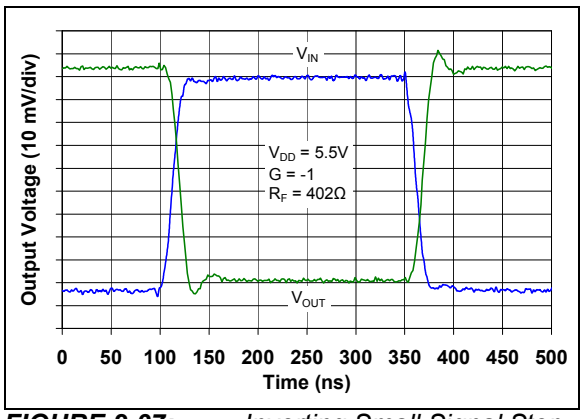


FIGURE 2-37: *Inverting Small Signal Step Response.*

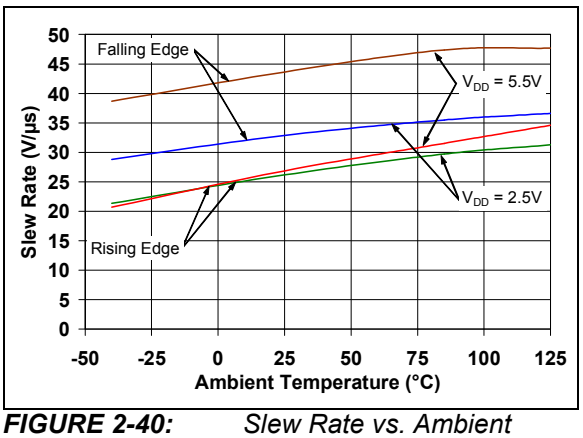


FIGURE 2-40: *Slew Rate vs. Ambient Temperature.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

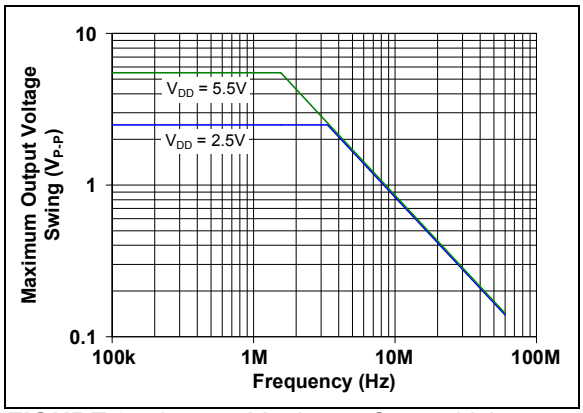


FIGURE 2-41: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.6 Chip Select Response

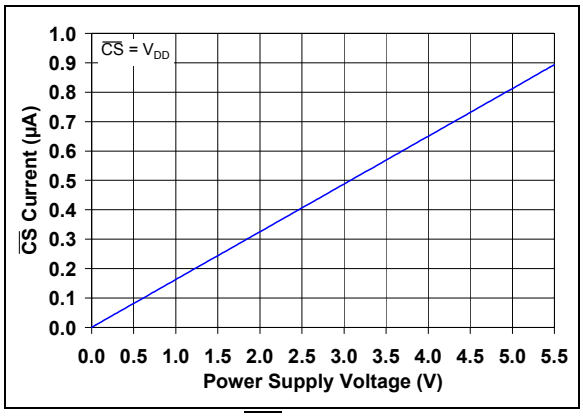


FIGURE 2-42: *$\overline{CS}$ Current vs. Power Supply Voltage.*

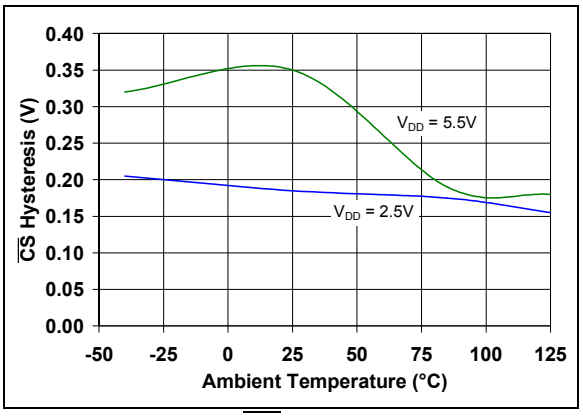


FIGURE 2-45: *$\overline{CS}$ Hysteresis vs. Ambient Temperature.*

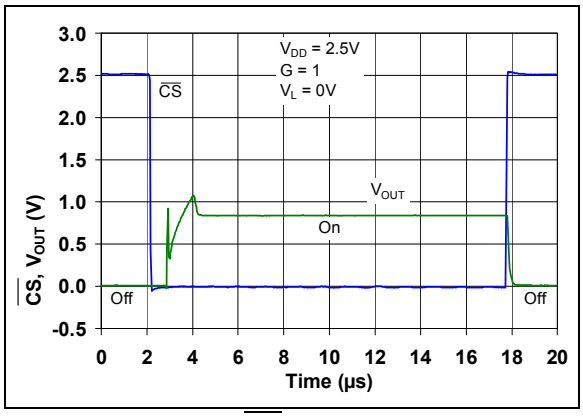


FIGURE 2-43: *$\overline{CS}$ and Output Voltages vs. Time with V_{DD} = 2.5V.*

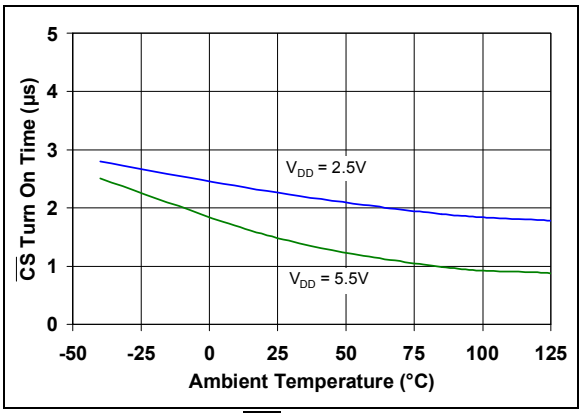


FIGURE 2-46: *$\overline{CS}$ Turn On Time vs. Ambient Temperature.*

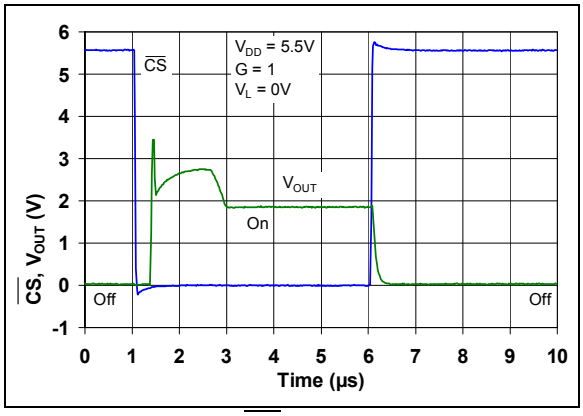


FIGURE 2-44: *$\overline{CS}$ and Output Voltages vs. Time with V_{DD} = 5.5V.*

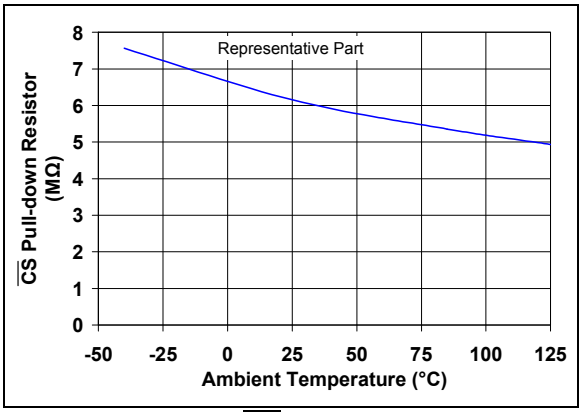


FIGURE 2-47: *$\overline{CS}$'s Pull-down Resistor (R_{PD}) vs. Ambient Temperature.*

Note: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

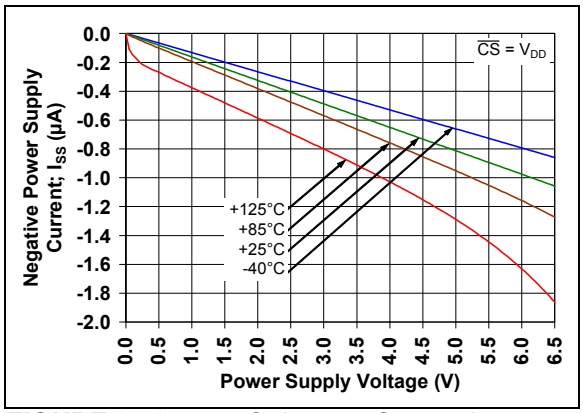


FIGURE 2-48: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

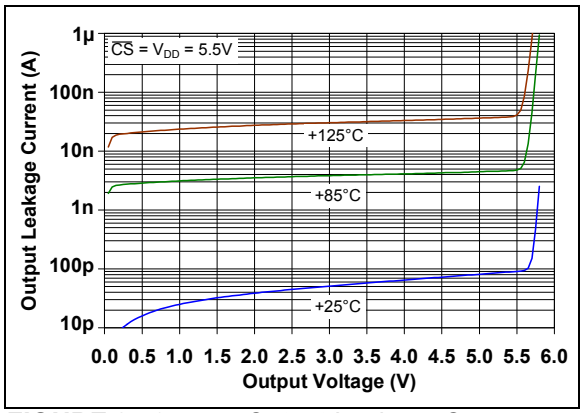


FIGURE 2-49: *Output Leakage Current vs. Output Voltage.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP660		MCP661	MCP662		MCP663	MCP664	MCP665		MCP669	Symbol	Description
4x4 QFN	SOIC, TSSOP	SOIC	SOIC	DFN	SOIC	SOIC, TSSOP	MSOP	DFN	4x4 QFN		
5	6	2	2	2	2	2	2	2	1	V_{IN}-, V_{INA}-	Inverting Input (op amp A)
4	5	3	3	3	3	3	3	3	2	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
3	4	7	8	8	7	4	10	10	3	V_{DD}	Positive Power Supply
10	10	—	5	5	—	5	7	7	4	V_{INB}+	Non-inverting Input (op amp B)
9	9	—	6	6	—	6	8	8	5	V_{INB}-	Inverting Input (op amp B)
8	8	—	7	7	—	7	9	9	6	V_{OUTB}	Output (op amp B)
—	—	—	—	—	—	—	—	—	7	$\overline{CS}_{BC}$	Chip Select Digital Input (op amps B and C)
14	14	—	—	—	—	8	—	—	8	V_{OUTC}	Output (op amp C)
13	13	—	—	—	—	9	—	—	9	V_{INC}-	Inverting Input (op amp C)
12	12	—	—	—	—	10	—	—	10	V_{INC}+	Non-inverting Input (op amp C)
11	11	4	4	4	4	11	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	—	12	—	—	12	V_{IND}+	Inverting Input (op amp D)
—	—	—	—	—	—	13	—	—	13	V_{IND}-	Inverting Input (op amp D)
—	—	—	—	—	—	14	—	—	14	V_{OUTD}	Output (op amp D)
—	—	—	—	—	—	—	—	—	15	$\overline{CS}_{AD}$	Chip Select Digital Input (op amps A and D)
6	7	6	1	1	6	1	1	1	16	V_{OUT}, V_{OUTA}	Output (op amp A)
17		—	—	9	—	—	—	11	17	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}
—	—	—	—	—	8	—	5	5	—	$\overline{CS}$, $\overline{CS}_A$	Chip Select Digital Input (op amp A)
—	—	—	—	—	—	—	6	6	—	$\overline{CS}_B$	Chip Select Digital Input (op amp B)
1, 2, 7, 15, 16	1, 2, 3	1, 5, 8	—	—	1, 5	—	—	—	—	NC	No Internal Connection

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs ($V_{IN}+$, $V_{IN}-$, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.5V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In that case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Chip Select Digital Input ($\overline{CS}$)

The input ($\overline{CS}$) is a CMOS, Schmitt-triggered input that places the part into a Low Power mode of operation.

3.5 Exposed Thermal Pad (EP)

There is an internal connection between the exposed thermal pad (EP) and the V_{SS} pin; they must be connected to the same potential on the printed circuit board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP660/1/2/3/4/5/9 family is manufactured using the Microchip state of the art CMOS process. It is designed for low cost, low power and high speed applications. Its low supply voltage, low quiescent current and wide bandwidth make the MCP660/1/2/3/4/5/9 ideal for battery-powered applications.

4.1 Input

4.1.1 PHASE REVERSAL

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-39 shows an input voltage exceeding both supplies with no phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The electrostatic discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

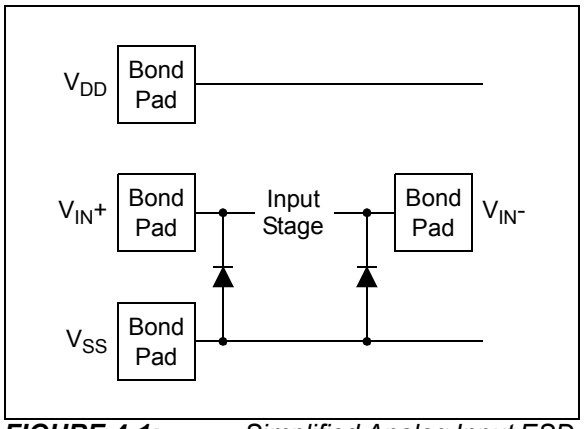


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). Figure 4-2 shows the recommended approach to protecting these inputs.

The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above V_{DD}, and dump any currents onto V_{DD}.

When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

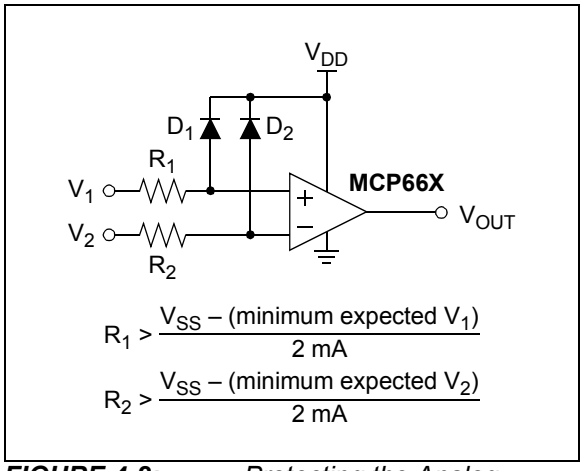


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-13. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP660/1/2/3/4/5/9 op amps uses a differential PMOS input stage. It operates at low common mode input voltages (V_{CM}), with V_{CM} between V_{SS} – 0.3V and V_{DD} – 1.3V. To ensure proper operation, the input offset voltage (V_{OS}) is measured at both V_{CM} = V_{SS} – 0.3V and V_{DD} – 1.3V. See Figure 2-5 and Figure 2-6 for temperature effects.

When operating at very low non-inverting gains, the output voltage is limited at the top by the V_{CM} range (<V_{DD} – 1.3V); see Figure 4-3.

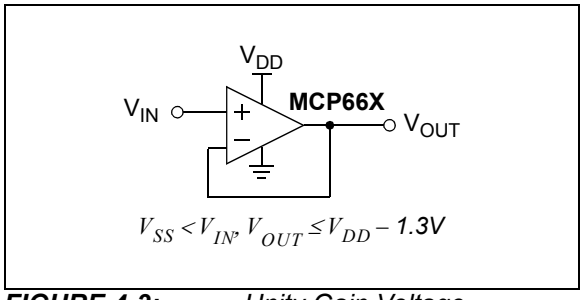


FIGURE 4-3: *Unity Gain Voltage Limitations for Linear Operation.*

4.2 Rail-to-Rail Output

4.2.1 MAXIMUM OUTPUT VOLTAGE

The Maximum Output Voltage (see Figure 2-16 and Figure 2-17) describes the output range for a given load. For example, the output voltage swings to within 50 mV of the negative rail with a 1 kΩ load tied to $V_{DD}/2$.

4.2.2 OUTPUT CURRENT

Figure 4-4 shows the possible combinations of output voltage (V_{OUT}) and output current (I_{OUT}), when V_{DD} = 5.5V.

I_{OUT} is positive when it flows out of the op amp into the external circuit.

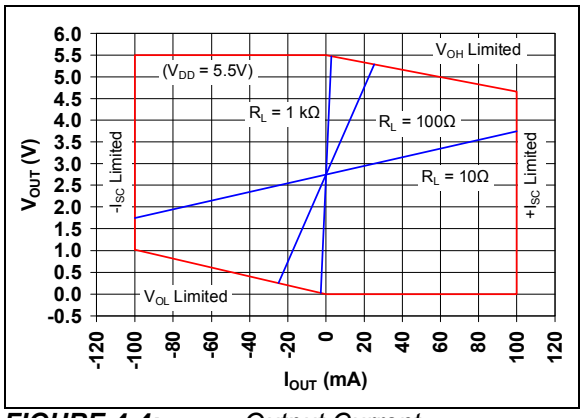


FIGURE 4-4: *Output Current.*

4.2.3 POWER DISSIPATION

Since the output short circuit current (I_{SC}) is specified at ±90 mA (typical), these op amps are capable of both delivering and dissipating significant power.

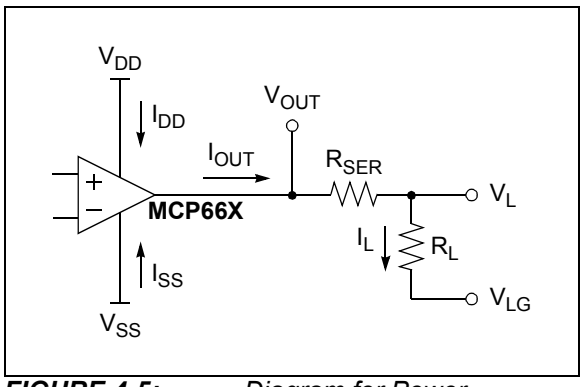


FIGURE 4-5: *Diagram for Power Calculations.*

Figure 4-5 shows the entities used in the following power calculations for a single op amp.

- R_{SER} is 0Ω in most applications and can be used to limit I_{OUT}.
- V_{OUT} is the op amp's output voltage.
- V_L is the voltage at the load.
- V_{LG} is the load's ground point.
- V_{SS} is usually ground (0V).

The input currents are assumed to be negligible. The currents shown in Figure 4-5 can be approximated using Equation 4-1:

EQUATION 4-1:

$$I_{OUT} = I_L = \frac{V_{OUT} - V_{LG}}{R_{SER} + R_L}$$
$$I_{DD} \approx I_Q + max(0, I_{OUT})$$
$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = quiescent supply current

The instantaneous op amp power ($P_{OA}(t)$), R_{SER} power ($P_{RSER}(t)$) and load power ($P_L(t)$) are calculated in Equation 4-2:

EQUATION 4-2:

$$P_{OA}(t) = I_{DD}\,(V_{DD} - V_{OUT}) + I_{SS}\,(V_{SS} - V_{OUT})$$
$$P_{RSER}(t) = I_{OUT}{}^2 R_{SER}$$
$$P_L(t) = I_L{}^2 R_L$$

The maximum op amp power, for resistive loads, occurs when V_{OUT} is halfway between V_{DD} and V_{LG} or halfway between V_{SS} and V_{LG}.

EQUATION 4-3:

$$P_{OAmax} \leq \frac{max^2(V_{DD} - V_{LG}, - V_{SS})}{4(R_{SER} + R_L)}$$

The maximum ambient to junction temperature rise (ΔT_{JA}) and junction temperature (T_J) can be calculated using P_{OAmax}, ambient temperature (T_A), the package thermal resistance (θ_{JA} – found in Table 1-4), and the number of op amps in the package (assuming equal power dissipations), as shown in Equation 4-4:

EQUATION 4-4:

$$\Delta T_{JA} = P_{OA}(t)\ \theta_{JA} \leq n\ P_{OAmax}\theta_{JA}$$
$$T_J = T_A + \Delta T_{JA}$$

Where:

n = number of op amps in package (1, 2)

The power de-rating across temperature for an op amp in a particular package can be easily calculated (assuming equal power dissipations):

EQUATION 4-5:

$$P_{OAmax} \leq \frac{T_{Jmax} - T_A}{n\ \theta_{JA}}$$

Where:

T_{Jmax} = absolute max. junction temperature

Several techniques are available to reduce ΔT_{JA} for a given P_{OAmax}:

- Lower θ_{JA}
  - Use another package
  - PCB layout (ground plane, etc.)
  - Heat sinks and air flow
- Reduce P_{OAmax}
  - Increase R_L
  - Limit I_{OUT} (using R_{SER})
  - Decrease V_{DD}

4.3 Distortion

Differential gain (DG) and differential phase (DP) refer to the non-linear distortion produced by a NTSC or a phase-alternating line (PAL) video component. Table 1-2 and Figure 2-34 show the typical performance of the MCP661, configured as a gain of +2 amplifier (see Figure 4-10), when driving one back-matched video load (150Ω, for 75Ω cable). Microchip tests use a sine wave at NTSC's color sub-carrier frequency of 3.58 MHz, with a $0.286V_{P-P}$ magnitude. The DC input voltage is changed over a +0.7V range (positive video) or a -0.7V range (negative video).

DG is the peak-to-peak change in the AC gain magnitude (color hue), as the DC level (luminance) is changed, in percentile units (%). DP is the peak-to-peak change in the AC gain phase (color saturation), as the DC level (luminance) is changed, in degree (°) units.

4.4 Improving Stability

4.4.1 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the phase margin (stability) of the feedback loop decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., >20 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-6) improves the phase margin of the feedback loop by making the output load resistive at higher frequencies. The bandwidth generally will be lower than bandwidth without the capacitive load.

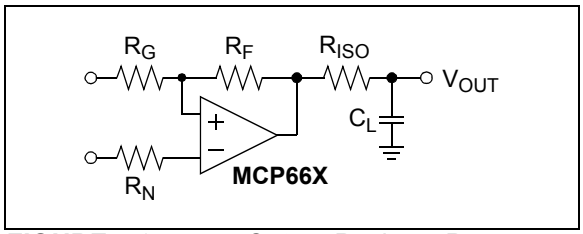


FIGURE 4-6: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-7 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

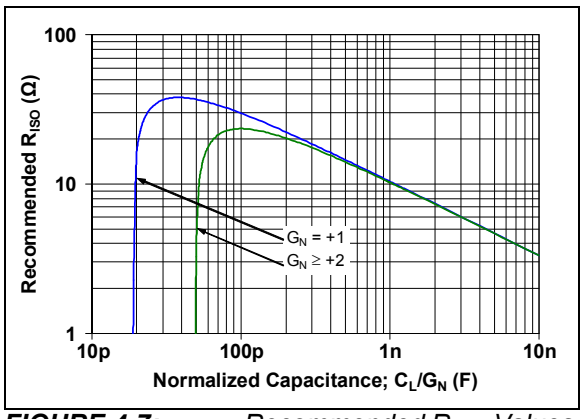


FIGURE 4-7: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for the circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP660/1/2/3/4/5/9 SPICE macro model are helpful.

4.4.2 GAIN PEAKING

Figure 4-8 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel.

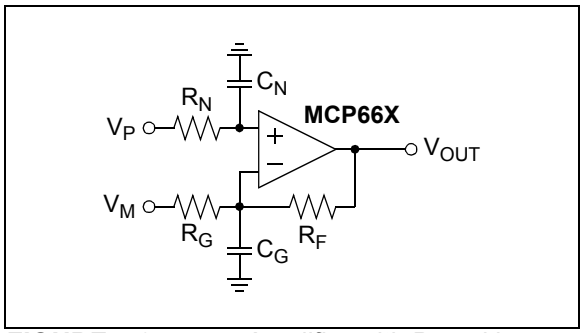


FIGURE 4-8: *Amplifier with Parasitic Capacitance.*

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or R_F.

C_N and R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at $1/(2\pi R_N C_N)$.

The largest value of R_F that should be used depends on noise gain (see G_N in **Section 4.4.1 "Capacitive Loads"**), C_G and the open-loop gain's phase shift. Figure 4-9 shows the maximum recommended R_F for several C_G values. Some applications may modify these values to reduce either output loading or gain peaking (step response overshoot).

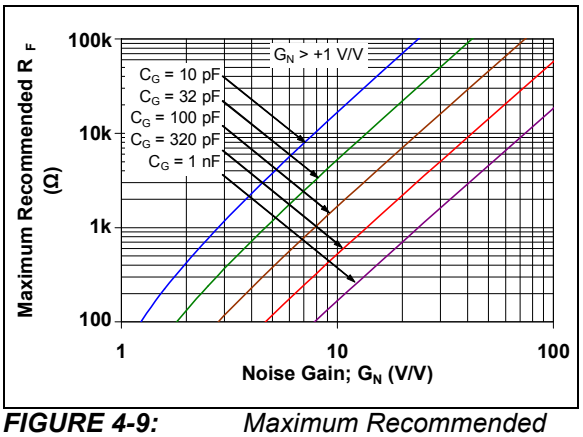


FIGURE 4-9: *Maximum Recommended R_F vs. Gain.*

Figure 2-35 and Figure 2-36 show the small signal and large signal step responses at G = +1 V/V. The unity gain buffer usually has $R_F = 0\Omega$ and R_G open.

Figure 2-37 and Figure 2-38 show the small signal and large signal step responses at G = -1 V/V. Since the noise gain is 2 V/V and $C_G \approx 10$ pF, the resistors were chosen to be $R_F = R_G = 401\Omega$ and $R_N = 200\Omega$.

It is also possible to add a capacitor (C_F) in parallel with R_F to compensate for the de-stabilizing effect of C_G. This makes it possible to use larger values of R_F. The conditions for stability are summarized in Equation 4-6.

EQUATION 4-6:

Given:

$$G_{N1} = 1 + R_F/R_G$$
$$G_{N2} = 1 + C_G/C_F$$
$$f_F = 1/(2\pi R_F C_F)$$
$$f_Z = f_F(G_{N1}/G_{N2})$$

We need:

$$f_F \leq f_{GBWP}/(2G_{N2}), \quad G_{N1} < G_{N2}$$
$$f_F \leq f_{GBWP}/(4G_{N1}), \quad G_{N1} > G_{N2}$$

4.5 MCP663 and MCP665 Chip Select

The MCP663 is a single amplifier with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 1 µA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pulldown resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pin is left floating. Figure 1-1, Figure 2-43 and Figure 2-44 show the output voltage and supply current response to a $\overline{CS}$ pulse.

The MCP665 is a dual amplifier with two $\overline{CS}$ pins; $\overline{CS_A}$ controls op amp A, and $\overline{CS_B}$ controls op amp B. These op amps are controlled independently, with an enabled quiescent current (I_Q) of 6 mA/amplifier (typical) and a disabled I_Q of 1 µA/amplifier (typical). The I_Q seen at the supply pins is the sum of the two op amps' I_Q; the typical value for the I_Q of the MCP665 will be 2 µA, 6 mA or 12 mA when there are 0, 1 or 2 amplifiers enabled, respectively.

4.6 Power Supply

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These op amps require a bulk capacitor (i.e., 2.2 µF or larger) within 50 mm to provide large, slow currents. Tantalum capacitors, or their equivalent, may be a good choice. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the supplies does not prove to be a problem.

4.7 High Speed PCB Layout

These op amps are fast enough that a little extra care in the printed circuit board (PCB) layout can make a significant difference in performance. Good PC board layout techniques will help you achieve the performance shown in the specifications and typical performance curves; it will also help to minimize electro-magnetic compatibility (EMC) issues.

Use a solid ground plane. Connect the bypass local capacitor(s) to this plane with minimal length traces. This cuts down inductive and capacitive crosstalk.

Separate digital from analog, low speed from high speed, and low power from high power. This will reduce interference.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

Sometimes, it helps to place guard traces next to victim traces. They should be on both sides of the victim trace, and as close as possible. Connect guard traces to ground plane at both ends, and in the middle for long traces.

Use coax cables, or low inductance wiring, to route signal and power to and from the PCB. Mutual and self inductance of power wires is often a cause of crosstalk and unusual behavior.

4.8 Typical Applications

4.8.1 50Ω LINE DRIVER

Figure 4-10 shows the MCP661 driving a 50Ω line. The large output current (e.g., see Figure 2-18) makes it possible to drive a back-matched line (R_{M2}, the 50Ω line and the 50Ω load at the far end) to more than ±2V (the load at the far end sees ±1V). It is worth mentioning that the 50Ω line and the 50Ω load at the far end together can be modeled as a simple 50Ω resistor to ground.

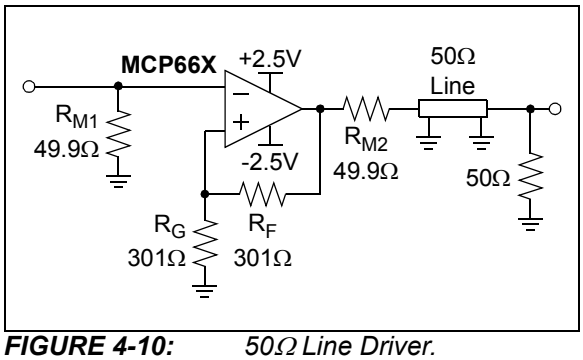


FIGURE 4-10: *50Ω Line Driver.*

The output headroom limits would be V_{OL} = -2.3V and V_{OH} = +2.3V (see Figure 2-16), leaving some design room for the ±2V signal. The open-loop gain (A_{OL}) typically does not decrease significantly with a 100Ω load (see Figure 2-11). The maximum power dissipated is about 48 mW (see **Section 4.2.3 "Power Dissipation"**), so the temperature rise (for the MCP661 in the SOIC-8 package) is under 8°C.

4.8.2 OPTICAL DETECTOR AMPLIFIER

Figure 4-11 shows a transimpedance amplifier, using the MCP661 op amp, in a photo detector circuit. The photo detector is a capacitive current source. R_F provides enough gain to produce 10 mV at V_{OUT}. C_F stabilizes the gain and limits the transimpedance bandwidth to about 1.1 MHz. The parasitic capacitance of R_F (e.g., 0.2 pF for a 0805 SMD) acts in parallel with C_F.

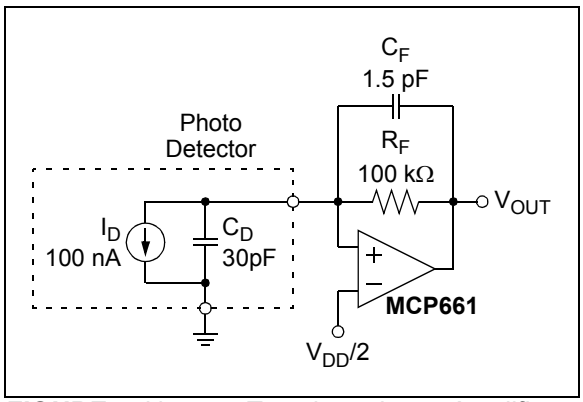


FIGURE 4-11: *Transimpedance Amplifier for an Optical Detector.*

4.8.3 H-BRIDGE DRIVER

Figure 4-12 shows the MCP662 dual op amp used as a H-bridge driver. The load could be a speaker or a DC motor.

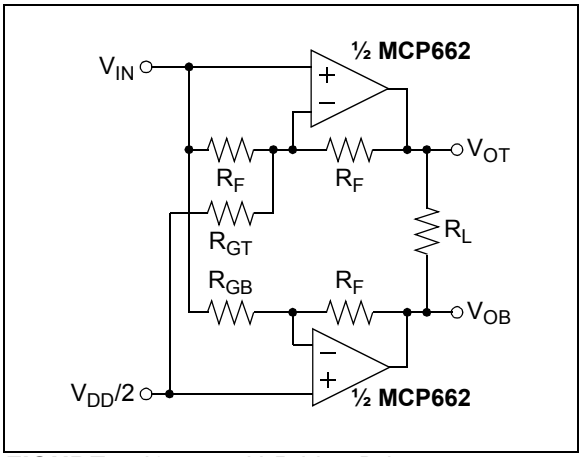


FIGURE 4-12: *H-Bridge Driver.*

This circuit automatically makes the noise gains (G_N) equal, when the gains are set properly, so that the frequency responses match well (in magnitude and in phase). Equation 4-7 shows how to calculate R_{GT} and R_{GB} so that both op amps have the same DC gains; G_{DM} needs to be selected first.

EQUATION 4-7:

$$G_{DM} \equiv \frac{V_{OT} - V_{OB}}{V_{IN} - V_{DD}/2} \geq 1\ V/V$$

$$R_{GT} = \frac{R_F}{(G_{DM}/2) - 1}$$

$$R_{GB} = \frac{R_F}{G_{DM}/2}$$

Equation 4-8 gives the resulting common mode and differential mode output voltages.

EQUATION 4-8:

$$\frac{V_{OT} + V_{OB}}{2} = \frac{V_{DD}}{2}$$

$$V_{OT} - V_{OB} = G_{DM}\left(V_{IN} - \frac{V_{DD}}{2}\right)$$

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP660/1/2/3/4/5/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP660/1/2/3/4/5/9 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the linear region of operation over the temperature range of the op amp. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the Filter-Lab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a filter can be defined to sort features for a parametric search of device, and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of analog demonstration and evaluation boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- MCP661 Line Driver Demo Board

5.5 Design and Application Notes

The following Microchip Analog Design Note and Application Notes are recommended as supplemental reference resources. They are available on the Microchip web site at www.microchip.com/appnotes.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1228:** *"Op Amp Precision Design: Random Noise"*, DS01228

Some of these application notes, and others, are listed in the *"Signal Chain Design Guide"*, DS21825.

NOTES:

6.0 PACKAGING INFORMATION

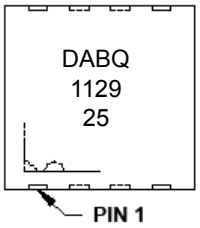
6.1 Package Marking Information

8-Lead DFN (3x3)**(MCP662)**

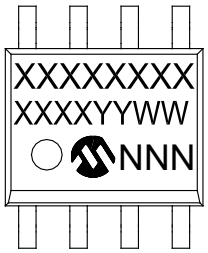
Device	Code
MCP662T-E/MF	DABQ

Note: Applies to 8-Lead 3x3 DFN

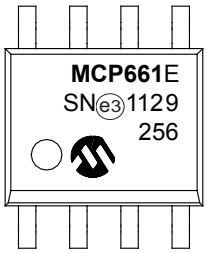
Example



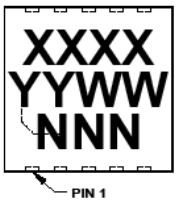
8-Lead SOIC (150 mil) **(MCP661, MCP662, MCP663)**



Example:



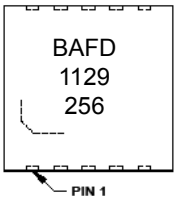
10-Lead DFN (3×3) **(MCP665)**



Device	Code
MCP665	BAFD

Note: Applies to 10-Lead 3x3 DFN

Example

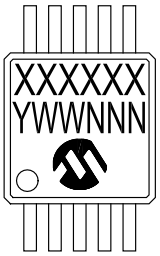


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

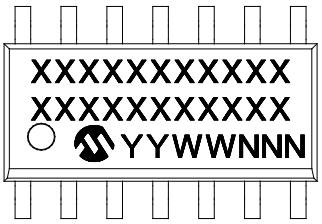
Package Marking Information (Continued)

10-Lead MSOP **(MCP665)**

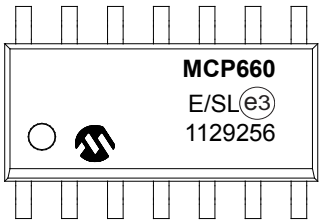


Example:

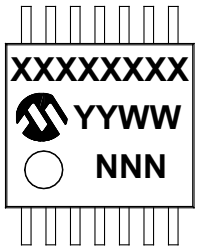
14-Lead SOIC (.150") **(MCP660, MCP664)**



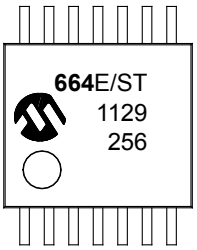
Example



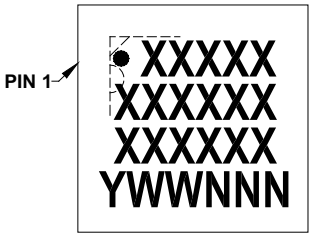
14-Lead TSSOP **(MCP660, MCP664)**



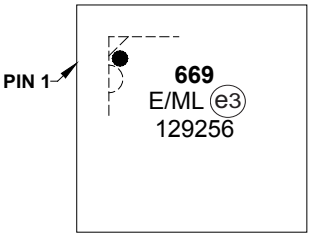
Example



16-Lead QFN (4x4) **(MCP669)**



Example

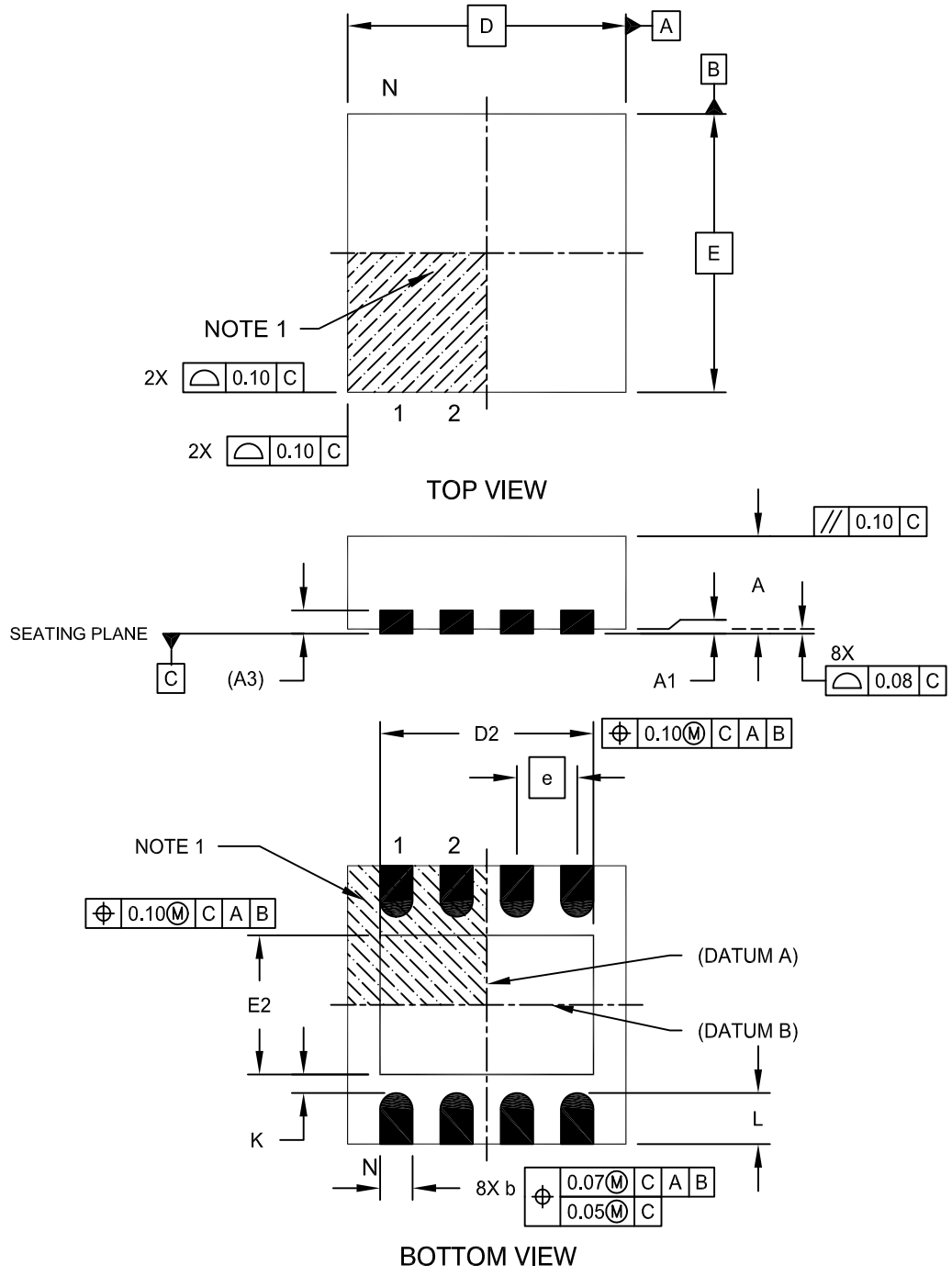


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

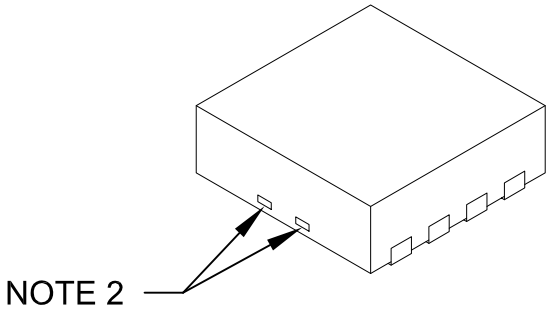
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

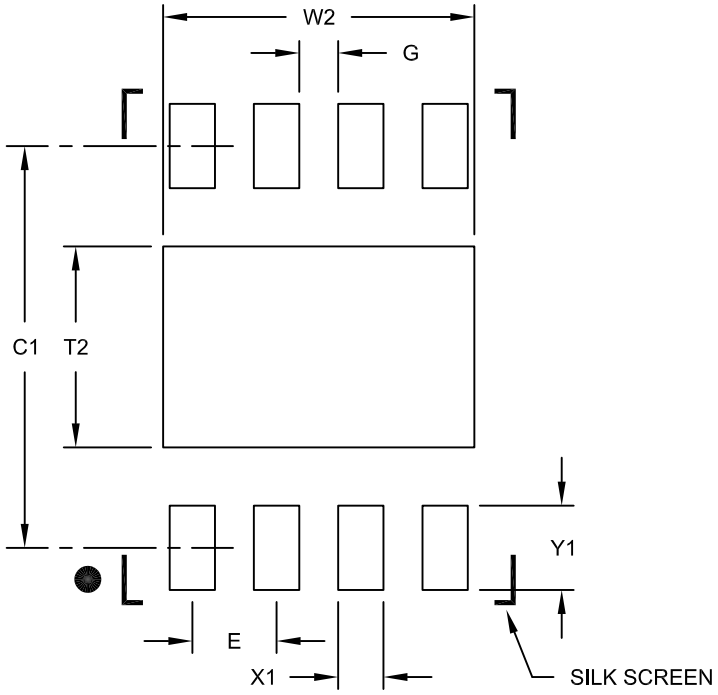
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

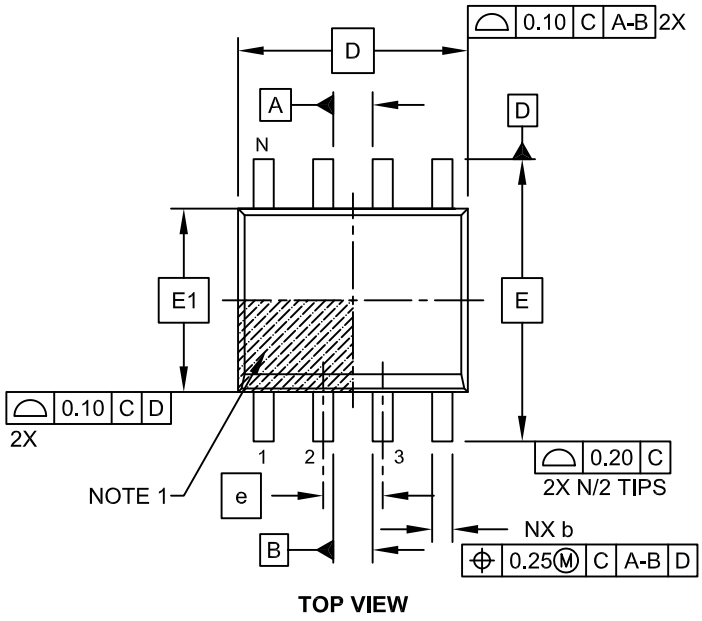
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

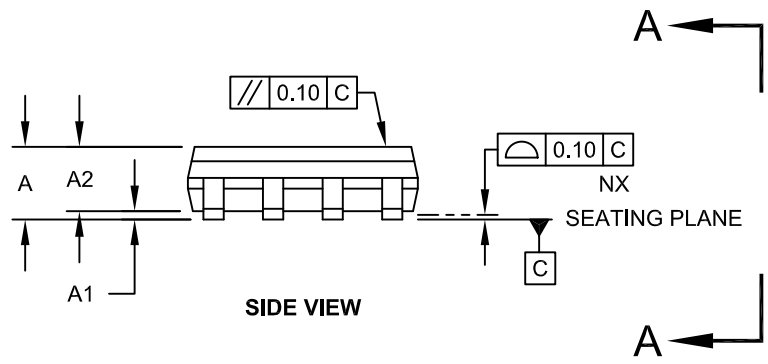
Microchip Technology Drawing No. C04-2062B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

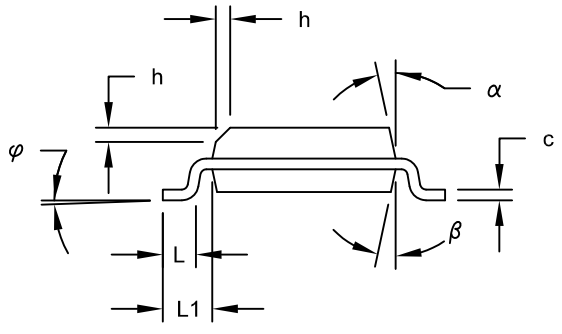
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

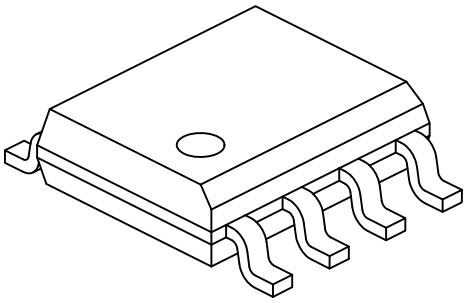


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

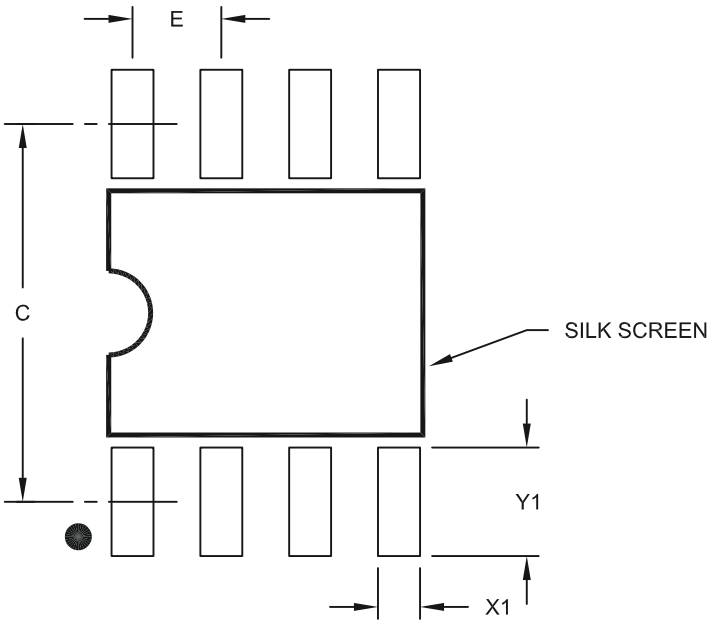
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

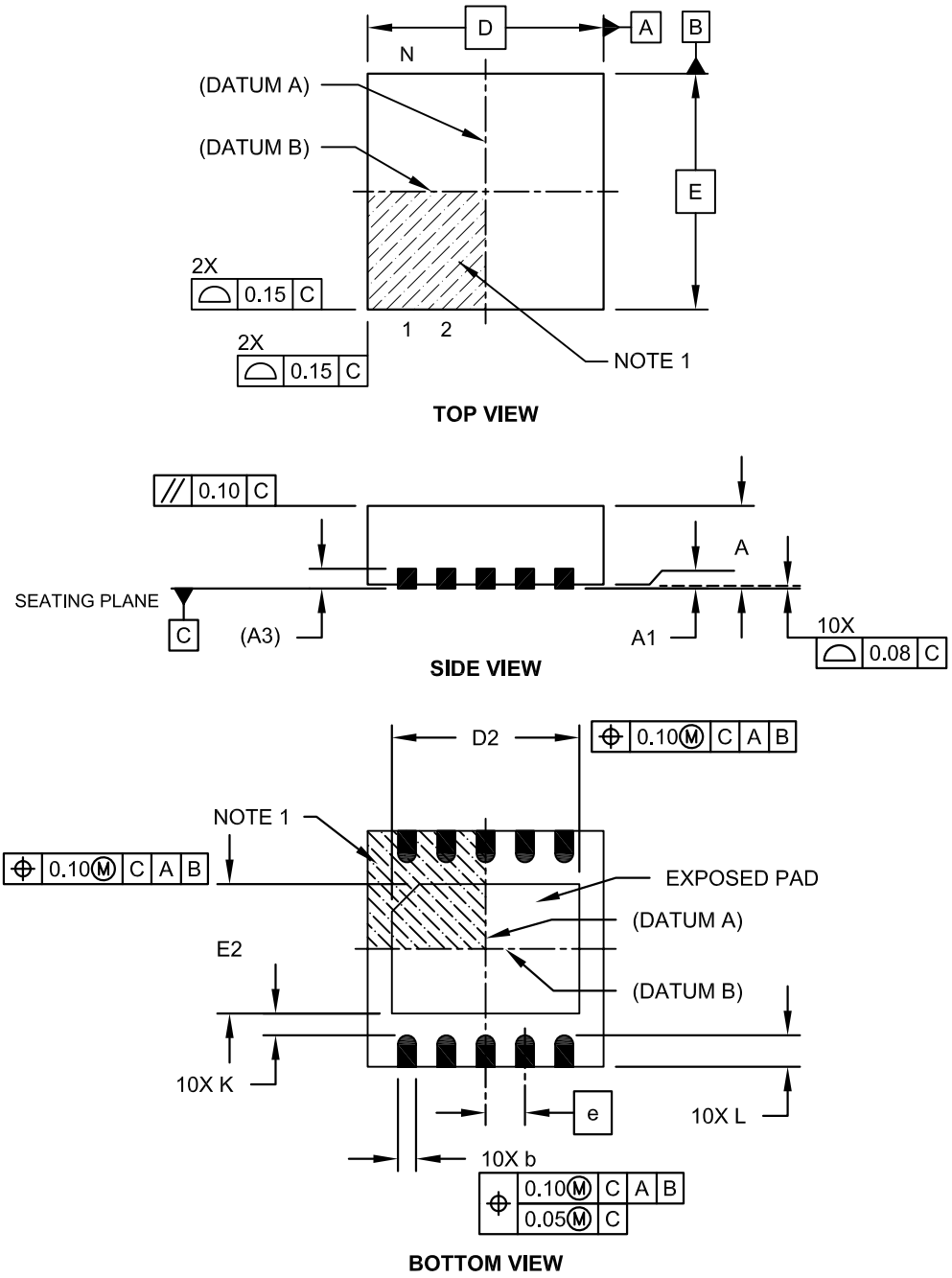
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

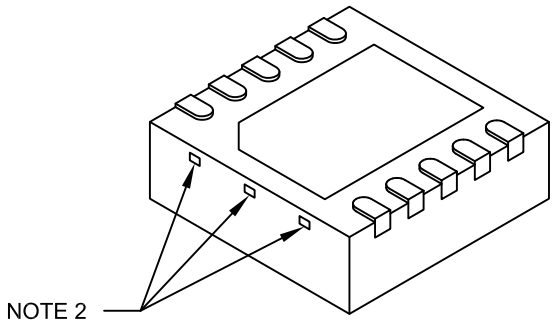
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-063C Sheet 1 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.15	2.35	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.50	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

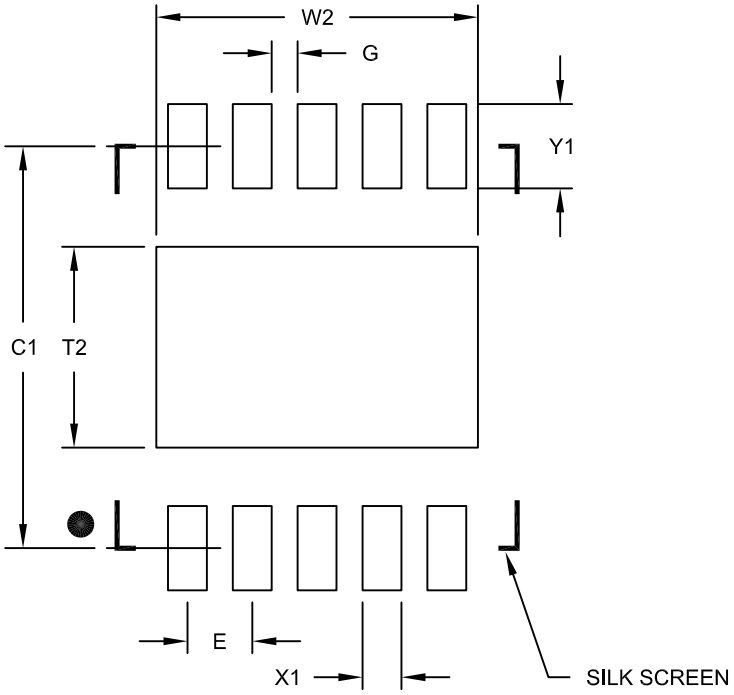
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

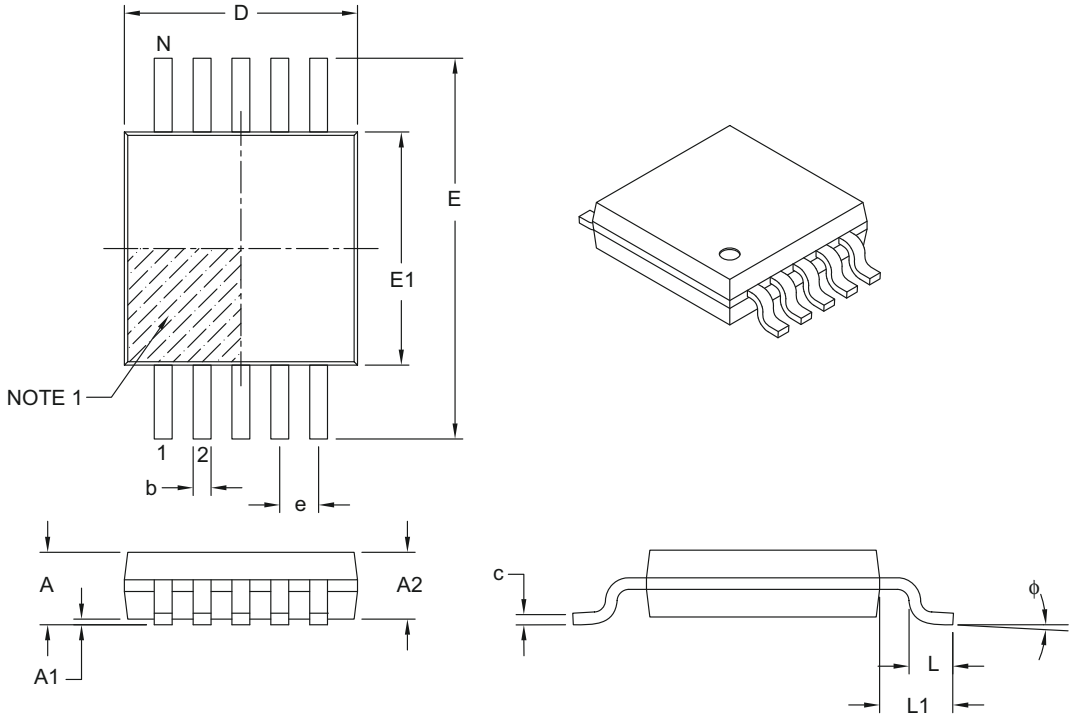
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

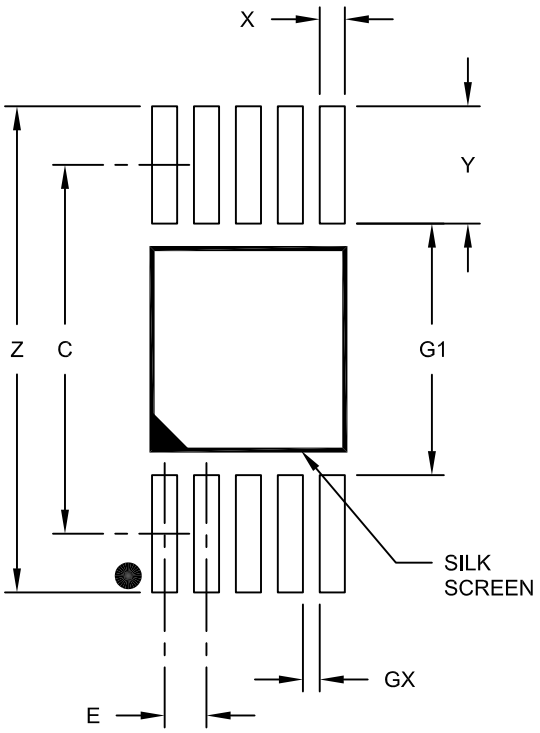
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads	G1	3.00		
Distance Between Pads	GX	0.20		

Notes:

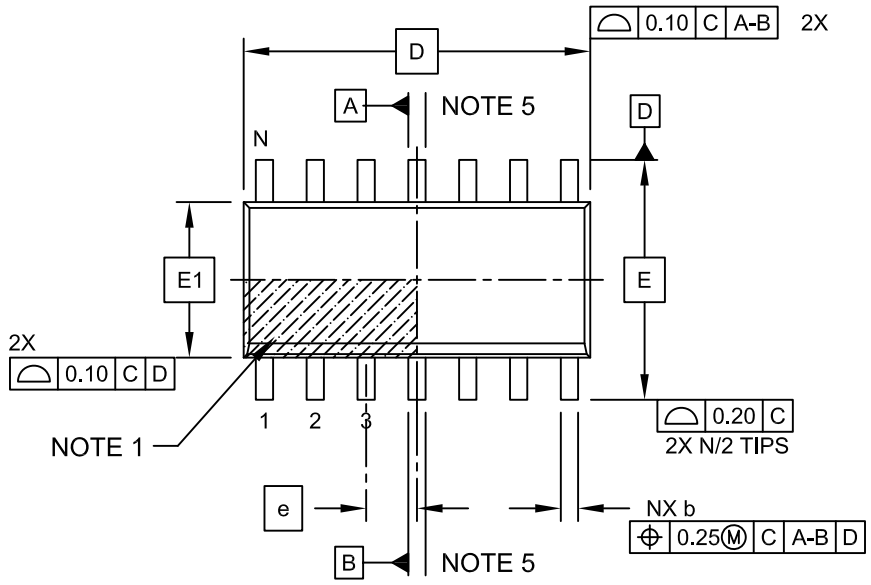
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

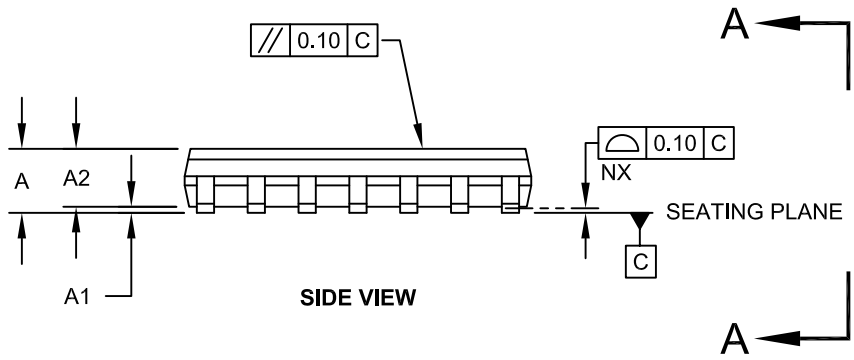
Microchip Technology Drawing No. C04-2021A

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

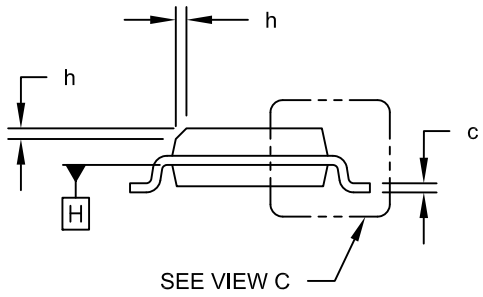
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

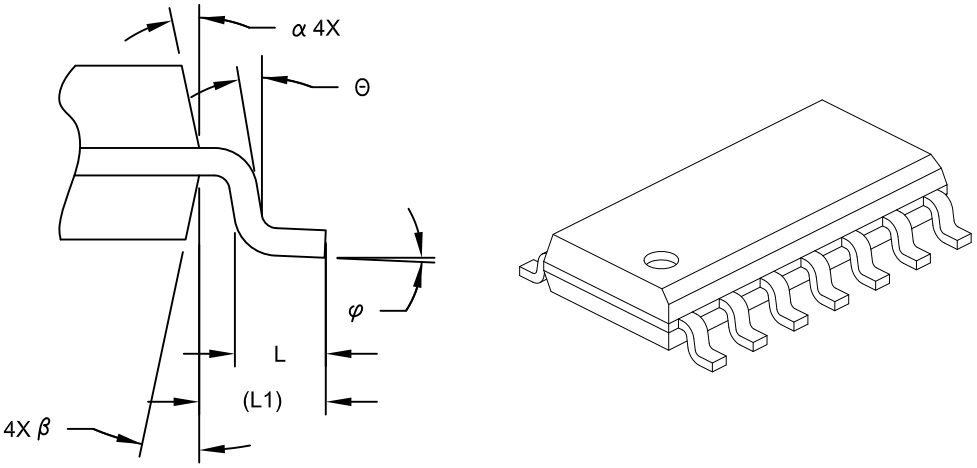


VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

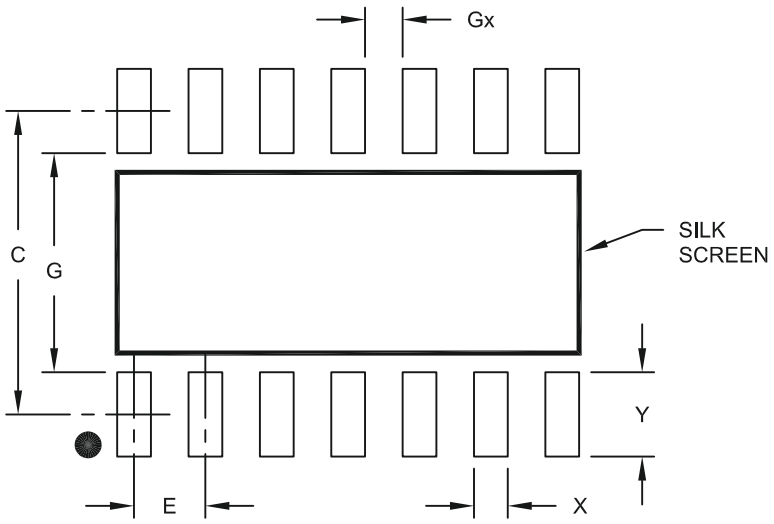
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

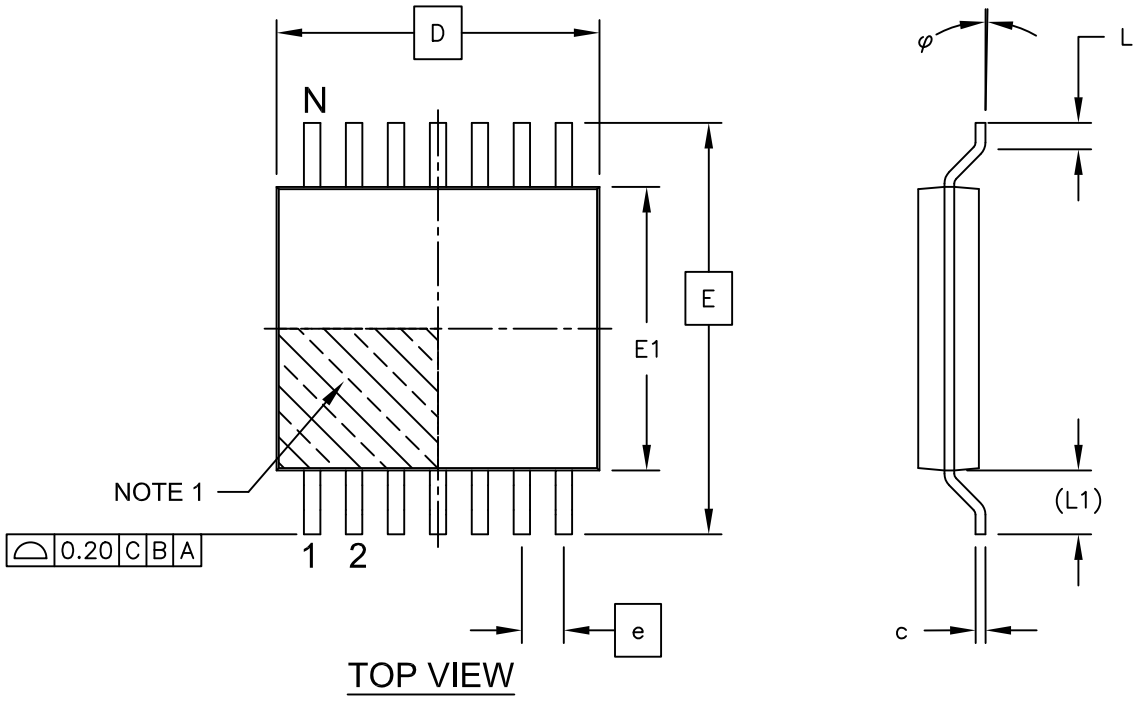
1. Dimensioning and tolerancing per ASME Y14.5M

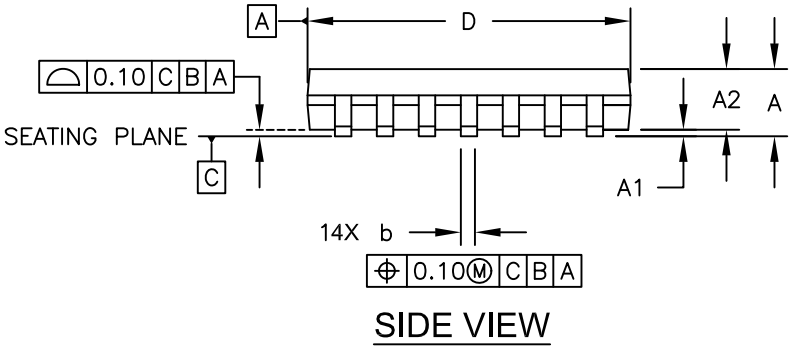
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

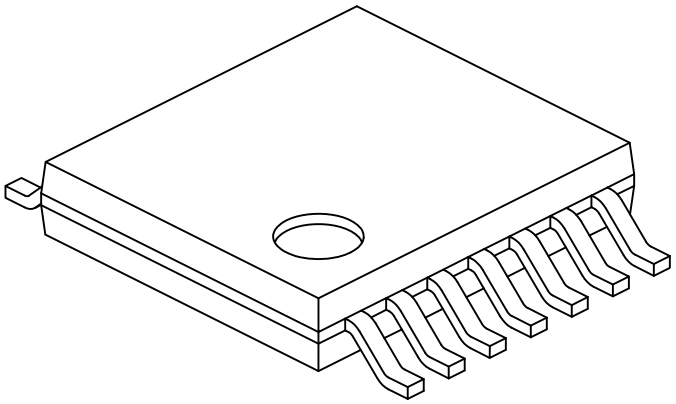




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

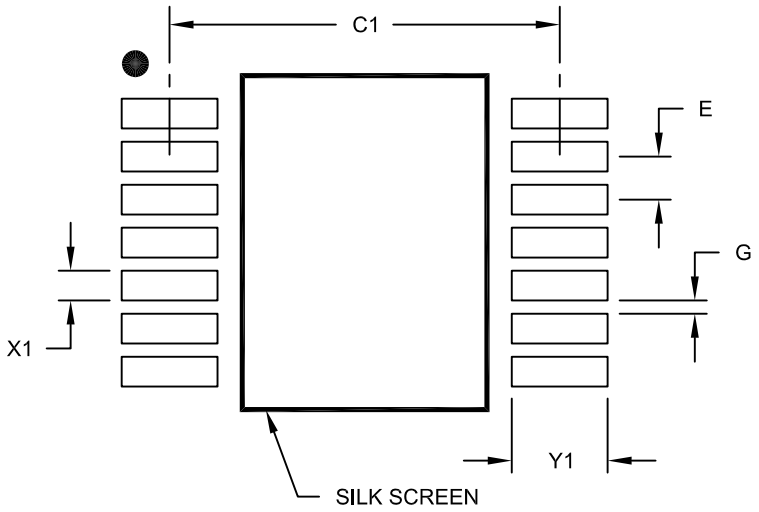
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

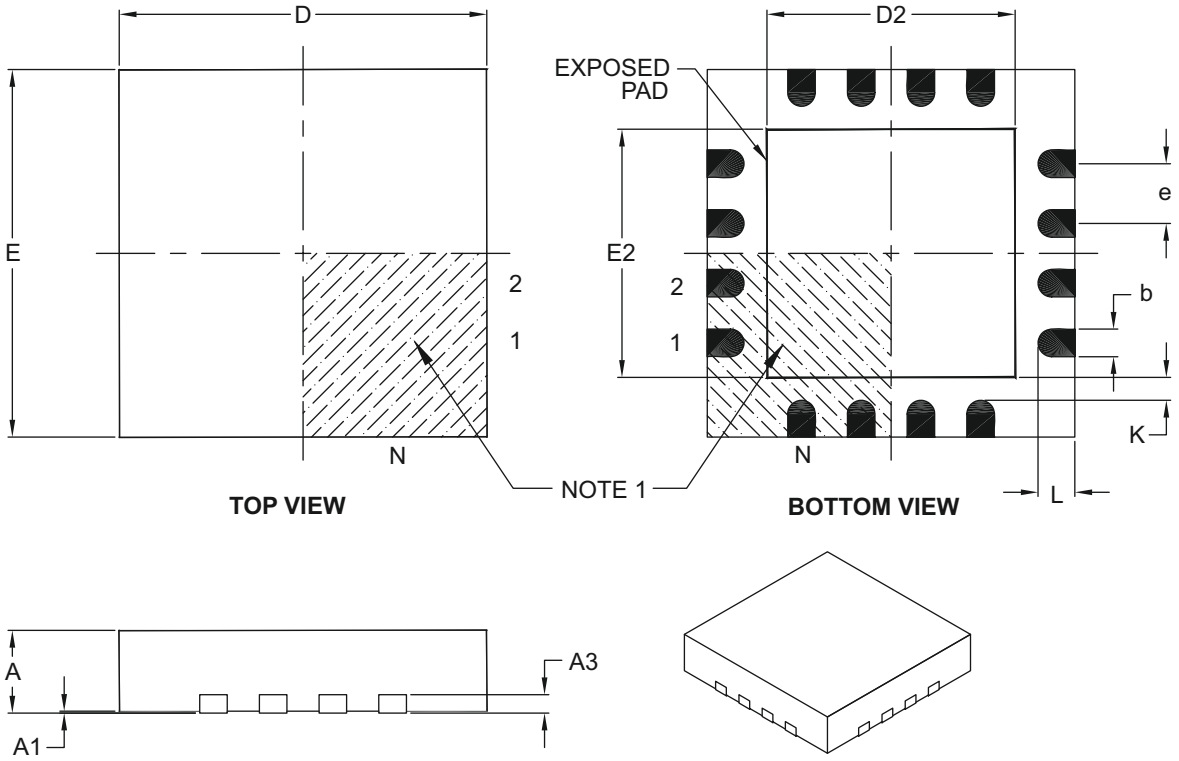
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

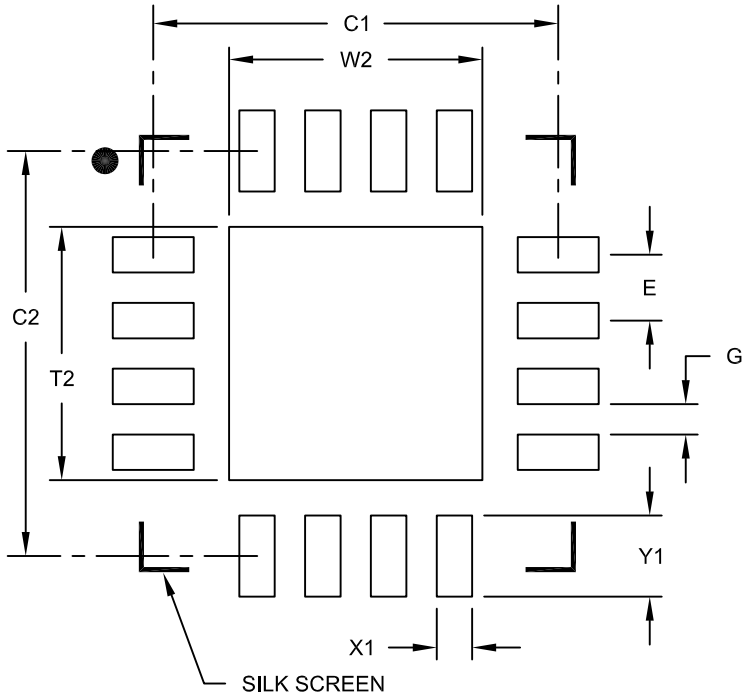
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2011)

The following is the list of modifications:

1. Added the MCP660, MCP664 and MCP669 amplifiers to the product family and the related information throughout the document.
2. Added the 4x4 QFN (16L) package option for MCP660 and MCP669, SOIC and TSSOP (14L) package options for MCP660 and MCP665 and the related information throughout the document. Updated **Package Types** drawing with pin designation for each new package.
3. Updated Table 1-4 to show the temperature specifications for new packages.
4. Updated Table 3-1 to show all the pin functions.
5. Updated **Section 6.0 "Packaging Information"** with markings for the new additions. Added the corresponding SOIC and TSSOP (14L), and 4x4 QFN (16L) package options and related information.
6. Updated table description and examples in **Product Identification System**.

Revision A (July 2009)

Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP660	Triple Op Amp
	MCP660T	Triple Op Amp (Tape and Reel) (SOIC, TSSOP, QFN)
	MCP661	Single Op Amp
	MCP661T	Single Op Amp (Tape and Reel) (SOIC)
	MCP662	Dual Op Amp
	MCP662T	Dual Op Amp (Tape and Reel) (DFN and SOIC)
	MCP663	Single Op Amp with $\overline{CS}$
	MCP663T	Single Op Amp with $\overline{CS}$ (Tape and Reel) (SOIC)
	MCP664	Quad Op Amp
	MCP664T	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
	MCP665	Dual Op Amp with $\overline{CS}$
	MCP665T	Dual Op Amp with $\overline{CS}$ (Tape and Reel) (DFN and MSOP)
	MCP669	Quad Op Amp with $\overline{CS}$
	MCP669T	Quad Op Amp with $\overline{CS}$ (Tape and Reel) (QFN)
Temperature Range:	E =	-40°C to +125°C
Package:	MF =	Plastic Dual Flat, No Lead (3×3 DFN), 8-lead, 10-lead
	ML =	Plastic Quad Flat, No Lead Package (4x4 QFN), (4x4x0.9 mm), 16-lead
	SL =	Plastic Small Outline, Narrow, (3.90 mm SOIC), 14-lead
	SN =	Plastic Small Outline (3.90 mm), 8-lead
	ST =	Plastic Thin Shrink Small Outline, (4.4 mm TSSOP), 14-lead
	UN =	Plastic Micro Small Outline (MSOP), 10-lead

Examples:

a)	MCP660T-E/ML:	Tape and Reel Extended temperature, 16LD QFN package
b)	MCP660T-E/SN:	Tape and Reel Extended temperature, 14LD SOIC package
c)	MCP660T-E/ST:	Tape and Reel Extended temperature, 14LD TSSOP package
d)	MCP661T-E/SN:	Tape and Reel Extended temperature, 8LD SOIC package
e)	MCP662T-E/MF:	Tape and Reel Extended temperature, 8LD DFN package
f)	MCP662T-E/SN:	Tape and Reel Extended temperature, 8LD SOIC package
g)	MCP663T-E/SN:	Tape and Reel Extended temperature, 8LD SOIC package
h)	MCP664T-E/SN:	Tape and Reel Extended temperature, 14LD SOIC package
i)	MCP664T-E/ST:	Tape and Reel Extended temperature, 14LD TSSOP package
j)	MCP665T-E/MF:	Tape and Reel Extended temperature, 10LD DFN package
k)	MCP665T-E/UN:	Tape and Reel Extended temperature, 10LD MSOP package
l)	MCP669T-E/ML:	Tape and Reel Extended temperature, 16LD QFN package

NOTES:

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