SY89295U

General Description

The SY89295U is a programmable delay line that delays the input signal using a digital control signal. The delay can vary from 3.2ns to 14.8ns in 10ps increments. In addition, the input signal is LVPECL, uses either a 2.5V ±5% or 3.3V ±10% power supply, and is guaranteed over the full industrial temperature range (–40°C to +85°C).

The delay varies in discrete steps based on a control word. The control word is 10-bits long and controls the delay in 10ps increments. The eleventh bit is D[10] and is used to simultaneously cascade the SY89295U which allows for a larger delay range. In addition, the input pins IN and /IN default to an equivalent low state when left floating. Further, for maximum flexibility, the control register interface accepts CMOS or TTL level signals.

For applications that require an analog delay input, see the SY89296L which is a programmable delay chip with fine tune control. The SY89295U and SY89296U are part of Micrel's high-speed, Precision Edge® product line.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

- Precision LVPECL programmable delay line
- Guaranteed AC performance over temperature and voltage:
  - >1.5GHz f_{MAX}
  - <160ps rise/fall times
- Low-jitter design:
  - <10ps$_{PP}$ total jitter
  - <2ps$_{RMS}$ cycle-to-cycle jitter
  - <1ps$_{RMS}$ random jitter
- Programmable delay range: 3.2ns to 14.8ns in 10ps increments
- Increased monotonicity over the MIC100EP195
- ±10ps INL
- V_{BB} output reference voltage
- Parallel inputs accepts LVPECL or CMOS/LVTTL
- Low voltage operation: 2.5V ±5% and 3.3V ±10%
- Industrial –40°C to +85°C temperature range
- Available in 32-pin (5mm × 5mm) MLF® and 32-pin TQFP packages

Applications

- Clock de-skewing
- Timing adjustments
- Aperture centering

March 2011

Ordering Information[1]

| Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89295UMI	MLF-32	Industrial	SY89295U	Sn-Pb
SY89295UMI TR[2]	MLF-32	Industrial	SY89295U	Sn-Pb
SY89295UTI	T32-1	Industrial	SY89295U	Sn-Pb
SY89295UTITR[2]	T32-1	Industrial	SY89295U	Sn-Pb
SY89295UMG[3]	MLF-32	Industrial	SY89295U with Pb-Free bar-line indicator	Pb-Free NiPd Au
SY89295UMGTR[2, 3]	MLF-32	Industrial	SY89295U with Pb-Free bar-line indicator	Pb-Free NiPd Au
SY89295UTG[3]	T32-1	Industrial	SY89295U with Pb-Free bar-line indicator	Pb-Free NiPd Au
SY89295UTGTR[2, 3]	T32-1	Industrial	SY89295U with Pb-Free bar-line indicator	Pb-Free NiPd Au

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

Pin Configuration
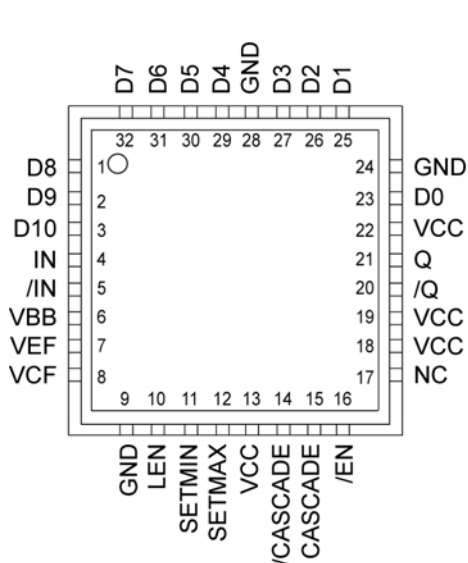
32-Pin MLF® (MLF-32)
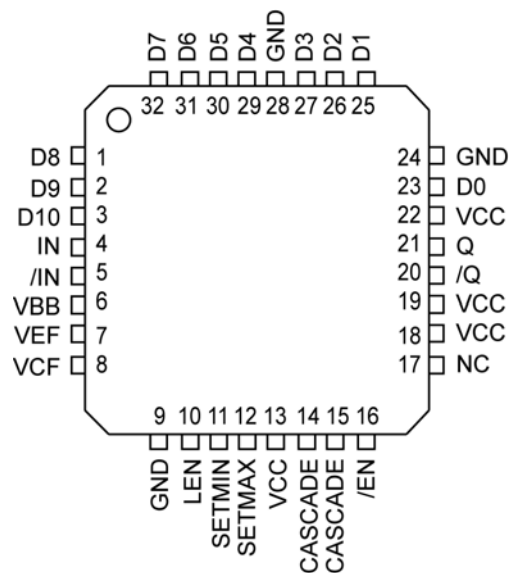
32-Pin TQFP (T32-1)

Truth Tables

Input/Output

Inputs		Outputs	
IN	/IN	OUT	/OUT
0	1	0	1
1	0	1	0

Digital Control Latch

LEN	Latch Action
0	Pass Through D[10:0]
1	Latched

Input Enable

/EN	Q, /Q
0	IN, /IN Delayed
1	Latched D[10:0]

Functional Block Diagram
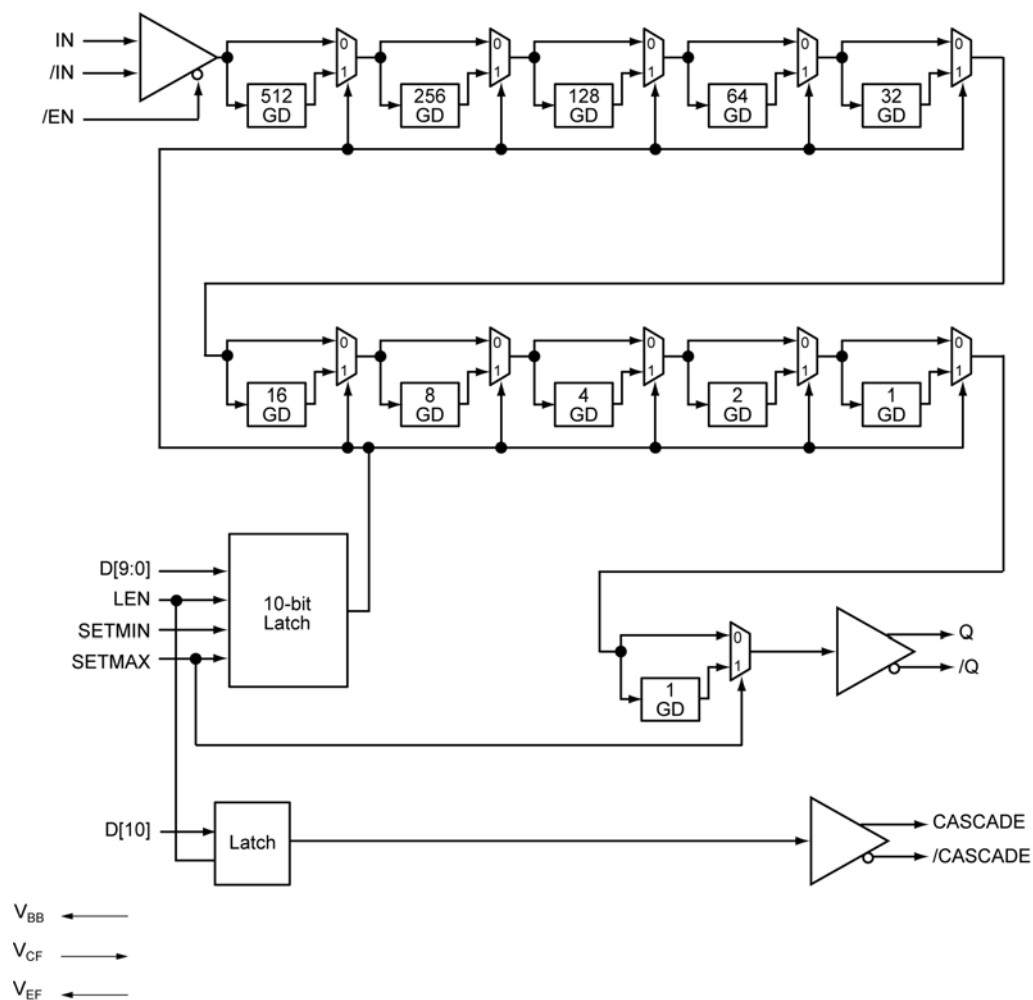
SY89295U Block Diagram

Pin Description

Pin Number	Pin Name	Pin Function
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[9:0]	CMOS, ECL, or TTL Control Bits: These control signals adjust the delay from IN to Q. See "AC Electrical Characteristics" for delay values. In addition, see "Interface Applications" section which illustrates the proper interfacing techniques for different logic standards. D[9:0] contains pull-downs and defaults LOW when left floating. D0 (LSB), and D9 (MSB). See "Typical Operating Characteristics" for delay information.
3	D10	CMOS, ECL, or TTL Control Bit: This bit is used to cascade devices for an extended delay range. In addition, it drives CASCADE, and /CASCADE. Further, D[10] contains a pull-down and defaults LOW when left floating.
4, 5	IN, /IN	LVPECL/ECL Signal Input: Input signal to be delayed. IN contains a 75ký pull-down and will default to a logic LOW if left floating.
6	VBB[1]	Reference Voltage Output: When using a single-ended input signal source to IN or /IN, connect the unused input of the differential pair to this pin. This pin can also be used to re-bias AC-coupled inputs to IN and /IN. When used, de-couple to V_{CC} using a 0.01µF capacitor, otherwise leave floating if not used. Maximum sink/source is ±0.5mA.
7	VEF	Reference Voltage Output: Connect this pin to V_{CF} when D[9:0], and D[10] is ECL..

		Logic Standard	V_{CF} Connects to:
7	VEF	LVPECL	$V_{EF,}$[1]
		CMOS	No Connect
		TTL	1.5V Source

Pin Number	Pin Name	Pin Function
8	VCF	Reference Voltage Input: The voltage driven on V_{CF} sets the logic transition threshold for D[9:0], and D[10].
9, 24, 28	GND, Exposed Pad[2]	Negative Supply: For MLF® package, exposed pad must be connected to a ground plane that is the same potential as the ground pin.
10	LEN	ECL Control Input: When HIGH latches the D[9:0] and D[10] bits. When LOW, the D[9:0] and D[10] latches are transparent.
11	SETMIN	ECL Control Input: When HIGH, D[9:0] registers are reset. When LOW, the delay is set by SETMAX or D[9:0] and D[10]. SETMIN contains a pull-down and defaults LOW when left floating.
12	SETMAX	ECL Control Input: When SETMAX is set HIGH and SETMIN is set LOW, D[9:0] = 1111111111. When SETMAX is LOW, the delay is set by SETMIN or D[9:0] and D[10]. SETMAX contains a pull-down and defaults LOW when left floating.
13, 18, 19, 22	VCC	Positive Power Supply: Bypass with 0.1µF and 0.01µF low ESR capacitors.
14, 15	/Cascade, Cascade	LVPECL Differential Output: The outputs are used when cascading two or more SY89295U to extend the delay range.
16	/EN	LVPECL Single-Ended Control Input: When LOW, Q is delayed from IN. When HIGH, Q is a differential LOW. /EN contains a pull-down and defaults LOW when left floating.
20, 21	/Q, Q	LVPECL Differential Output: Q is a delayed version of IN. Always terminate the output with 50Ω to $V_{CC} - 2V$. See "Output Interface Applications" section.
17	NC	No Connect.

Notes:

1. Single-ended operation is only functional at 3.3V.

2. MLF® package only.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
    Continuous...50mA
    Surge 100mA
Lead Temperature (soldering, 20 sec.)................... +260°C
Storage Temperature Range (T_S).............–65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}).............................. +2.375V to +3.6V
Ambient Temperature (T_A)........................–40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
    Still-Air ···35°C/W
MLF® (ψ_{JB})
    Junction-to-Board ·······································28°C/W
TQFP (θ_{JA})
    Still-Air ···28°C/W
TQFP (ψ_{JB})
    Junction-to-Board ·······································20°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply	V_{CC} = 2.5V	2.375	2.5	2.625	V
		V_{CC} = 3.3V	3	3.3	3.6	
I_{EE}	Power Supply Current	No load, max. V_{CC}			220	mA
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	150		1200	mV
V_{DIFF_IN}	Differential Input Voltage Swing (IN, /IN)	See Figure 1b.	300		2400	mV
V_{IHCMR}	Input High Common Mode Range	IN, /IN	V_{EE} + 1.2		V_{CC}	V

V_{CC} = 3.3V, T_A = –40°C to 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage (IN, /IN)		2.075		2.420	V
V_{IL}	Input Low High Voltage (IN, /IN)		1.355		1.675	V
V_{BB}	Output Voltage Reference		1.775	1.875	1.975	V
V_{EF}	Mode Connection		1.9	2.0	2.1	V
V_{CF}	Input Select Voltage		1.55	1.65	1.75	V

Notes:

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Thermal performance on MLF® packages assumes exposed pad is soldered (or equivalent) to the device most negative potential (GND).

4. The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. Input and output parameters vary 1:1 with V_{CC}, with the exception of V_{CF}.

DC Electrical Characteristics[4] (Continued)

V_{CC} = 2.5V, T_A = –40°C to 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage (IN, /IN)		1.275		1.62	V
V_{IL}	Input Low High Voltage (IN, /IN)		0.555		0.875	V
V_{BB}	Output Voltage Reference		1.175	1.075	0.975	V
V_{EF}	Mode Connection		1.10	1.20	1.30	V
V_{CF}	Input Select Voltage		1.15	1.25	1.35	V

LVPECL Outputs DC Electrical Characteristics[4]

V_{CC} = 3.3V; R_{LOAD} = 50Ω to V_{CC}−2V; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		2.155	2.280	2.405	V
V_{OL}	Output LOW Voltage (Q, /Q)		1.355	1.480	1.605	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1.1	1.6		V

LVPECL Outputs DC Electrical Characteristics[5]

V_{CC} = 2.5V; R_{LOAD} = 50Ω to V_{CC}−2V; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Output HIGH Voltage (Q, /Q)		1.355	1.480	1.605	V
I_{EE}	Output LOW Voltage (Q, /Q)		0.555	0.68	0.805	V
V_{IN}	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1.1	1.6		V

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	µA
I_{IL}	Input LOW Current		–300			µA

Notes:

5. The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. V_{OH} and V_{OL} parameters vary 1:1 with V_{CC}.

6. The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC Electrical Characteristics[7]

T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Operating Frequency	Clock $V_{OUT} \geq 400mV$	1.5			GHz
t_{pd}	Propagation Delay IN to Q; D[0–10]=0 IN to Q; D[0–10]=1023 /EN to Q: D[0–10]=0 D10 to CASCADE		3200 11500 3400 350		4200 14800 4400 670	ps
t_{RANGE}	Programmable Range t_{pd} (max.) – t_{pd} (min)		8300			ps
t_{SKEW}	Duty Cycle Skew $t_{PHL} - t_{PLH}$	**Note 8**			25	ps
Δt	Step Delay D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High D0-D9 High			10 15 35 70 145 290 575 1150 2300 4610 9220		ps
INL	Integral Non-Linearity	**Note 9**		±10		ps
t_S	Setup Time D to LEN D to IN /EN to IN	 **Note 10** **Note 11**	200 350 300			ps
t_H	Hold Time LEN to D IN to /EN	 **Note 12**	200 400			ps

Notes:

7. High-frequency AC electricals are guaranteed by design and characterization.

8. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the crosspoint of the output.

9. INL (Integral Non-Linearity) is defined from its corresponding point on the ideal delay versus D[9:0] curve as the deviation from its ideal delay. The maximum difference is the INL. Theoretical Ideal Linearity (TIL) = (measured maximum delay – measured minimum delay) ÷ 1024. INL = measured delay – measured minimum delay + (step number ∞ TIL).

10. This setup time defines the amount of time prior to the input signal. The delay tap of the device must be set.

11. This setup time defines the amount of the time that /EN must be asserted prior to the next transition of IN, /IN to prevent an output response greater than ±75mV to the IN, /IN transition.

12. Hold time is the minimum time that /EN must remain asserted after a negative going IN or a positive going /IN to prevent an output response greater than ±75mV to the IN, /IN transition.

AC Electrical Characteristics[7]

T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_R	Release Time /EN to IN SETMAX to LEN SETMIN to LEN		 500 500 450			ps
t_{JITTER}	Cycle-to-Cycle Jitter Total Jitter Random Jitter	**Note 13** **Note 14** **Note 15**			2 10 1	ps_{RMS} ps_{PP} ps_{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80% (Q) 20% to 80% (Cascade)	50 90	85	160 300	ps
	Duty Cycle		45		55	%

Notes:

13. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles over a random sample of adjacent cycle pairs. $T_{jitter\_cc} = T_n - T_n+1$, where T is the time between rising edges of the output signal.

14. Total jitter definition: With an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

15. Random jitter definition: Jitter that is characterized by a Gaussian distribution, unbounded and is quantified by its standard deviation and mean. Random jitter is measured with a K28.7 comma defect pattern, measured at 1.5Gbps.

Typical Operating Characteristics

V_{CC} = 3.3V, GND = 0, D_{IN} = 100mV, T_A = 25ºC, unless otherwise stated.

Delay vs. D[9:0]

DELAY (ps) vs D[9:0]

Amplitude vs. Frequency

AMPLITUDE (mV) vs FREQUENCY (MHz)
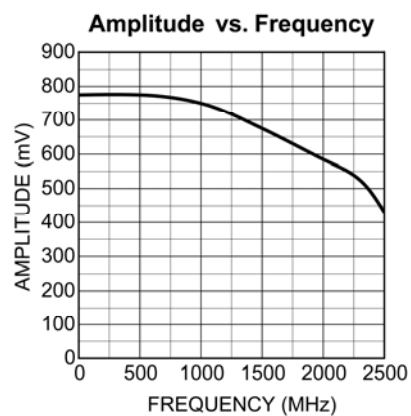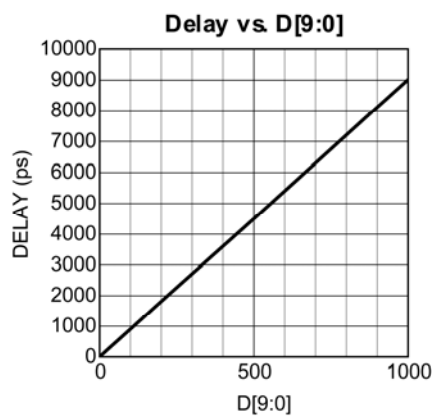
Timing Diagrams
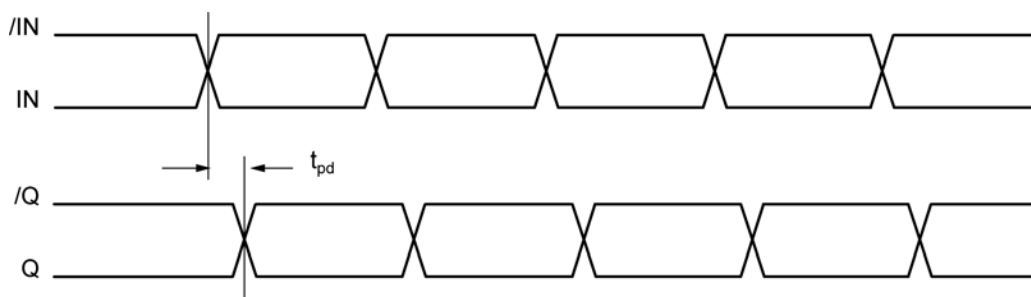
Single-Ended and Differential Swings
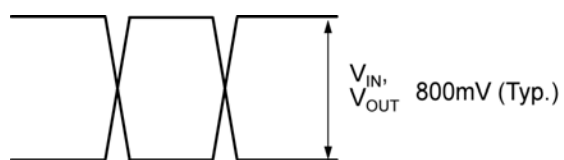
Figure 1a. Single-Ended Voltage Swing
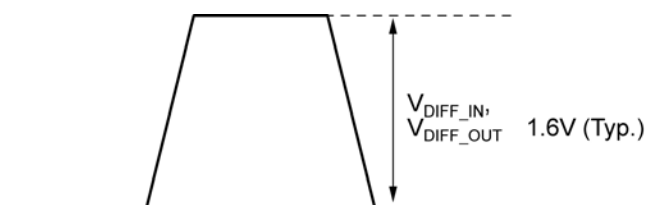
Figure 1b. Differential Voltage Swing

Input and Output Stages
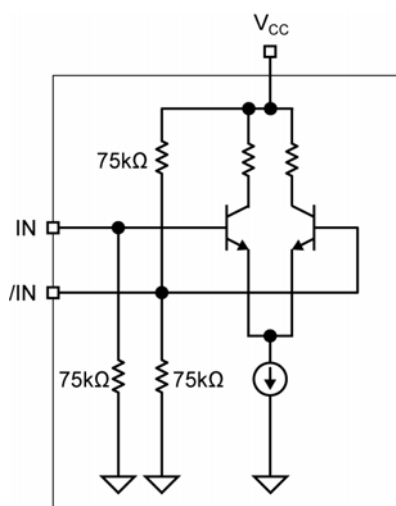
Figure 2a. Differential Input Stage
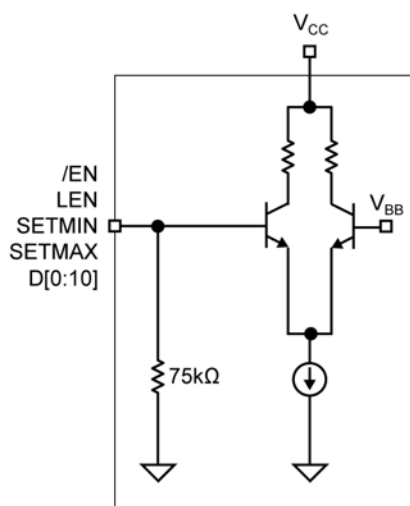
Figure 2b. Single-Ended Input Stage
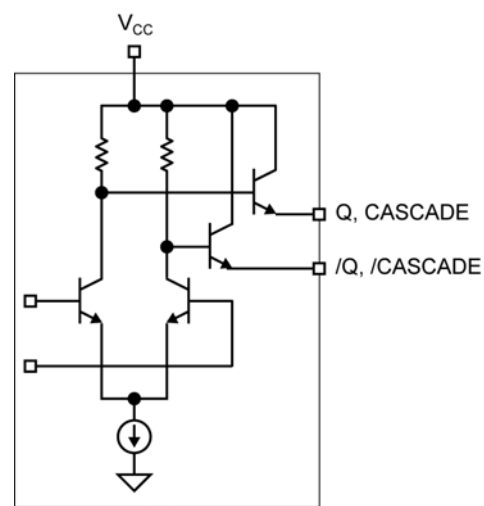
Figure 3. LVPECL Output Stage

Output Interface Applications
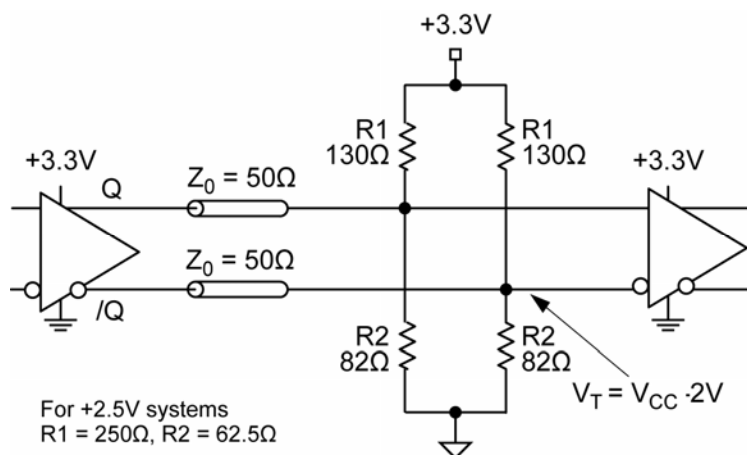
Figure 4. Parallel Termination
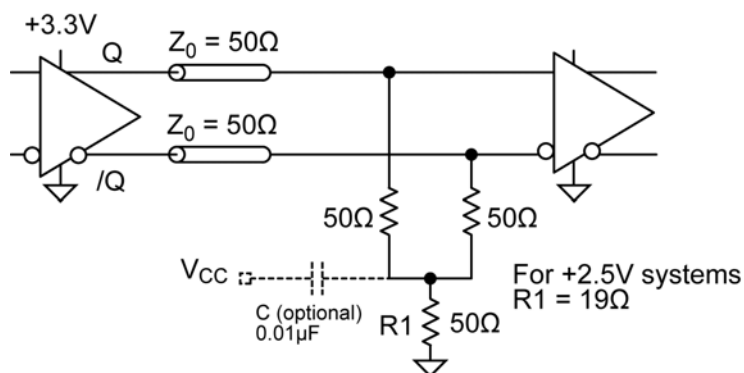
Figure 5. Y-Termination
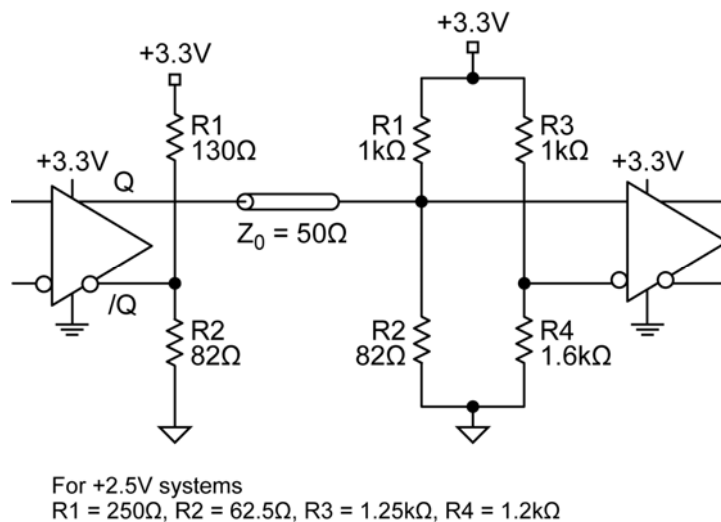
Figure 6. Terminating Unused I/O

Applications Information

For best performance, use good high-frequency layout techniques, filter V_{CC} supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY89295U data inputs and outputs.

V_{BB} Reference

The VBB pin is an internally generated reference and is available for use only by the SY89295U. When unused, this pin should be left unconnected. Two common uses for V_{BB} are to handle a single-ended PECL input, and to re-bias inputs for AC-coupling applications.

If IN and /IN are driven by a single-ended output, V_{BB} is used to bias the unused input. Please refer to Figure 10. The PECL signal driving the SY89295U may optionally be inverted in this case.

When the signal is AC-coupled, V_{BB} is used, as shown in Figure 13, to re-bias IN and /IN. This ensures that SY89295U inputs are within acceptable common mode range.

In all cases, V_{BB} current sinking or sourcing must be limited to 0.5mA or less.

Setting D Input Logic Thresholds

In all designs where the SY89295U GND supply is at zero volts, the D inputs can accommodate CMOS and TTL level signals, as well as PECL or LVPECL. Figures 11, 12 and 14 show how to connect V_{CF} and V_{EF} for all possible cases.

Cascading

Two or more SY89295U may be cascaded in order to extend the range of delays permitted. Each additional SY89295U adds about 3.2ns to the minimum delay and adds another 10240ps to the delay range.

Internal cascade circuitry has been included in the SY89295U. Using this internal circuitry, the SY89295U may be cascaded without any external gating.

Examples of cascading 2, 3, or 4 SY89295U appear in Figures 7, 8, and 9.
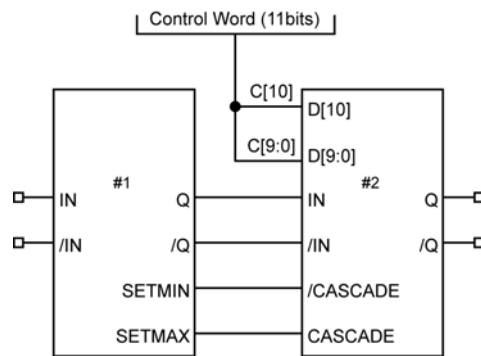
Figure 7. Cascading Two SY89295U
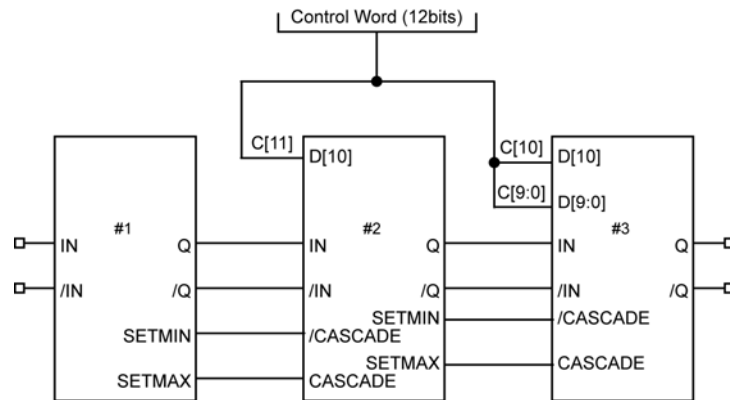
Figure 8. Cascading Three SY89295U
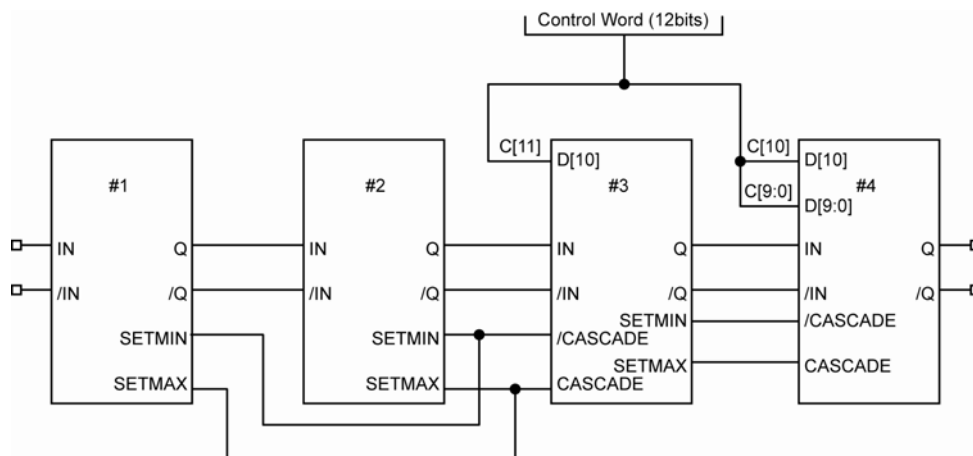
Figure 8. Cascading Four SY89295U

hbwhelp@micrel.com or (408) 955-1690

Interface Applications
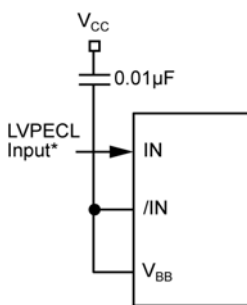
**Figure 10. Interfacing to a
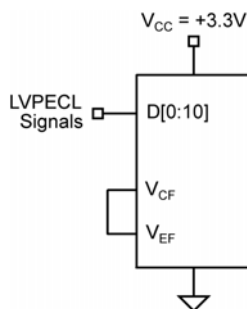Single-Ended LVPECL Signal**

**Figure 11. V_{CF}/V_{EF} Biasing for
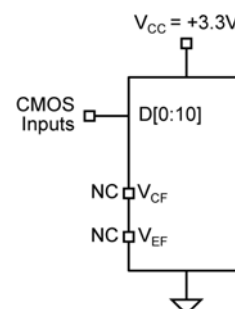LVPECL Control (D) Input**
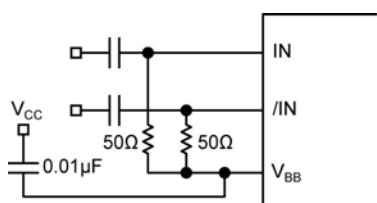

**Figure 12. V_{CF}/V_{EF} Biasing for
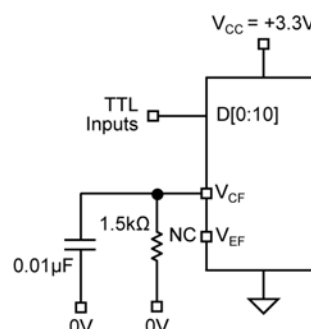CMOS (D) Input**


**Figure 13. Re-Biasing an
AC-Coupled Signal**

**Figure 14. V_{CF}/V_{EF} Biasing for
LVTTL Control (D) Input**

Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY89295U	2.5/3.3V 1.5GHz Precision LVPECL Programmable Delay	www.micrel.com/product-info/products/sy89295u.shtml
SY89296U	2.5/3.3V 1.5GHz Precision LVPECL Programmable Delay with Fine Tune Control	www.micrel.com/product-info/products/sy89296u.shtml
	16-MLF Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_appnote_0902.pdf
	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

Package Information
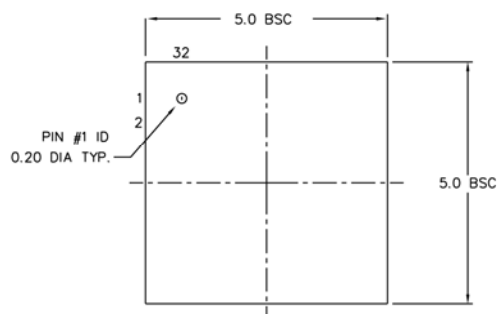
TOP VIEW

BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
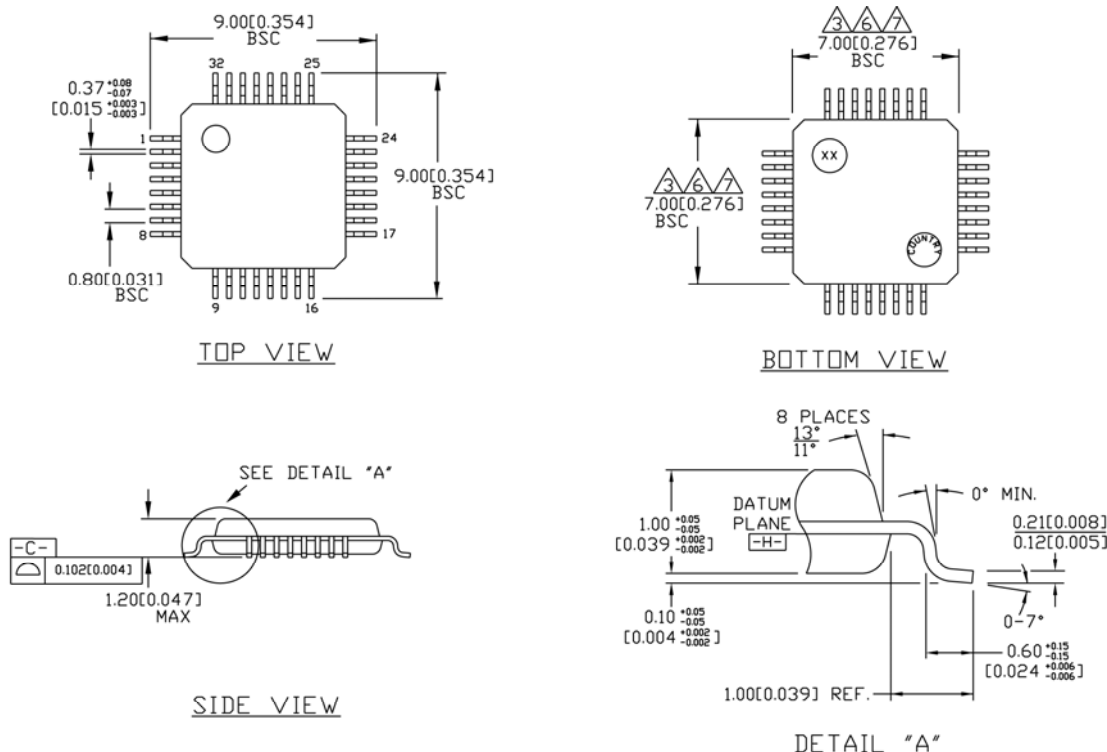7. APPLIED FOR EXPOSED PAD AND TERMINALS.
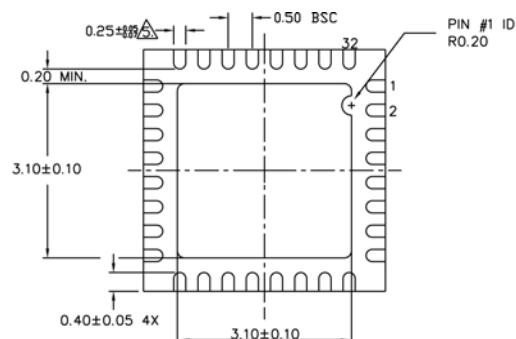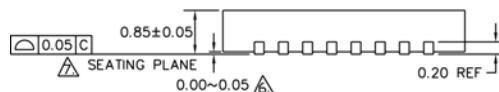
SIDE VIEW

MLF55Q-32LD-PD-2-B
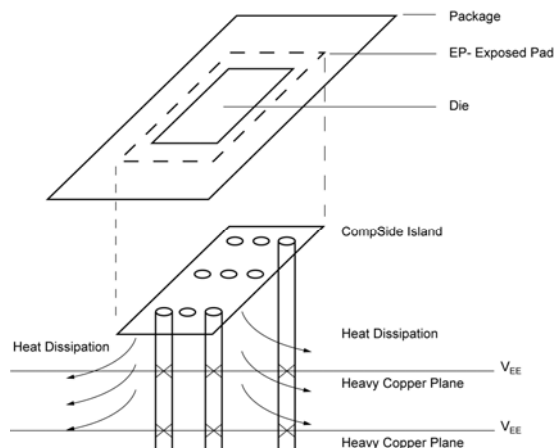
PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualifications

2. All parts are dry-packed before shipment.

3. Exposed pads must be soldered to a ground for proper thermal management.

32-Pin MLF® (MLF-32)

Package Information (Continued)

TOP VIEW

9.00[0.354] BSC

0.37 +0.08 -0.07 [0.015 +0.003 -0.003]

9.00[0.354] BSC

0.80[0.031] BSC

BOTTOM VIEW

7.00[0.276] BSC

7.00[0.276] BSC

SIDE VIEW

SEE DETAIL "A"

-C-

0.102[0.004]

1.20[0.047] MAX

DETAIL "A"

8 PLACES 13° 11°

0° MIN.

DATUM PLANE -H-

1.00 +0.05 -0.05 [0.039 +0.002 -0.002]

0.21[0.008] 0.12[0.005]

0.10 +0.05 -0.05 [0.004 +0.002 -0.002]

0-7°

0.60 +0.15 -0.15 [0.024 +0.006 -0.006]

1.00[0.039] REF.

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

32-Pin TQFP (T32-1)