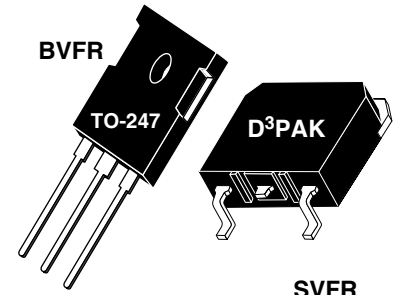
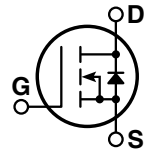


POWER MOS V® FREDFET

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **Avalanche Energy Rated**
- **Lower Leakage**
- **FAST RECOVERY BODY DIODE**
- **TO-247 or Surface Mount D³PAK Package**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT1201R6BVFR_SVFR	UNIT
V_{DSS}	Drain-Source Voltage	1200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	8	Amps
I_{DM}	Pulsed Drain Current ^①	32	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	280	Watts
	Linear Derating Factor	2.24	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	8	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1200			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	8			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 4A$)			1.600	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1200V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT1201R6BVFR_SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{GS} = 0V		3050	3660	pF
C _{OSS}	Output Capacitance	V _{DS} = 25V		255	360	
C _{RSS}	Reverse Transfer Capacitance	f = 1 MHz		125	190	
Q _g	Total Gate Charge ^③	V _{GS} = 10V		155	230	nC
Q _{gs}	Gate-Source Charge	V _{DD} = 0.5 V _{DSS}		15	23	
Q _{gd}	Gate-Drain ("Miller") Charge	I _D = I _D [Cont.] @ 25°C		78	115	
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V		12	24	ns
t _r	Rise Time	V _{DD} = 0.5 V _{DSS}		10	20	
t _{d(off)}	Turn-off Delay Time	I _D = I _D [Cont.] @ 25°C		50	75	
t _f	Fall Time	R _G = 1.6Ω		15	30	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			8	Amps
I _{SM}	Pulsed Source Current ^① (Body Diode)			32	
V _{SD}	Diode Forward Voltage ^② (V _{GS} = 0V, I _S = -I _D [Cont.])			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			18	V/ns
t _{rr}	Reverse Recovery Time (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		220	ns
		T _j = 125°C		450	
Q _{rr}	Reverse Recovery Charge (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		1.0	μC
		T _j = 125°C		3.0	
I _{RPM}	Peak Recovery Current (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		10	Amps
		T _j = 125°C		14	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.45	°C/W
R _{θJA}	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471
- ④ Starting T_j = +25°C, L = 37.81mH, R_G = 25Ω, Peak I_L = 8A
- ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ I_D-8A di/dt ≤ 700A/μs v_R ≤ 1200V T_j ≤ 150°C

APT Reserves the right to change, without notice, the specifications and information contained herein.

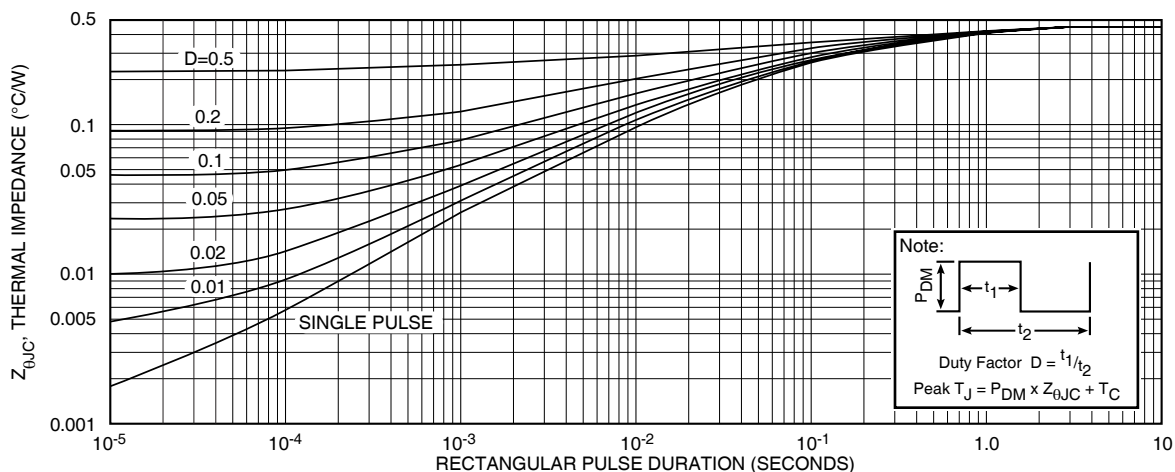


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

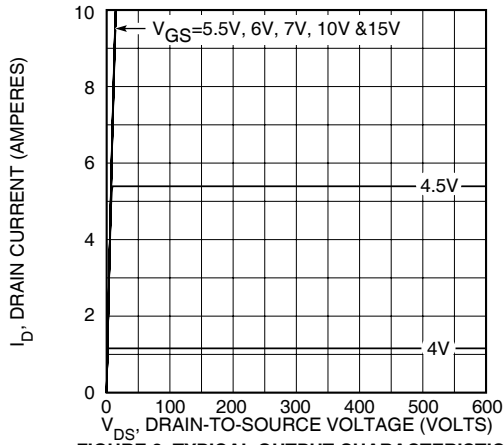


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

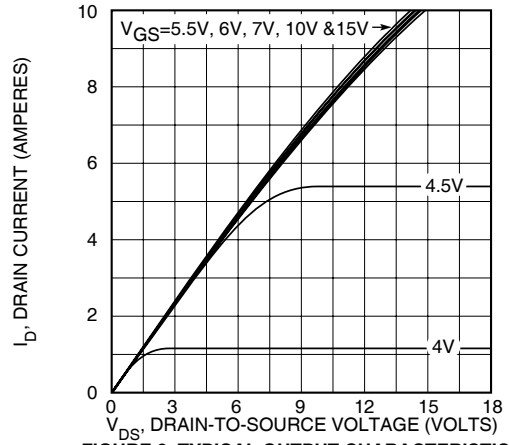


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

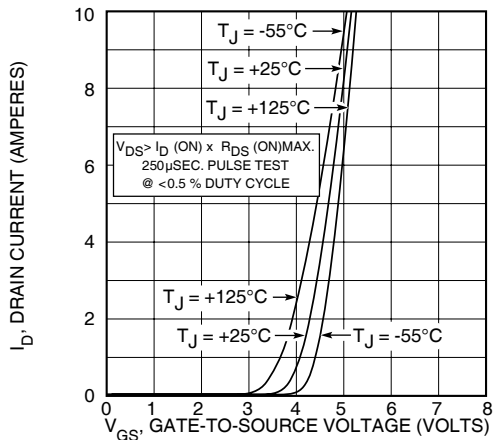


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

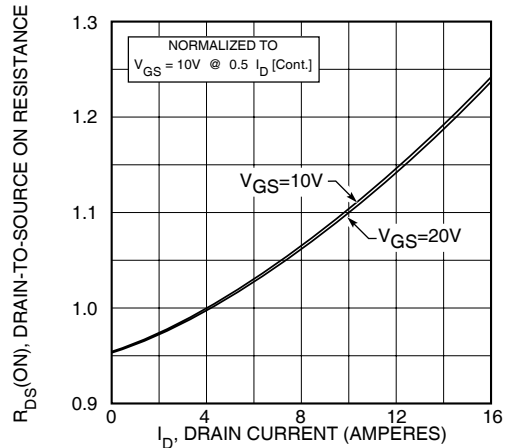


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

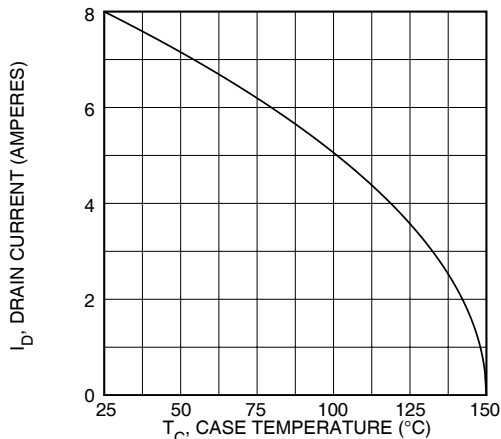


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

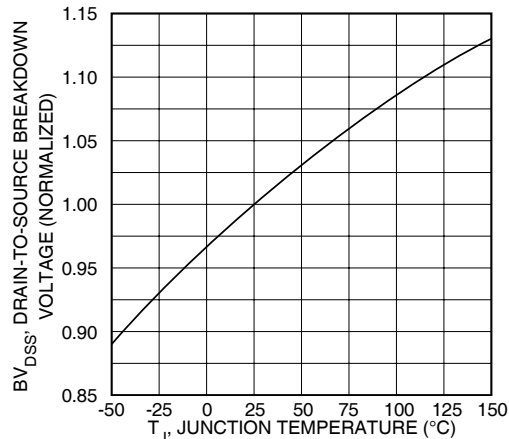


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

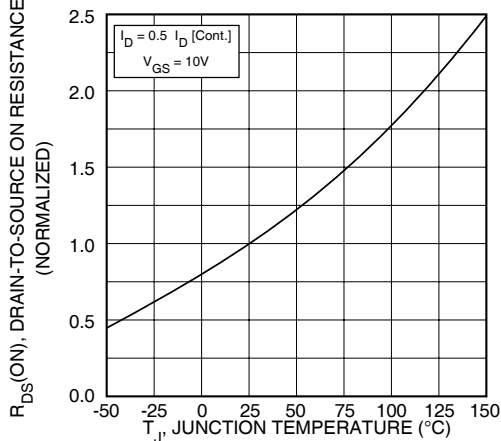


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

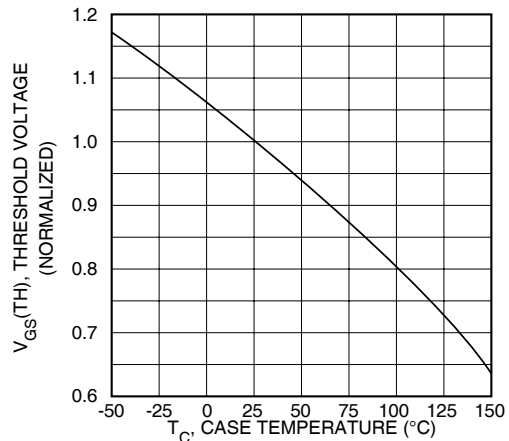


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

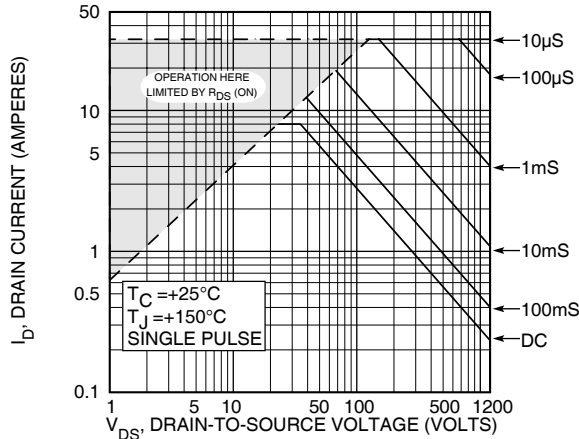


FIGURE 10, MAXIMUM SAFE OPERATING AREA

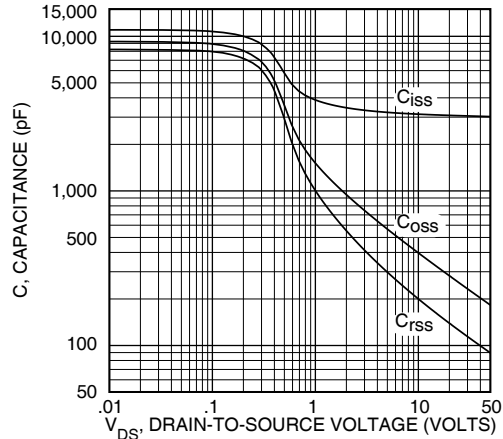


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

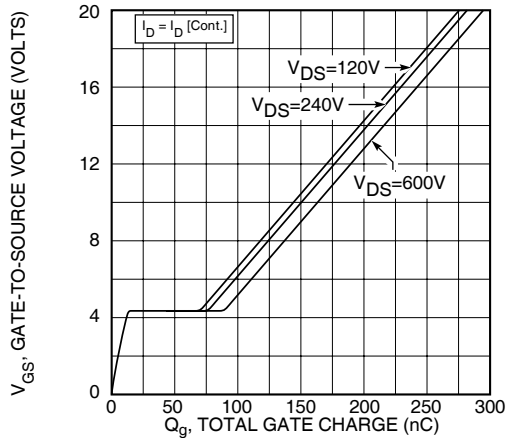


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

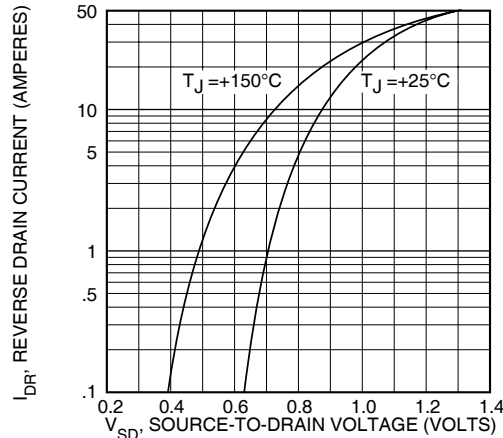
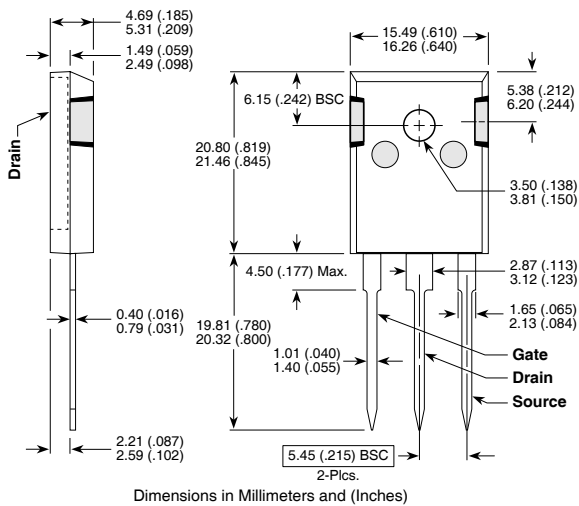
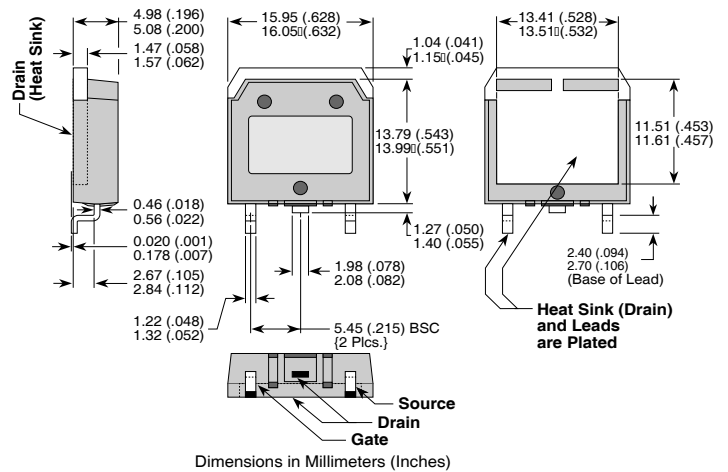


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)



D³PAK Package Outline (SVFR)



050-5849 Rev A 6-2004

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.