Features

- Single 2.7V - 3.6V Supply
- Dual-interface Architecture
  - RapidS™ Serial Interface: 50 MHz Maximum Clock Frequency (SPI Modes 0 and 3 Compatible for Frequencies up to 33 MHz)
  - Rapid8™ 8-bit Interface: 20 MHz Maximum Clock Frequency
- Page Program
  - 16,384 Pages (1,056 Bytes/Page) Main Memory
- Sector Erase Architecture
  - Sixty-three 270,336-byte Sectors
  - One 261,888-byte Sector
  - One 8,488-byte Sector
- Two 1056-byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 10 mA Active Read Current Typical – Serial Interface
  - 12 mA Active Read Current Typical – 8-bit Interface
  - 15 µA CMOS Standby Current Typical
- Hardware Data Protection
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100 Program/Erase Cycles Per Sector Minimum
- Data Retention – 10 Years
- Commercial Temperature Range

Description

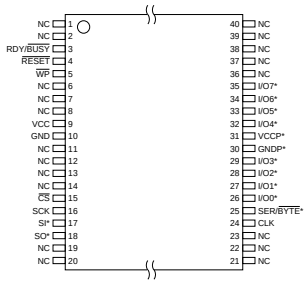
The AT45CS1282 is a 2.7-volt, dual-interface sequential access Flash memory ideally suited for infrequent code shadowing applications. This device utilizes Atmel's e-STAC™ Multi-Level Cell (MLC) memory technology, which allows a single cell to

Pin Configurations

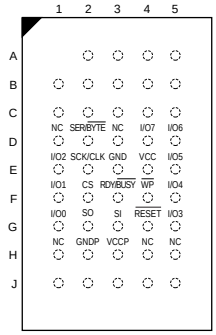
Pin Name	Function
$\overline{CS}$	Chip Select
SCK/CLK	Serial Clock/Clock
SI	Serial Input
SO	Serial Output
I/O7 - I/O0	8-bit Input/Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy
SER/$\overline{BYTE}$	Serial/8-bit Interface Control

Note: *Optional Use – See pin description text for connection information.

TSOP Top View: Type 1



CBGA Top View



128-megabit 2.7-volt Dual-interface Code Shadow DataFlash®

AT45CS1282

Preliminary

e-STAC™

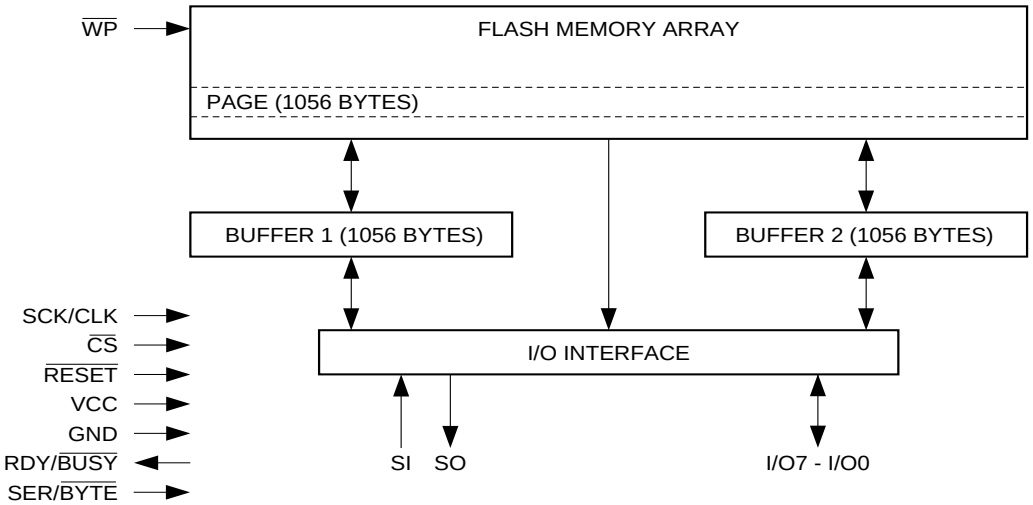
Rev. 3447A–DFLSH–2/04

store two bits of information delivering a very cost effective high density Flash memory. The AT45CS1282 supports RapidS serial interface and Rapid8 8-bit interface. RapidS serial interface is SPI compatible for frequencies up to 33 MHz. The dual-interface allows a dedicated serial interface to be connected to a DSP and a dedicated 8-bit interface to be connected to a microcontroller or vice versa. However, the use of either interface is purely optional. Its 138,412,032 bits of memory are organized as 16,384 pages of 1,056 bytes each. In addition to the 132-megabit main memory, the AT45CS1282 also contains two SRAM buffers of 1,056 bytes each. The buffers allow the receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses either a RapidS serial interface or a 8-bit Rapid8 interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial applications where high-density, low-pin count, low-voltage and low-power are essential. The device operates at clock frequencies up to 50 MHz with a typical active read current consumption of 10 mA.

To allow for simple in-system reprogrammability, the AT45CS1282 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45CS1282 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK), or an 8-bit interface consisting of the input/output pins (I/O7 - I/O0) and the clock pin (CLK).

All programming and erase cycles are self-timed.

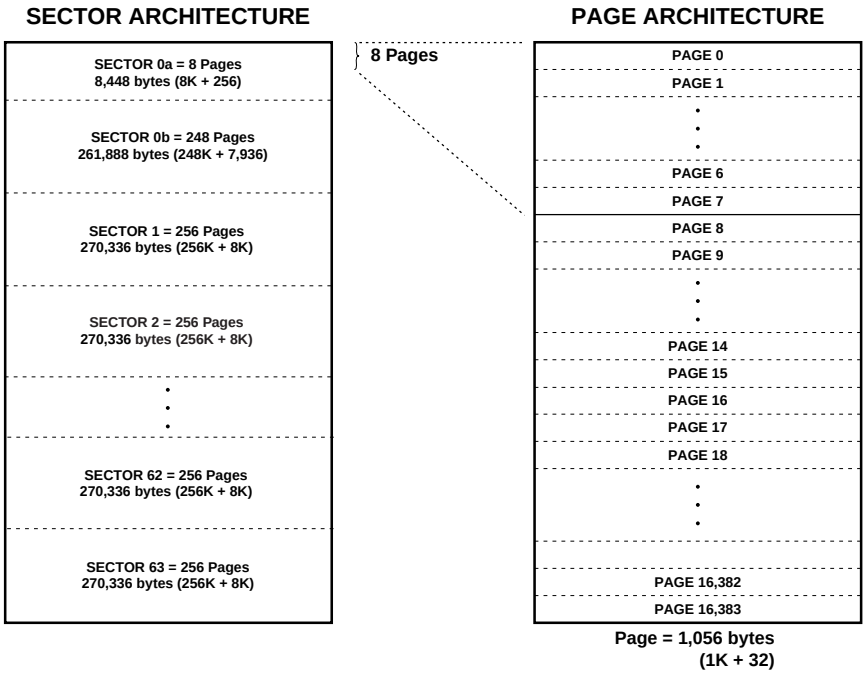
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45CS1282 is divided into two levels of granularity comprising of sectors, and pages. The “Memory Architecture Diagram” illustrates the breakdown of each level and details the number of pages per sector. All program operations to the DataFlash occur on a page by page basis. The erase operations is performed at the sector level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 through 4. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK/CLK pin controls the loading of the opcode and the desired buffer or main memory address location through either the SI (serial input) pin or the 8-bit input pins (I/O7 - I/O0). All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Buffer addressing is referenced in the datasheet using the terminology BFA10 - BFA0 to denote the 11 address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA13 - PA0 and BA10 - BA0, where PA13 - PA0 denotes the 14 address bits required to designate a page address and BA10 - BA0 denotes the 11 address bits required to designate a byte address within the page.

Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS and Rapid8 protocols for Mode 0 and Mode 3. Please refer to the “Detailed Bit-level Read Timing” diagrams in this datasheet for details on the clock cycle sequences for each mode.

CONTINUOUS ARRAY READ: By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read, an opcode of E8H must be clocked into the device followed by four address bytes (which comprises 7 don’t care bits plus the 25-bit page and byte address sequence) and a series of don’t care clock cycles (24 if using the serial interface or 19 if using the 8-bit interface). The first 14 bits (PA13 - PA0) of the

25-bit address sequence specify which page of the main memory array to read, and the last 11 bits (BA10 - BA0) of the 25-bit address sequence specify the starting byte address within the page. The 24 or 19 don't care clock cycles that follow the four address bytes are needed to initialize the read operation. Following the don't care clock cycles, additional clock pulses on the SCK/CLK pin will result in data being output on either the SO (serial output) pin or the eight output pins (I/O7- I/O0).

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit (or byte if using the 8-bit interface mode) in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7-I/O0). The maximum SCK/CLK frequency allowable for the Continuous Array Read is defined by the f_{CAR} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

MAIN MEMORY PAGE READ: A main memory page read allows the user to read data directly from any one of the 16384 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, an opcode of D2H must be clocked into the device followed by four address bytes (which comprise 7 don't care bits plus the 25-bit page and byte address sequence) and a series of don't care clock cycles (24 if using the serial interface or 19 if using the 8-bit interface). The first 14 bits (PA13 - PA0) of the 25-bit address sequence specify the page in main memory to be read, and the last 11 bits (BA10 - BA0) of the 25-bit address sequence specify the starting byte address within that page. The 24 or 19 don't care clock cycles that follow the four address bytes are sent to initialize the read operation. Following the don't care bytes, additional pulses on SCK/CLK result in data being output on either the SO (serial output) pin or the eight output pins (I/O7 - I/O0). The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7 - I/O0). The maximum SCK/CLK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. With the serial interface, an opcode of D4H is used to read data from buffer 1, and an opcode of D6H is used to read data from buffer 2. Likewise with the 8-bit interface an opcode of 54H is used to read data from buffer 1 and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the opcode must be clocked into the device followed by four address bytes comprised of 21 don't care bits and 11 buffer address bits (BFA10 - BFA0). Following the four address bytes, additional don't care bytes (one byte if using the serial interface or two bytes if using the 8-bit interface) must be clocked in to initialize the read operation. Since the buffer size is 1056 bytes, 11 buffer address bits are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7 - I/O0).

Program and Erase Commands

BUFFER WRITE: Data can be clocked in from the input pins (SI or I/O7 - I/O0) into either buffer 1 or buffer 2. To load data into either buffer, a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by four address bytes comprised of 21 don't care bits and 11 buffer address bits (BFA10 - BFA0). The 11 buffer address bits specify the first byte in the buffer to be written. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM: A previously-erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. The programming time is selectable by the system through the use of different opcodes between a normal mode and a fast mode (the fast program option will consume more current). A 1-byte opcode, 88H for buffer 1 or 89H for buffer 2 (98H for buffer 1 fast program or 99H for buffer 2 fast program), must be clocked into the device followed by four address bytes consisting of 7 don't care bits, 14-page address bits (PA13 - PA0) that specify the page in the main memory to be written and 11 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased using the sector erase commands. The programming of the page is internally self-timed and should take place in a maximum time of t_P for normal programming or t_{FP} for fast programming. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

SECTOR ERASE: The Sector Erase command can be used to individually erase any sector in the main memory. There are 65 sectors and only one sector can be erased at one time. Sector 0a requires a different opcode than sectors 0b-63. To perform a sector 0a erase, an opcode of 50h must be loaded into the device, followed by four address bytes comprised of 7 don't care bits, 11-page address bits (PA13 - PA3) and 14 don't care bits. To perform a sector 0b-63 erase, an opcode of 7Ch must be loaded into the device, followed by four address bytes comprised of 7 don't care bits, 6-page address bits (PA13 - PA8) and 19 don't care bits. The 6-page address bits are used to specify which sector is to be erased. Refer to Sector Erase addressing table. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected sector. The erase operation is internally self-timed and should take place in a maximum time of t_{SE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Sector Erase Addressing

PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Sector
0	0	0	0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	X	X	X	X	X	X	X	X	0b
0	0	0	0	0	1	X	X	X	X	X	X	X	X	1
0	0	0	0	1	0	X	X	X	X	X	X	X	X	2
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	0	X	X	X	X	X	X	X	X	60
1	1	1	1	0	1	X	X	X	X	X	X	X	X	61
1	1	1	1	1	0	X	X	X	X	X	X	X	X	62
1	1	1	1	1	1	X	X	X	X	X	X	X	X	63

Additional Commands

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation, a 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, must be clocked into the device, followed by four address bytes comprised of 7 don't care bits, 14-page address bits (PA13- PA0), which specify the page in main memory that is to be transferred, and 11 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK/CLK pin to load the opcode and the address bytes from the input pins (SI or I/O7 - I/O0). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read or the RDY/$\overline{BUSY}$ can be monitored to determine whether the transfer has been completed.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation, a 1-byte opcode, 60H for buffer 1 and 61H for buffer 2, must be clocked into the device, followed by four address bytes consisting of 7 don't care bits, 14-page address bits (PA13 - PA0) that specify the page in the main memory that is to be compared to the buffer, and 11 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK/CLK pin to load the opcode and the address bytes from the input pins (SI or I/O7 - I/O0). On the low-to-high transition of the $\overline{CS}$ pin, the 1056 bytes in the selected main memory page will be compared with the 1056 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

STATUS REGISTER READ: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode must be loaded into the device. After the opcode and optional dummy byte(s) is clocked in, the 1-byte status register will be clocked out on the output pins (SO or I/O7 - I/O0), starting with the next clock cycle. In case of serial interface, opcode D7H is followed with an optional dummy byte (8 clocks). For Serial applications over 25 MHz, opcode must be always followed with a dummy byte. In case of applications with 8-bit interface, opcode D7H and two dummy clock cycles should be used. When using the serial interface, the data in the status register, starting with the MSB (bit 7), will be clocked out on the SO pin during the next eight clock cycles.

The six most-significant bits of the status register will contain device information, while the remaining two least-significant bits are reserved for future use and will have undefined values. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK/CLK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. Since the data in the status register is constantly updated, the user must toggle SCK/CLK pin to check the ready/busy status. There are four operations that can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program and Sector Erase.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, 3, and 2 of the status register. For the AT45CS1282, the four bits are 0, 1, 0, 0. The decimal value of these four binary bits does not equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The device density is not the same as the density code indicated in the JEDEC device ID information. The device density is provided only for backward compatibility.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	0	1	0	0	X	X

Manufacturer and Device ID Read

This instruction conforms to the JEDEC standard and allows the user to read the Manufacturer ID, Device ID, and Extended Device Information. This mode is only offered via the serial interface with clock frequencies up to 25 MHz. A 1-byte opcode, 9FH, must be clocked into the device while the $\overline{CS}$ pin is low. After the opcode is clocked in, the Manufacturer ID, 2 bytes of Device ID and Extended Device Information will be clocked out on the SO pin. The fourth byte of the sequence output is the Extended Device Information String Length byte. This byte is used to signify how many bytes of Extended Device Information will be output.

Manufacturer and Device ID Information

Byte 1 – Manufacturer ID

Hex Value	JEDEC Assigned Code							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FH	0	0	0	1	1	1	1	1

Manufacturer ID	1FH = Atmel

Byte 2 – Device ID (Part 1)

Hex Value	Family Code			Density Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
29H	0	0	1	0	1	0	0	1

Family Code	001 = DataFlash
Density Code	01001 = 128-Mbit

Byte 3 – Device ID (Part 2)

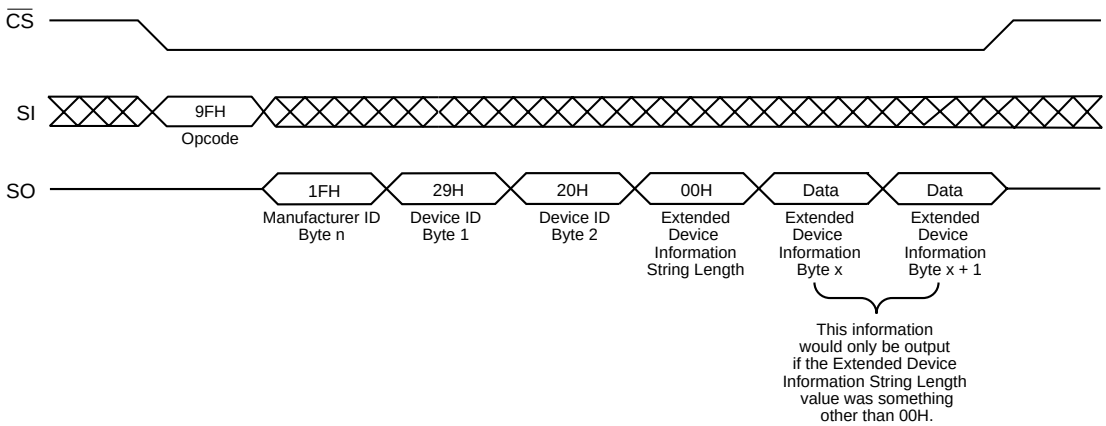
Hex Value	MLC Code			Product Version Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H	0	0	1	0	0	0	0	0

MLC Code	001 = 2-Bit/Cell Technology
Product Version	00000 = Initial Version

Byte 4 – Extended Device Information String Length

Hex Value	Byte Count							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

Byte Count	00H = 0 Bytes of Information



Note: Based on JEDEC publication 106 (JEP106), Manufacturer ID data can be comprised of any number of bytes. Some manufacturers may have Manufacturer ID codes that are two, three or even four bytes long with the first byte(s) in the sequence being 7FH. A system should detect code 7FH as a “Continuation Code” and continue to read Manufacturer ID bytes. The first non-7FH byte would signify the last byte of Manufacturer ID data. For Atmel (and some other manufacturers), the Manufacturer ID data is comprised of only one byte.

Security Register

The AT45CS1282 contains a specialized register that can be used for security purposes in system design. The Security Register is a unique 128-byte register that is divided into two portions. The first 64 bytes (byte 0 to byte 63) of this register are allocated as a one-time user programmable space. Once these 64 bytes have been programmed, they should not be reprogrammed. The remaining 64 bytes of this register (byte 64 to byte 127) are factory programmed by Atmel and will contain a unique number for each device. The factory programmed data is fixed and cannot be changed.

The Security Register can be read by clocking in opcode 77H to the device followed by four address bytes (which are comprised of 21 don't care bits plus 11 byte address bits) and a series of don't care clock cycles (24 if using the serial interface and 19 if using the 8-bit interface). The Security Register Read can be terminated by asserting $\overline{CS}$ low to high after the 128-byte security register has been read out. The continuation of clocking past that will result in indeterminate data on the output. See the opcode table on page 13 for this mode.

To program the first 64 bytes of the Security Register, a two step sequence must be used. The first step requires that the user loads the desired data into Buffer 1 by using the Buffer 1 Write operation (opcode 84H – see Buffer Write description). The user should specify the starting buffer address as location zero and should write a full 64 bytes of information into the buffer. Otherwise, the first 64 bytes of the buffer may contain data that was previously stored in the buffer. It is not necessary to fill the remaining 992 bytes (byte locations 64 through 1055) of the buffer with data. After the Buffer 1 Write operation has been completed, the Security Register can be subsequently programmed by reselecting the device and clocking in opcode 9AH into the device followed by four don't care bytes (32 clock cycles if using the serial interface and four clock cycles if using the 8-bit interface). After the final don't care clock cycle has been completed, a low-to-high transition on the $\overline{CS}$ pin will cause the device to initiate an internally self-timed program operation in which the contents of Buffer 1 will be programmed into the Security Register. Only the first 64 bytes of data in Buffer 1 will be programmed into the Security Register; the remaining 992 bytes of the buffer will be ignored. The Security Register program operation should take place in a maximum time of t_P.

Operation Mode Summary

The modes described can be separated into two groups – modes that make use of the Flash memory array (Group A) and modes that do not make use of the Flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Continuous Array Read
3. Main Memory Page to Buffer 1 (or 2) Transfer
4. Main Memory Page to Buffer 1 (or 2) Compare
5. Buffer 1 (or 2) to Main Memory Page Program
6. Sector 0a Erase
7. Sector 0b-63 Erase

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed), then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started, except the first two Group A commands (Memory Array Read Commands).

This gives the DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Pin Descriptions

SERIAL/8-BIT INTERFACE CONTROL (SER/$\overline{\text{BYTE}}$): The DataFlash may be configured to utilize either its serial port or 8-bit port through the use of the serial/8-bit control pin (SER/$\overline{\text{BYTE}}$). When the SER/$\overline{\text{BYTE}}$ pin is held high, the serial port (SI and SO) of the DataFlash will be used for all data transfers, and the 8-bit port (I/O7 - I/O0) will be in a high impedance state. Any data presented on the 8-bit port while SER/$\overline{\text{BYTE}}$ is held high will be ignored. When the SER/$\overline{\text{BYTE}}$ is held low, the 8-bit port will be used for all data transfers, and the SO pin of the serial port will be in a high impedance state. While SER/$\overline{\text{BYTE}}$ is low, any data presented on the SI pin will be ignored. Switching between the serial port and 8-bit port should only be done while the $\overline{\text{CS}}$ pin is high and the device is not busy in an internally self-timed operation.

The SER/$\overline{\text{BYTE}}$ pin is internally pulled high; therefore, if the 8-bit port is never to be used, then connection of the SER/$\overline{\text{BYTE}}$ pin is not necessary. In addition, if the SER/$\overline{\text{BYTE}}$ pin is not connected or if the SER/$\overline{\text{BYTE}}$ pin is always driven high externally, then the 8-bit input/output pins (I/O7-I/O0), the VCCP pin, and the GNDP pin should be treated as "don't connects".

SERIAL INPUT (SI): The SI pin is an input-only pin and is used to shift data serially into the device. The SI pin is used for all data input, including opcodes and address sequences. If the SER/$\overline{\text{BYTE}}$ pin is always driven low, then the SI pin should be a "don't connect".

SERIAL OUTPUT (SO): The SO pin is an output-only pin and is used to shift data serially out from the device. If the SER/$\overline{\text{BYTE}}$ pin is always driven low, then the SO pin should be a "don't connect".

8-BIT INPUT/OUTPUT (I/O7-I/O0): The I/O7-I/O0 pins are bidirectional and used to clock data into and out of the device. The I/O7-I/O0 pins are used for all data input, including opcodes and address sequences. The use of these pins is optional, and the pins should be treated as "don't connects" if the SER/$\overline{\text{BYTE}}$ pin is not connected or if the SER/$\overline{\text{BYTE}}$ pin is always driven high externally.

SERIAL CLOCK/CLOCK (SCK/CLK): The SCK and CLK pins are input-only pins and are used to control the flow of data to and from the DataFlash. The SCK and CLK pins are used for serial and 8-bit interface respectively. Data is always clocked into the device on the rising edge of SCK/CLK and clocked out of the device on the falling edge of SCK/CLK.

CHIP SELECT ($\overline{\text{CS}}$): The DataFlash is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted on the input pins (SI or I/O7-I/O0), and the output pins (SO or I/O7-I/O0) will remain in a high impedance state. A high-to-low transition on the $\overline{\text{CS}}$ pin is required to start an operation, and a low-to-high transition on the $\overline{\text{CS}}$ pin is required to end an operation.

HARDWARE PAGE WRITE PROTECT: If the $\overline{\text{WP}}$ pin is held low, the first 256 pages (sectors 0 and 1) of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program

commands previously mentioned. If this pin and feature are not utilized it is recommended that the $\overline{WP}$ pin be driven high externally.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature are not utilized it is recommended that the $\overline{RESET}$ pin be driven high externally.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming/erase operations, compare operations, and page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

8-BIT PORT SUPPLY VOLTAGE (VCCP AND GNDP): The VCCP and GNDP pins are used to supply power for the 8-bit input/output pins (I/O7-I/O0). The VCCP and GNDP pins need to be used if the 8-bit port is to be utilized; however, these pins should be treated as “don’t connects” if the SER/$\overline{BYTE}$ pin is not connected or if the SER/$\overline{BYTE}$ pin is always driven high externally.

Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to Mode 3. In addition, the output pins (SO or I/O7 - I/O0) will be in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state. After power is applied and V_{CC} is at the minimum datasheet value, the system should wait 20 ms before an operational mode is started.

System Considerations

The RapidS serial interface is controlled by the serial clock SCK, serial input SI and chip select $\overline{CS}$ pins. The sequential 8-bit Rapid8 is controlled by the clock CLK, 8 I/Os and chip select $\overline{CS}$ pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash occur during the programming and erase operation. The regulator needs to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

Table 1. Read Commands

Command	Serial/8-bit	Opcode
Main Memory Page Read	Both	D2h
Continuous Array Read	Both	E8h
Buffer 1 Read	Serial	D4h
Buffer 2 Read	Serial	D6h
Buffer 1 Read	8-bit	54h
Buffer 2 Read	8-bit	56h

Table 2. Program and Erase Commands

Command	Serial/8-bit	Opcode
Buffer 1 Write	Both	84h
Buffer 2 Write	Both	87h
Buffer 1 to Main Memory Page Program	Both	88h
Buffer 1 to Main Memory Page Program, Fast Program	Both	98h
Buffer 2 to Main Memory Page Program	Both	89h
Buffer 2 to Main Memory Page Program, Fast Program	Both	99h
Sector 0a Erase	Both	50h
Sector 0b-63 Erase	Both	7Ch

Table 3. Additional Commands

Command	Serial/8-bit	Opcode
Main Memory Page to Buffer 1 Transfer	Both	53h
Main Memory Page to Buffer 2 Transfer	Both	55h
Main Memory Page to Buffer 1 Compare	Both	60h
Main Memory Page to Buffer 2 Compare	Both	61h
Status Register Read	Both	D7h
Manufacturer and Device ID Read	Serial	9Fh
Security Register Program(1)	Both	9Ah
Security Register Read	Both	77h

Note: 1. The Security Register Program command utilizes data stored in Buffer 1. Therefore, this command must be used in conjunction with the Buffer 1 write command. See the Security Register description for details.

Table 4. Detailed Bit-level Addressing Sequence

Opcode	Opcode	Address Byte								Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes*
									PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
50h	0 1 0 1 0 0 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
53h	0 1 0 1 0 0 1 1	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
54h	0 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	2*
55h	0 1 0 1 0 1 0 1	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
56h	0 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	2*
60h	0 1 1 0 0 0 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
61h	0 1 1 0 0 0 0 1	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
77h	0 1 1 1 0 1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	3 or 19*
7Ch	0 1 1 1 1 1 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
84h	1 0 0 0 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	N/A
87h	1 0 0 0 0 1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	N/A
88h	1 0 0 0 1 0 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
89h	1 0 0 0 1 0 0 1	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
98h	1 0 0 1 1 0 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
99h	1 0 0 1 1 0 0 1	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
9Ah	1 0 0 1 1 0 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
9Fh	1 0 0 1 1 1 1 1	N/A								N/A								N/A								N/A								N/A
D2h	1 1 0 1 0 0 1 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	B	3 or 19*
D4h	1 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	1
D6h	1 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	B	1
D7h	1 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A								1/0 or 1*
E8h	1 1 1 0 1 0 0 0	x	x	x	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	B	3 or 19*

Notes: P = Page Address Bit
B = Byte/Buffer Address Bit
x = Don't Care
*The number with (*) is for 8-bit interface.

Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45CS1282
Operating Temperature (Case)	Com.	0° C to 70° C
V_{CC} Power Supply(1)		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified datasheet value, the system should wait 20 ms before an operational mode is started.

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		15	50	µA
I_{CC1}(1)	Active Current, Read Operation, Serial Interface	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	20	mA
I_{CC2}(2)	Active Current, Read Operation, 8-bit Interface	f = 10 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		12	20	mA
I_{CC3}	Active Current, Program Operation, Page Program	V_{CC} = 3.6V			50	mA
I_{CC4}	Active Current, Program Operation, Fast Page Program	V_{CC} = 3.6V			65	mA
I_{CC5}	Active Current, Sector Erase Operation	V_{CC} = 3.6V			50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

Notes: 1. I_{CC1} during a buffer read is 25 mA maximum.
2. I_{CC2} during a buffer read is 25 mA maximum.

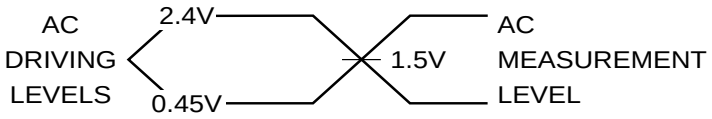
AC Characteristics – RapidS Serial Interface

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			50	MHz
f_{CAR}	SCK Frequency for Continuous Array Read			40	MHz
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			150	ns
t_{SU}	Data In Setup Time	5			ns
t_{H}	Data In Hold Time	7			ns
t_{HO}	Output Hold Time	2			ns
t_{DIS}	Output Disable Time			10	ns
t_{V}	Output Valid			10	ns
t_{XFR}	Page to Buffer Transfer/Compare Time			500	µs
t_{P}	Page Programming Time		50		ms
t_{FP}	Fast Page Programming Time		15		ms
t_{SE0a}	Sector 0a Erase Time		75	200	ms
$t_{SE0b-63}$	Sector 0b-63 Erase Time		2	4	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

AC Characteristics – Rapid8 8-bit Interface

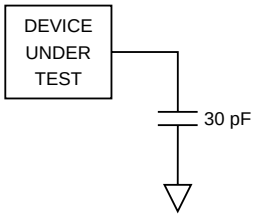
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK1}	CLK Frequency			20	MHz
f_{CAR1}	CLK Frequency for Continuous Array Read			20	MHz
t_{WH}	CLK High Time	16			ns
t_{WL}	CLK Low Time	16			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			150	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	10			ns
t_{HO}	Output Hold Time	3			ns
t_{DIS}	Output Disable Time			15	ns
t_V	Output Valid			15	ns
t_{XFR}	Page to Buffer Transfer/Compare Time			500	µs
t_P	Page Programming Time		50		ms
t_{FP}	Fast Page Programming Time		15		ms
t_{SE0a}	Sector 0a Erase Time		75	200	ms
$t_{SE0b-63}$	Sector 0b-63 Erase Time		2	4	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 2 ns (10% to 90%)

Output Test Load

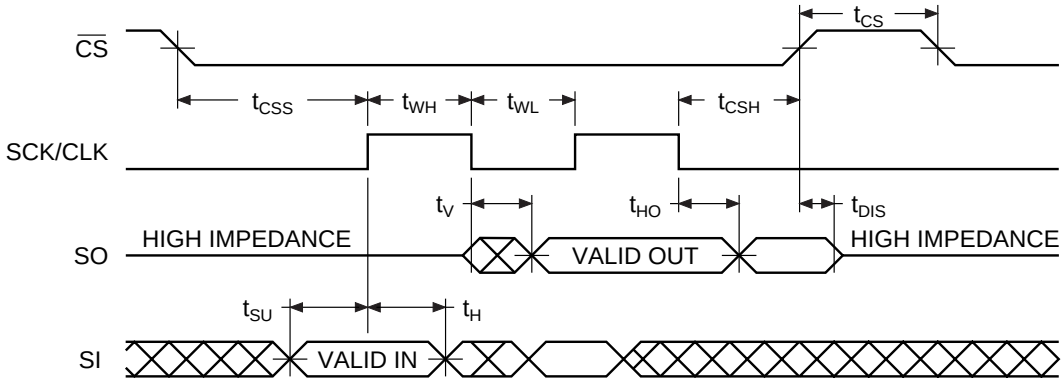


AC Waveforms

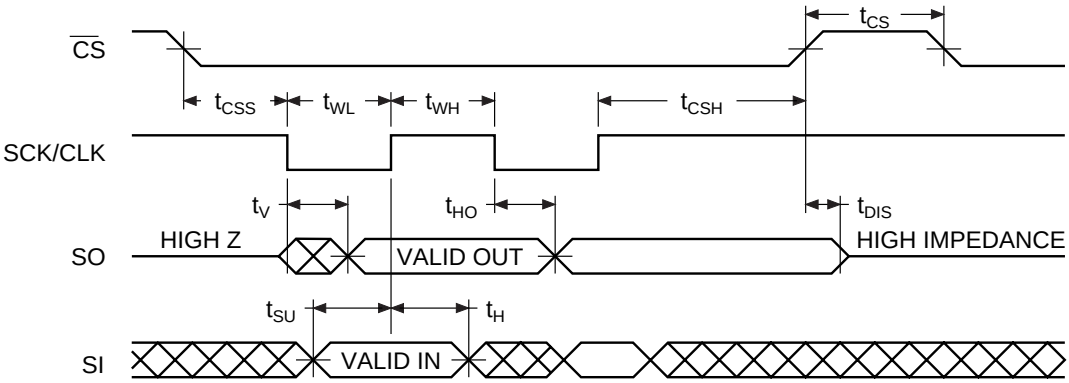
Six different timing waveforms are shown below. Waveform 1 shows the SCK/CLK signal being low when $\overline{CS}$ makes a high-to-low transition, and waveform 2 shows the SCK/CLK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK/CLK signal is still low (SCK/CLK low time is specified as t_{WL}). Timing waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 33 MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and waveform 4 illustrate general timing diagram for RapidS serial interface. These are similar to waveform 1 and waveform 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 50 MHz) of the RapidS serial case. Waveform 5 and waveform 6 are for 8-bit Rapid8 interface over the full frequency range of operation (maximum frequency = 20 MHz).

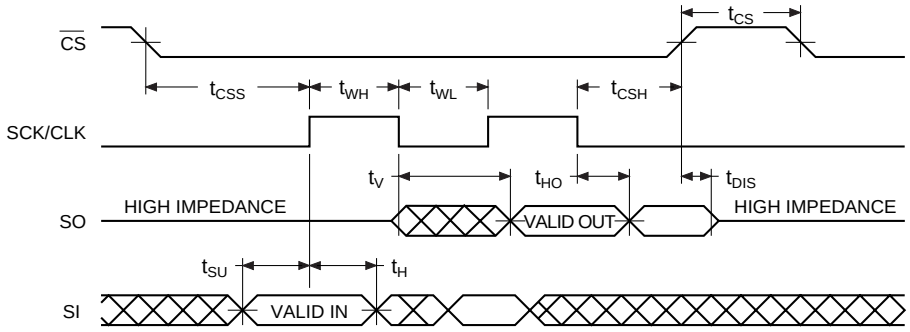
Waveform 1 – SPI Mode 0 Compatible (for Frequencies up to 33 MHz)



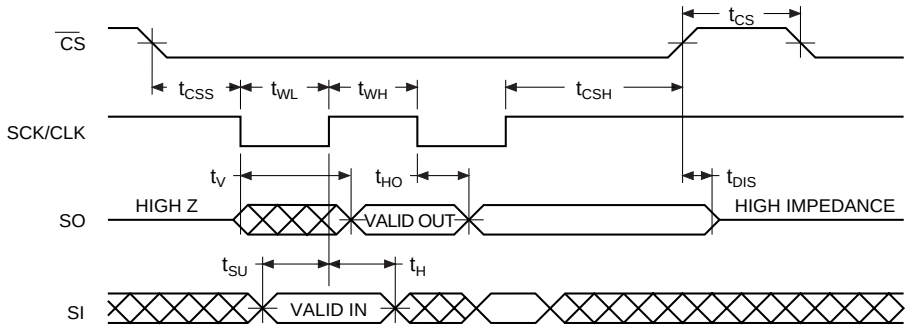
Waveform 2 – SPI Mode 3 Compatible (for Frequencies up to 33 MHz)



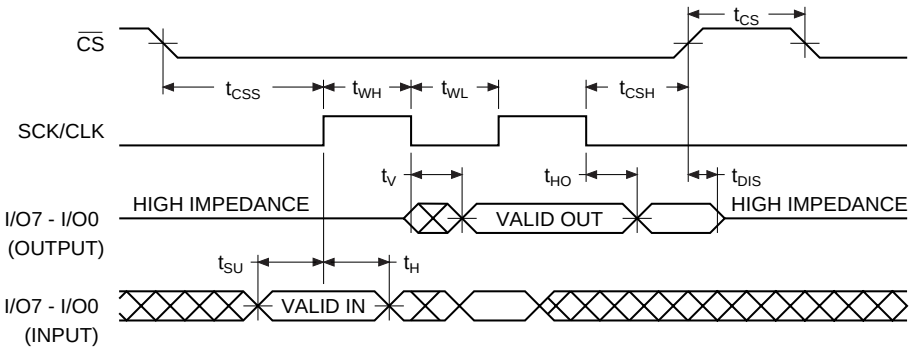
Waveform 3 – RapidS Mode 0 (for all Frequencies)



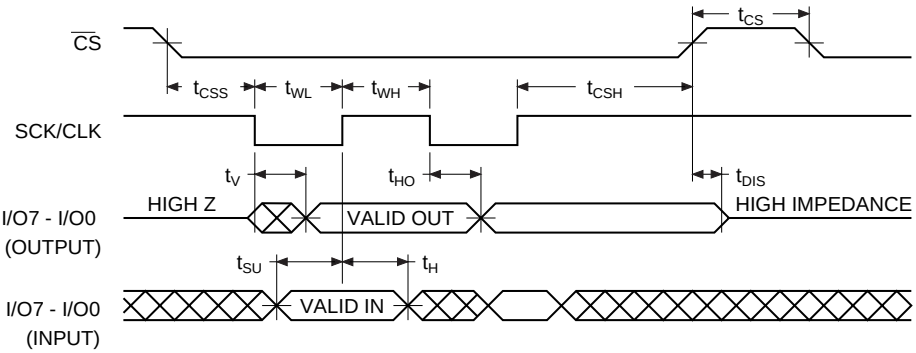
Waveform 4 – RapidS Mode 3 (for all Frequencies)



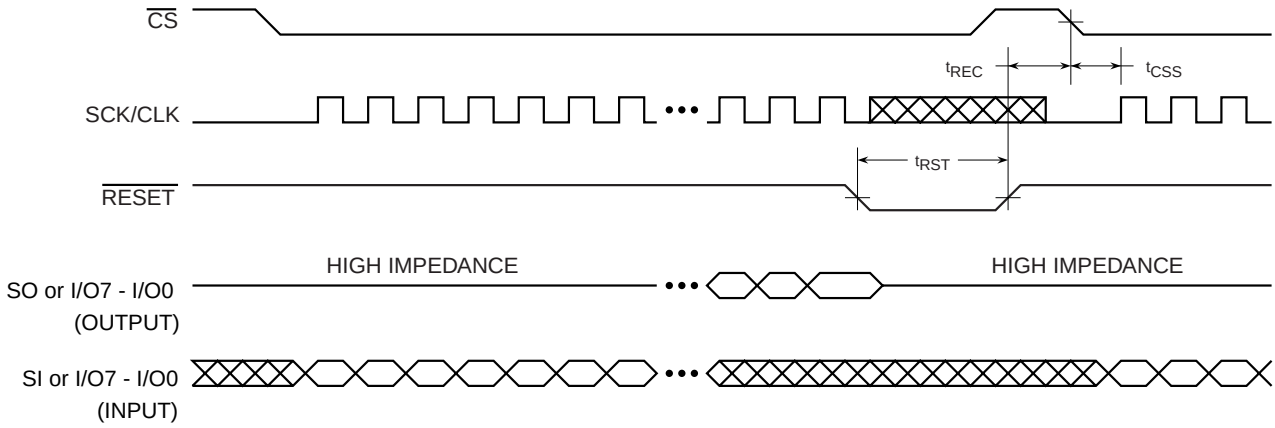
Waveform 5 – Rapid8 Mode 0 (F_{MAX} = 20 MHz)



Waveform 6 – Rapid8 Mode 3 (F_{MAX} = 20 MHz)

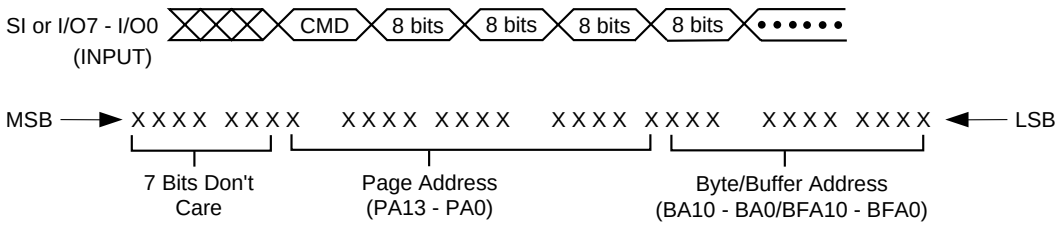


Reset Timing



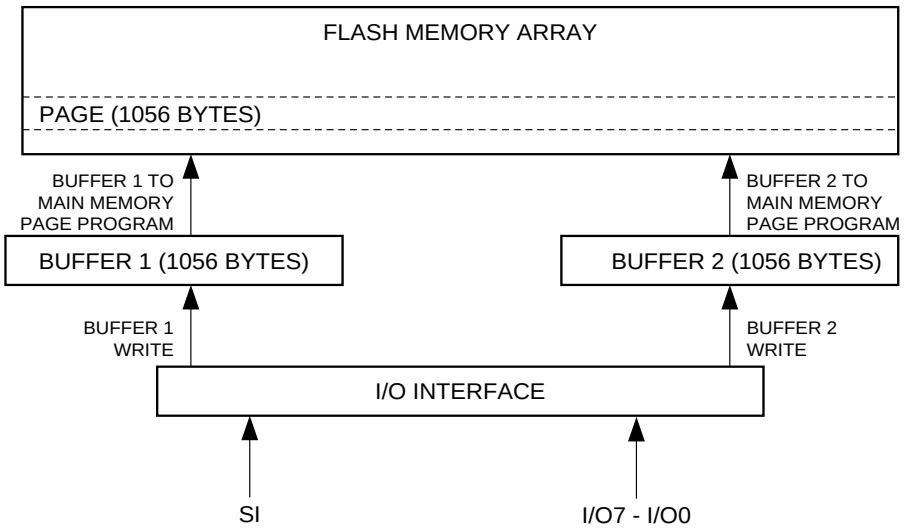
Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

Command Sequence for Read/Write Operations (Except Status Register Read, Manufacturer and Device ID Read)

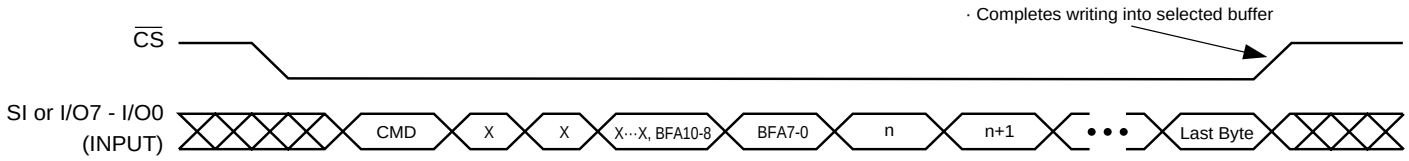


Write Operations

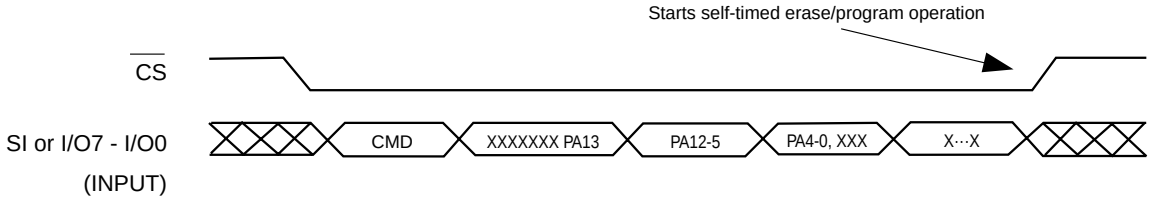
The following block diagram and waveforms illustrate the various write sequences available.



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

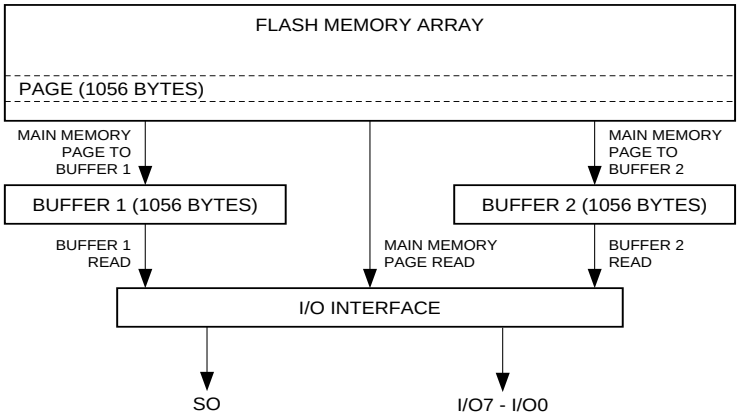


Each transition represents 8 bits 

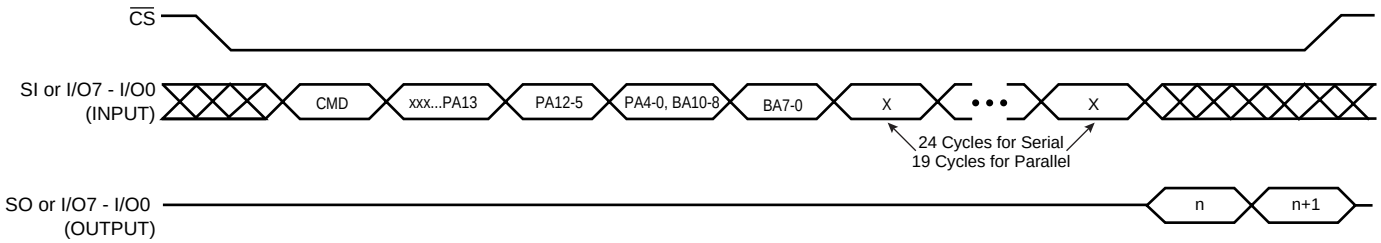
n = 1st byte
n+1 = 2nd byte

Read Operations

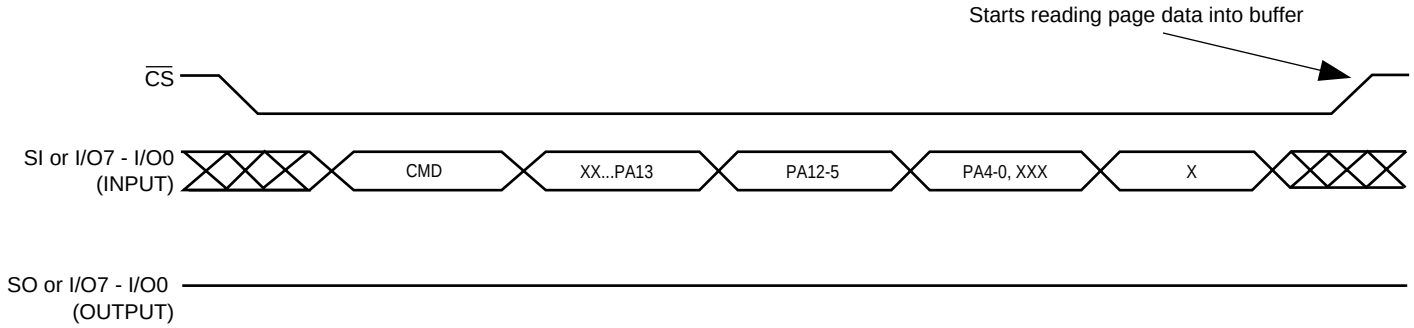
The following block diagram and waveforms illustrate the various read sequences available.



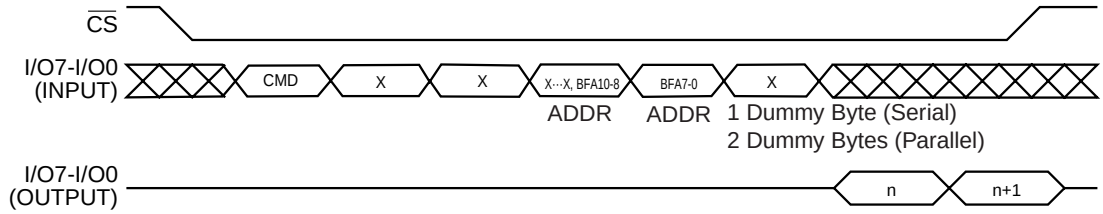
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read

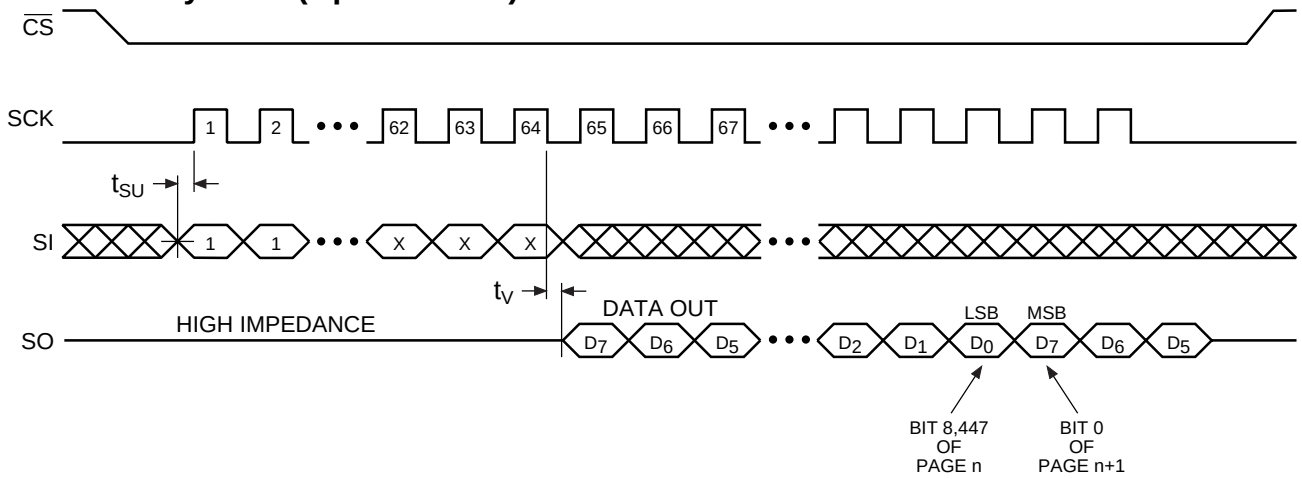


Each transition represents 8 bits

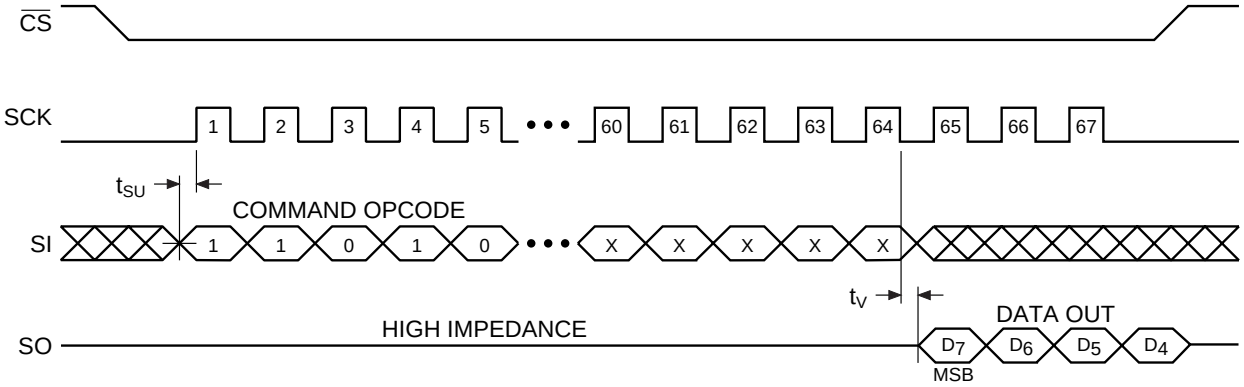
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-level Read Timing – RapidS Serial Interface Mode 0

Continuous Array Read (Opcode: E8H)

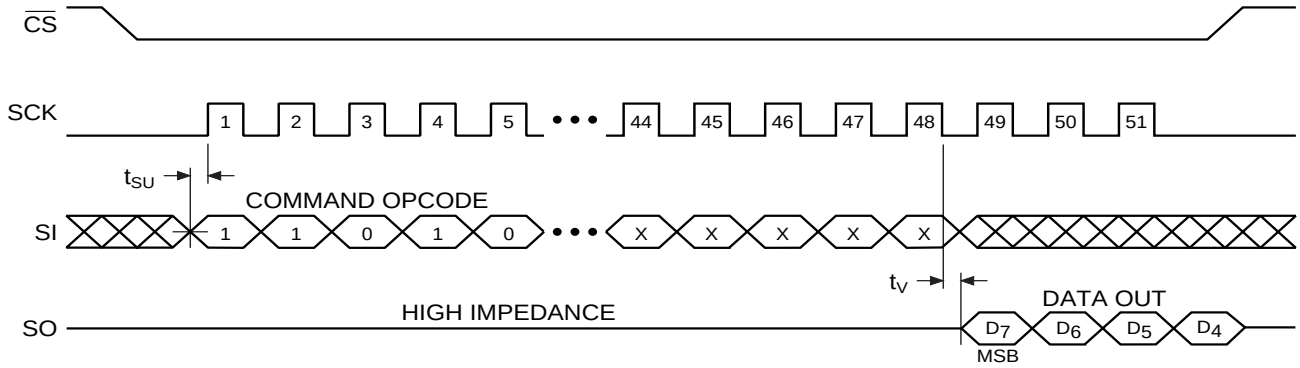


Main Memory Page Read (Opcode: D2H)

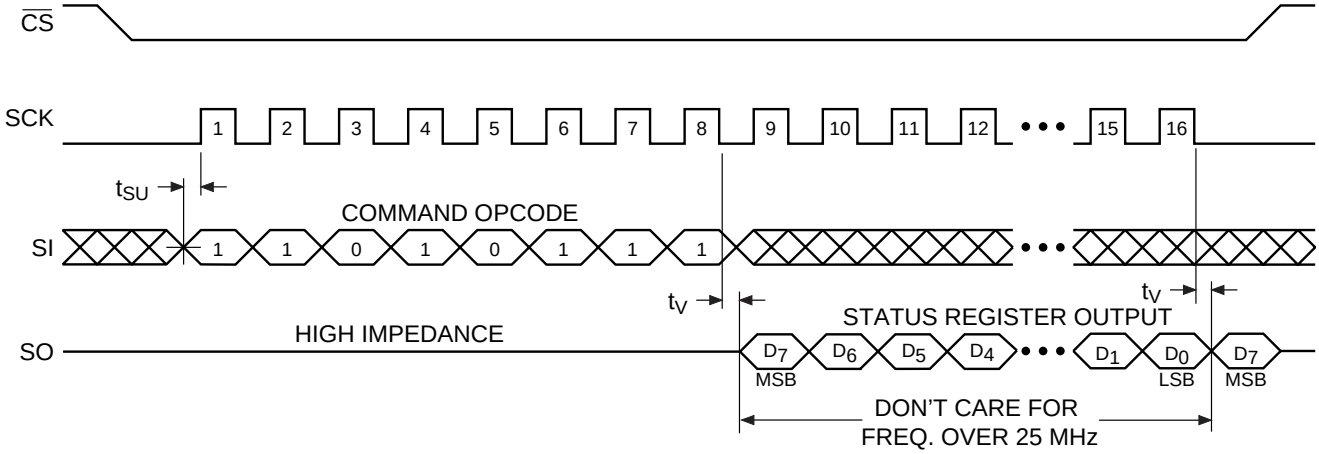


Detailed Bit-level Read Timing – RapidS Serial Interface Mode 0 (Continued)

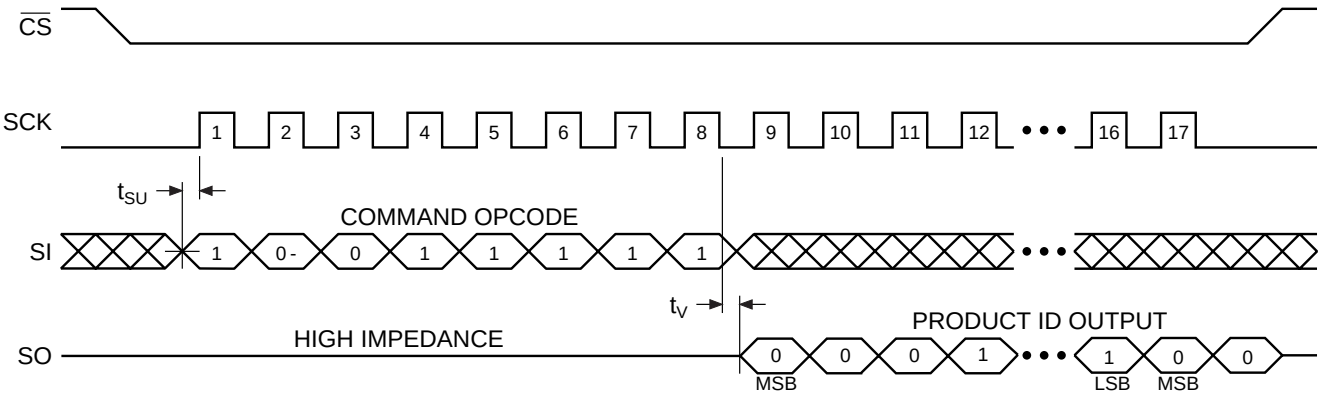
Buffer Read (Opcode: D4H or D6H)



Status Register Read (Opcode: D7H)

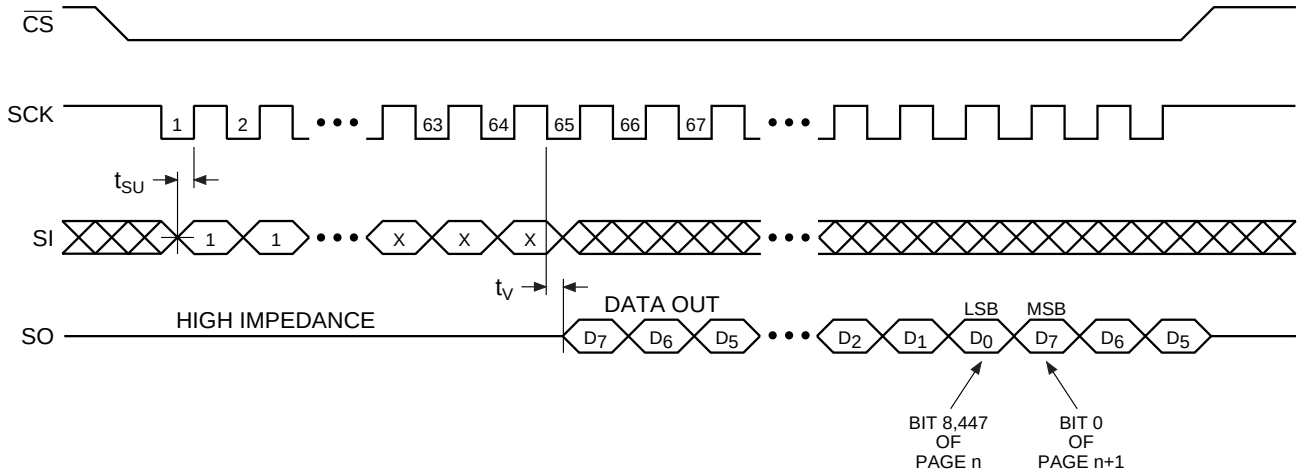


Manufacturer and Device ID Read (Opcode: 9FH)

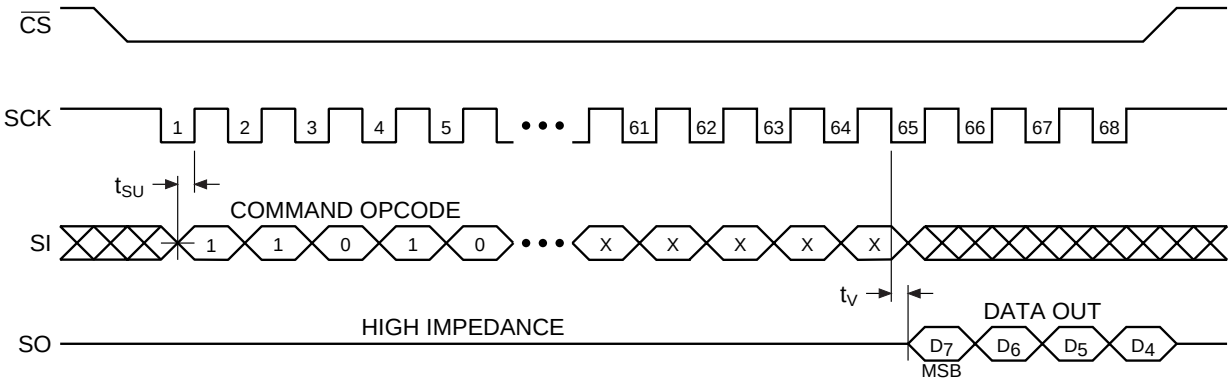


Detailed Bit-level Read Timing – RapidS Serial Interface Mode 3

Continuous Array Read (Opcode: E8H)

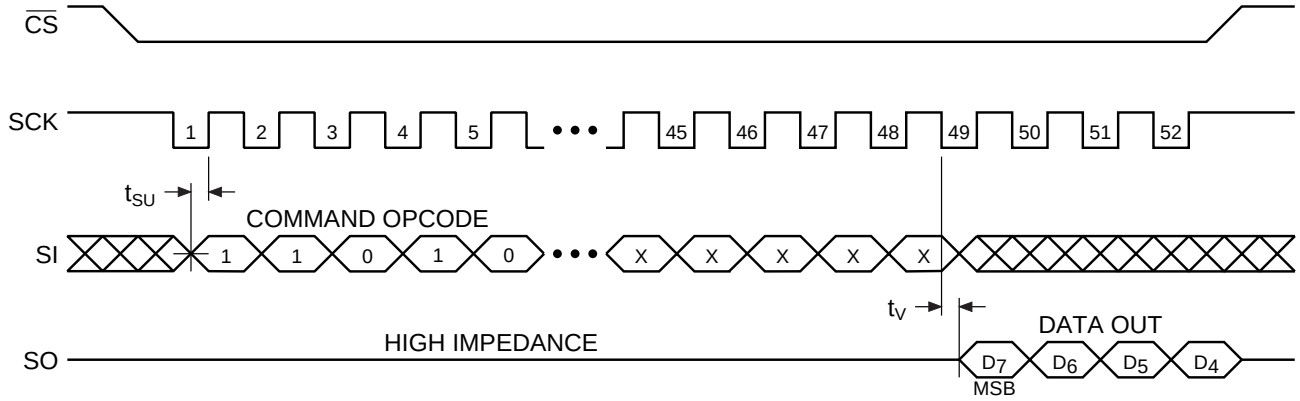


Main Memory Page Read (Opcode: D2H)

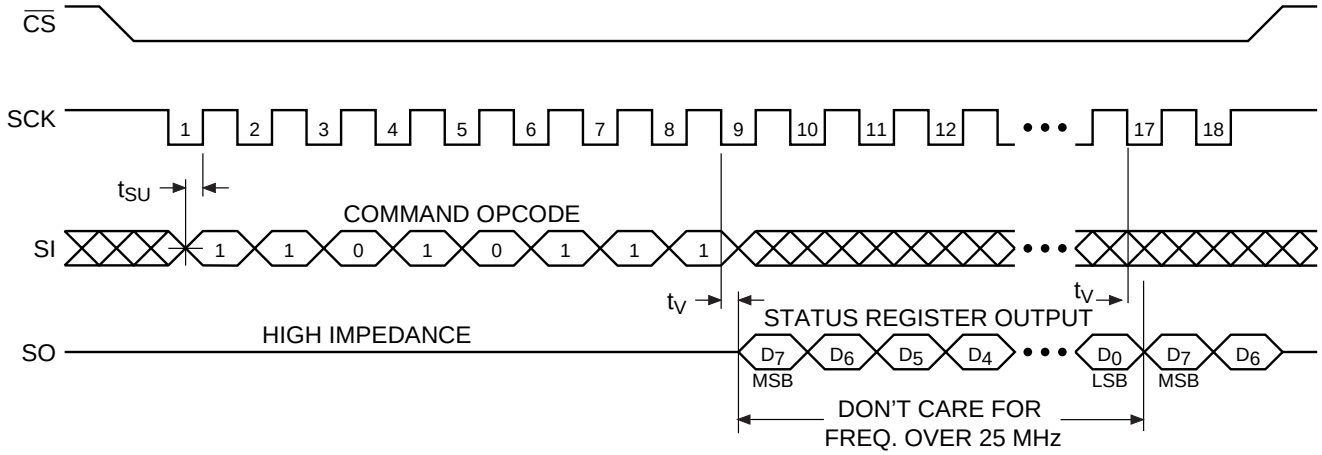


Detailed Bit-level Read Timing – RapidS Serial Interface Mode 3 (Continued)

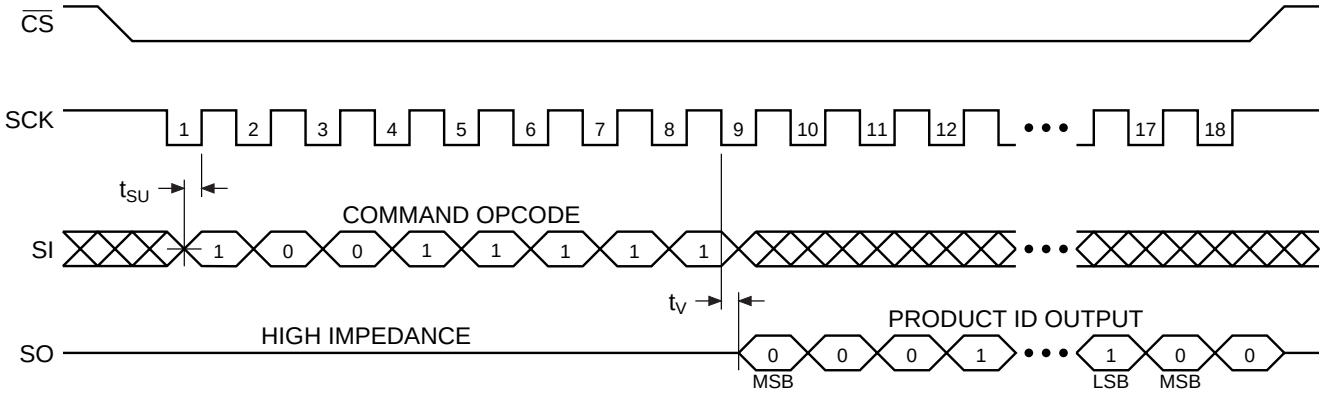
Buffer Read (Opcode: D4H or D6H)



Status Register Read (Opcode: D7H)

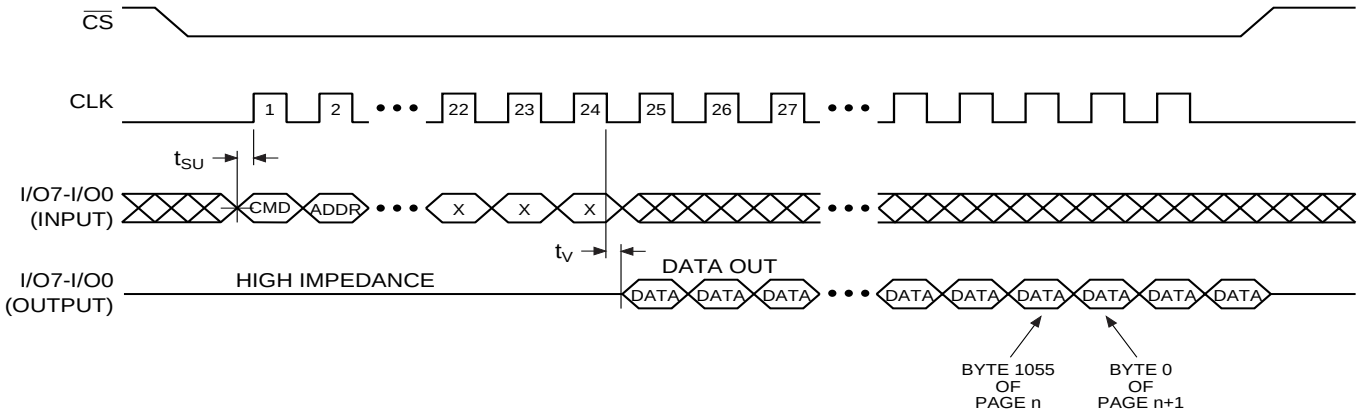


Manufacturer and Device ID Read (Opcode: 9FH)

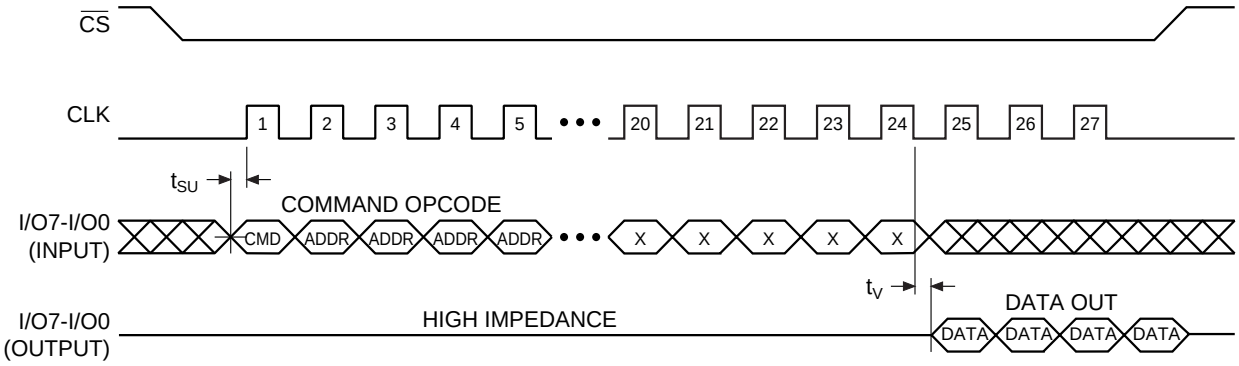


Detailed 8-bit Read Timing – Rapid8 Mode 0

Continuous Array Read (Opcode: E8H)

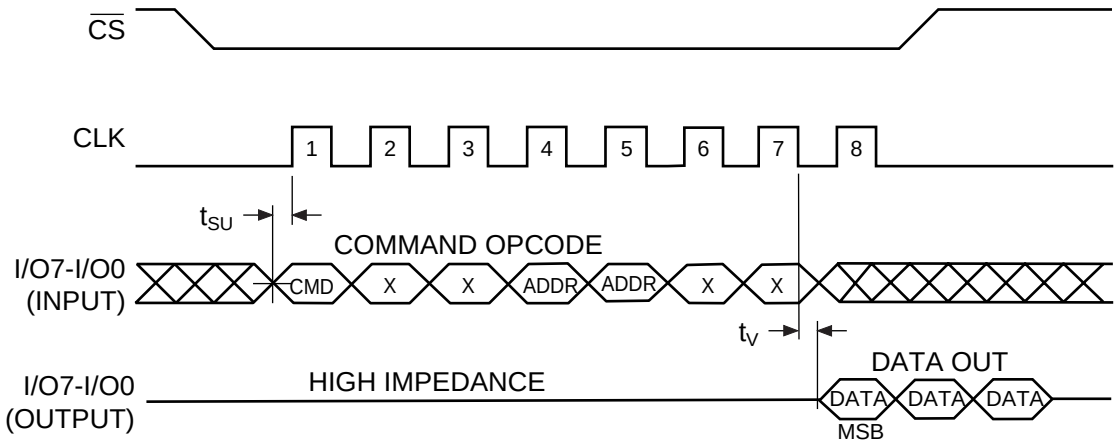


Main Memory Page Read (Opcode: D2H)

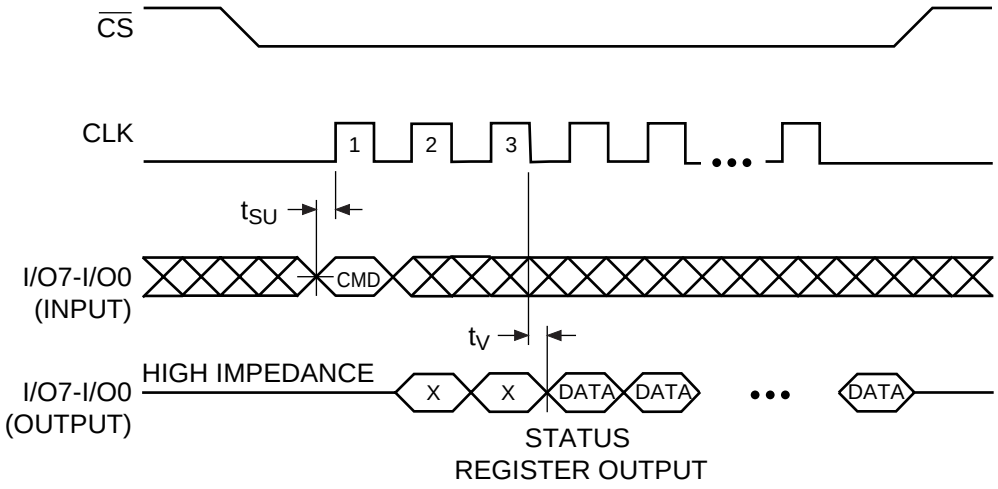


Detailed 8-bit Timing – Rapid8 Mode 0 (Continued)

Buffer Read (Opcode: 54H or 56H)

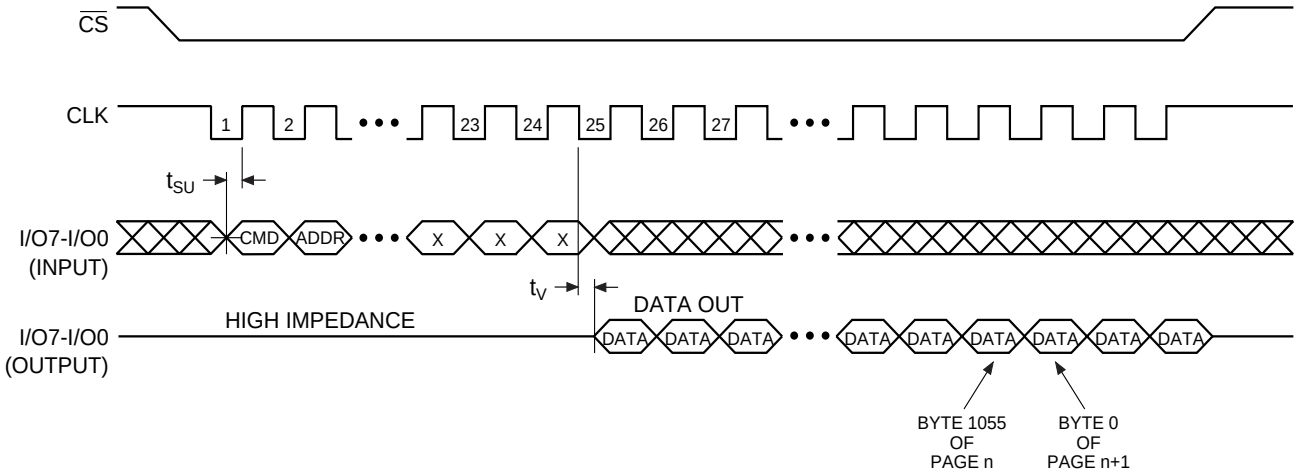


Status Register Read (Opcode: D7H)

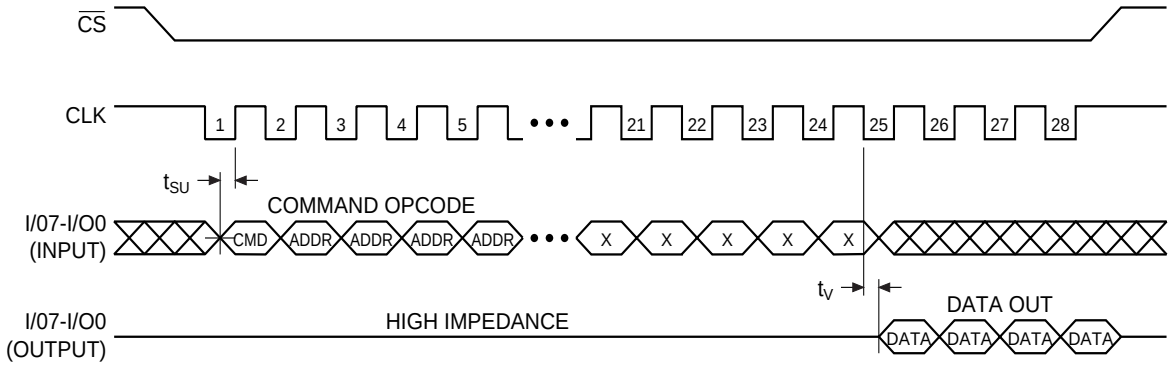


Detailed 8-bit Read Timing – Rapid8 Mode 3

Continuous Array Read (Opcode: E8H)

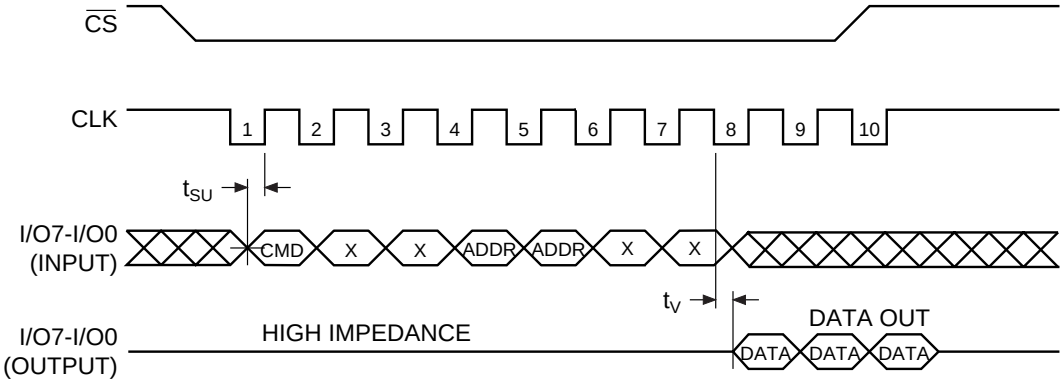


Main Memory Page Read (Opcode: D2H)

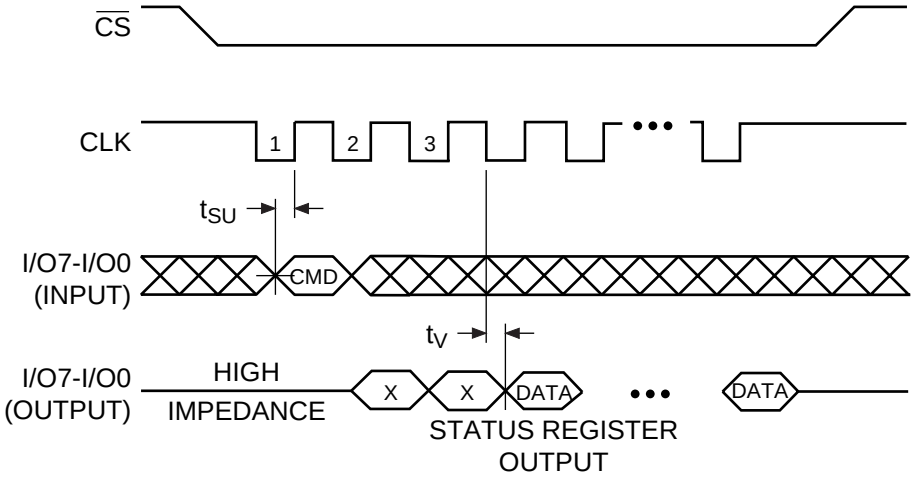


Detailed 8-bit Read Timing – Rapid8 Mode 3 (Continued)

Buffer Read (Opcode: 54H or 56H)



Status Register Read (Opcode: D7H)



Ordering Information

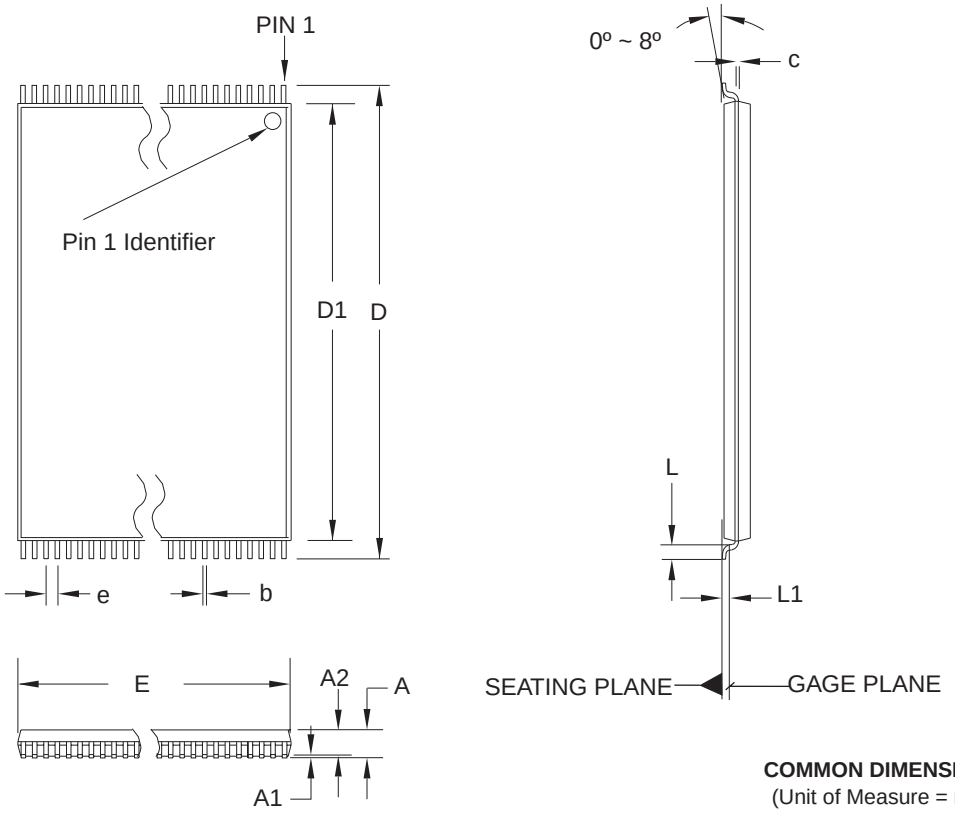
f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
50(1)	20(1)	0.05	AT45CS1282-TC	40T	Commercial (0° C to 70° C)
50(1)	20(1)	0.05	AT45CS1282-CC	44C2	Commercial (0° C to 70° C)

Note: 1. RapidS Serial Interface.

Package Type	
40T	40-lead, (10 x 20 mm) Plastic Thin Small Outline Package, Type I (TSOP)
44C2	44-ball, (8 x 12 mm) Plastic Chip-size Ball Grid Array Package (CBGA)

Packaging Information

40T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

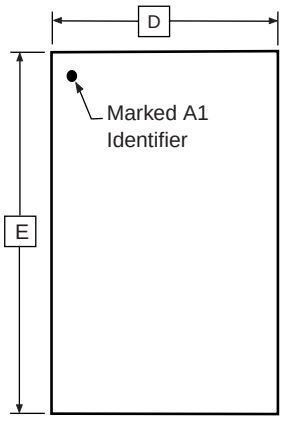
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	9.90	10.00	10.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation CD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

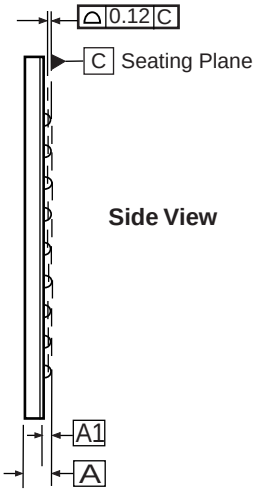
10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40T**, 40-lead (10 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	40T	B

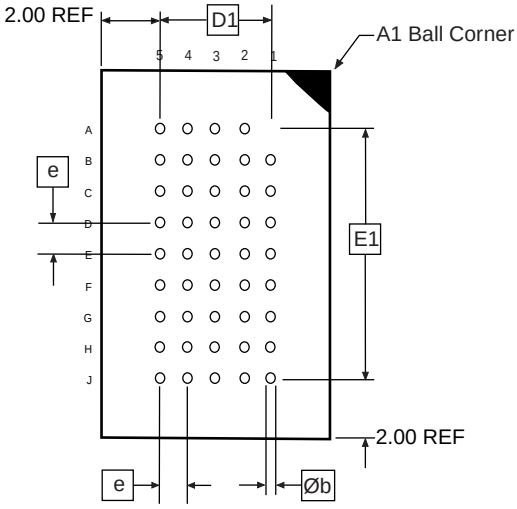
44C2 – CBGA



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.25	–	–	
D	7.90	8.00	8.10	
D1		4.00 TYP		
E	11.90	12.00	12.10	
E1		8.00 TYP		
e		1.00 TYP		
øb		0.40 TYP		

06/10/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44C2**, 44-ball (5 x 9 Array), 8 x 12 x 1.2 mm Body, 0.4 mm Ball Plastic Chip-scale Ball Grid Array Package (CBGA)	44C2	A

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