MCP6L01/1R/1U/2/4

1 MHz, 85 µA Op Amps

Features

- Available in SC70 and SOT-23 Packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I_Q = 85 µA/Amplifier (typical)
- Extended Temperature Range: -40°C to +125°C
- Available in Single, Dual and Quad Packages

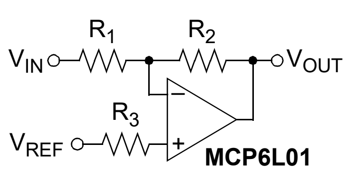
Typical Applications

- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Model
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



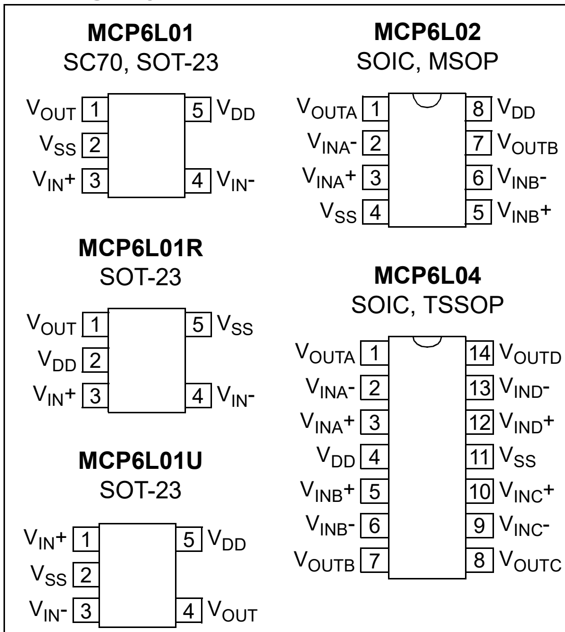
Inverting Amplifier

Description

The Microchip Technology Inc. MCP6L01/1R/1U/2/4 family of operational amplifiers (op amps) supports general purpose applications. The combination of rail-to-rail input and output, low quiescent current and bandwidth fit into many applications.

This family has a 1 MHz Gain Bandwidth Product (GBWP) and a low 85 µA per amplifier quiescent current. These op amps operate on supply voltages between 1.8V and 6.0V, with rail-to-rail input and output swing. They are available in the extended temperature range.

Package Types



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins ....±2 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† .... V_{SS} – 1.0V to V_{DD} + 1.0V
All Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage .... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .... Continuous
Current at Output and Supply Pins ....±30 mA
Storage Temperature ....-65°C to +150°C
Max. Junction Temperature ....+150°C
ESD Protection on All Pins (HBM, MM) ....≥ 4 kV, 200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, $V_{CM} = V_{SS}$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L (refer to Figure 1-1).

Parameters	Sym	Min(1)	Typ	Max(1)	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-5	±1	+5	mV	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	T_A = -40°C to+125°C
Power Supply Rejection Ratio	PSRR	—	83	—	dB	
Input Current and Impedance						
Input Bias Current	I_B	—	2	—	pA	
Across Temperature	I_B	—	80	—	pA	T_A = +85°C
Across Temperature	I_B	—	2,000	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common-Mode Input Impedance	Z_{CM}	—	10^{13}‖5	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖2	—	Ω‖pF	
Common-Mode						
Common-Mode Input Voltage Range	V_{CMR}	-0.3	—	5.3	V	
Common-Mode Rejection Ratio	CMRR	—	78	—	dB	V_{CM} = -0.3V to 5.3V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	—	105	—	dB	V_{OUT} = 0.2V to 4.8V
Output						
Maximum Output Voltage Swing	V_{OL}	—	—	0.035	V	G = +2, 0.5V input overdrive
	V_{OH}	4.965	—	—	V	G = +2, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±20	—	mA	
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	
Quiescent Current per Amplifier	I_Q	30	85	170	µA	I_O = 0

Note 1: For design guidance only; not tested.

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TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{SS}, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	24	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 1 kHz

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +6.0V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	(Note 1)
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8-Lead SOIC (150 mil)	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14-Lead SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: Operation must not cause T_J to exceed maximum junction temperature specification (+150°C).

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1.3 Test Circuit

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common-mode voltage ((V_P + V_M)/2) and that V_{OST} includes V_{OS}, plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential-Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common-Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

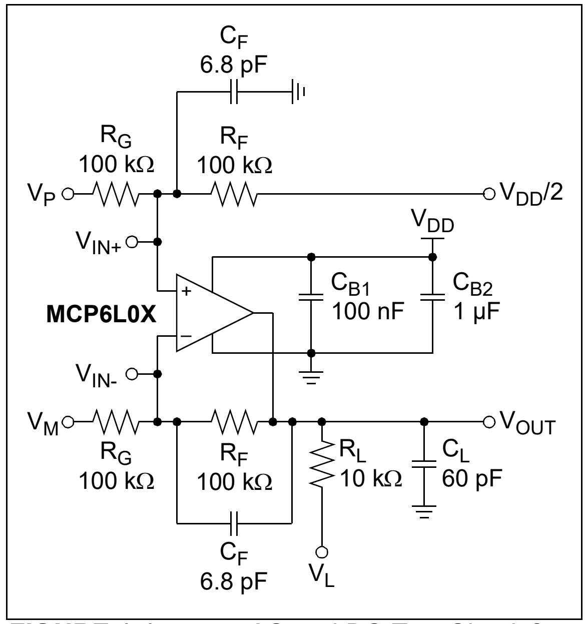

FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, $V_{CM} = V_{SS}$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

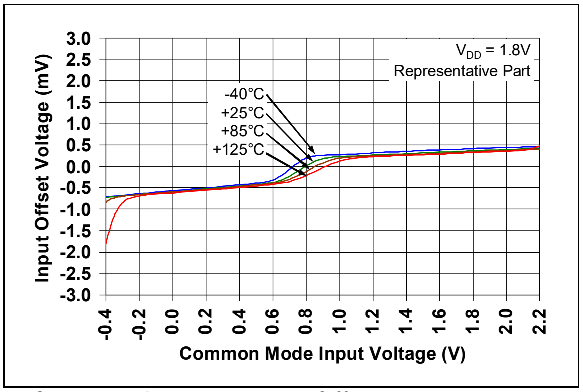

FIGURE 2-1: *Input Offset Voltage vs. Common-Mode Input Voltage at V_{DD} = 1.8V.*

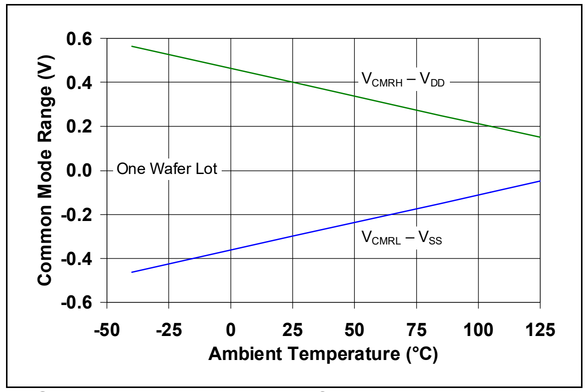

FIGURE 2-4: *Input Common-Mode Range Voltage vs. Ambient Temperature.*

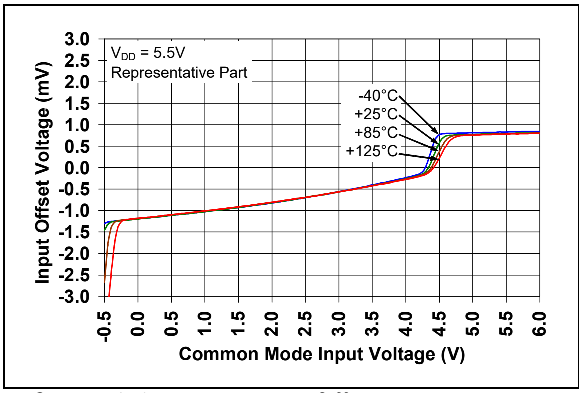

FIGURE 2-2: *Input Offset Voltage vs. Common-Mode Input Voltage at V_{DD} = 5.5V.*

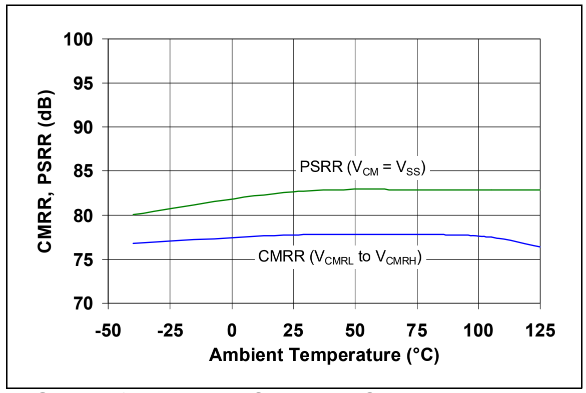

FIGURE 2-5: *CMRR, PSRR vs. Ambient Temperature.*

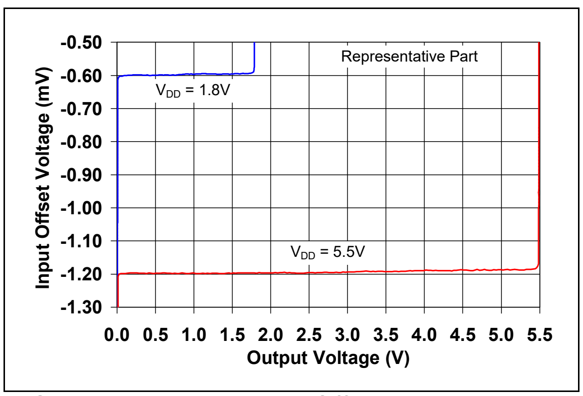

FIGURE 2-3: *Input Offset Voltage vs. Output Voltage.*

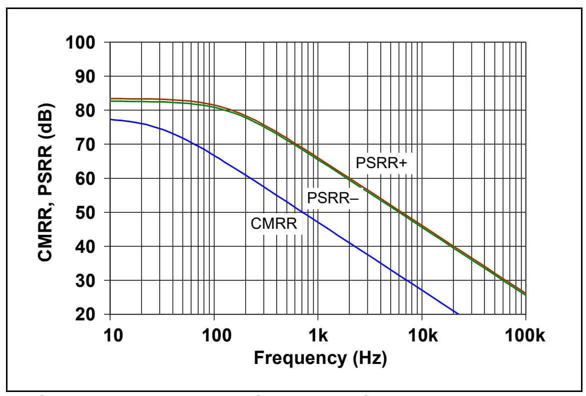

FIGURE 2-6: *CMRR, PSRR vs. Frequency.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, V_{CM} = V_{SS}, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

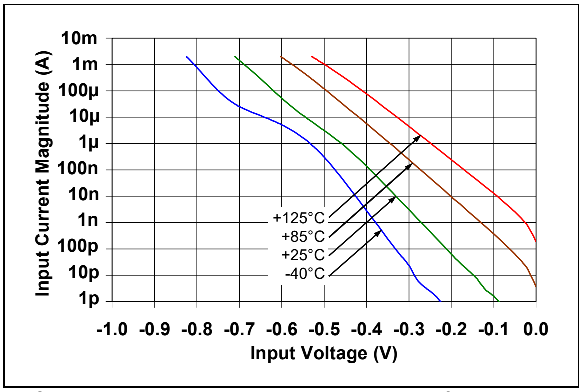

FIGURE 2-7: *Measured Input Current vs. Input Voltage (below V_{SS}).*

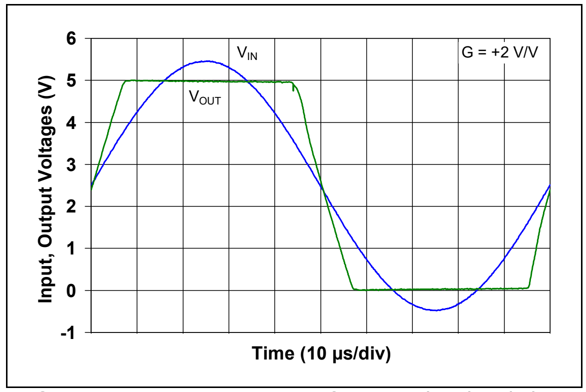

FIGURE 2-10: *The MCP6L01/1R/1U/2/4 Show No Phase Reversal.*

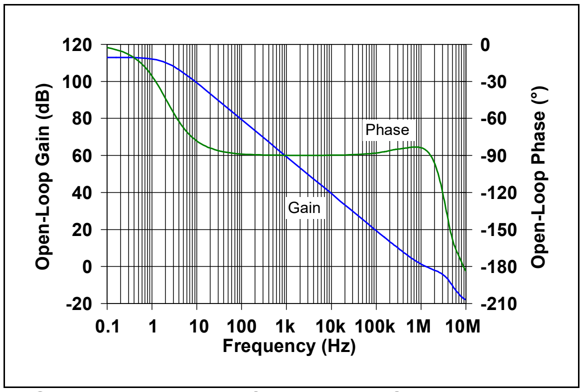

FIGURE 2-8: *Open-Loop Gain, Phase vs. Frequency.*

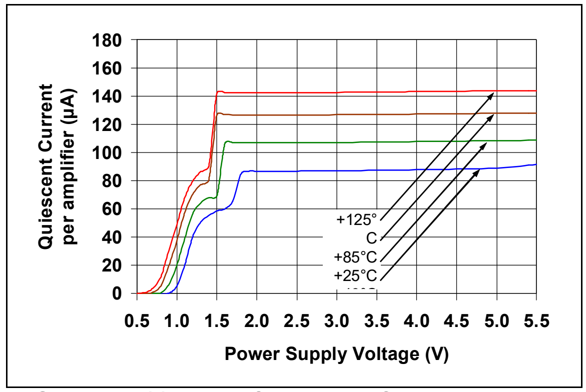

FIGURE 2-11: *Quiescent Current vs. Power Supply Voltage.*

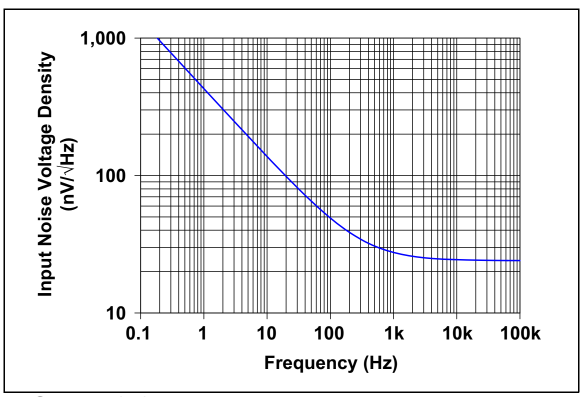

FIGURE 2-9: *Input Noise Voltage Density vs. Frequency.*

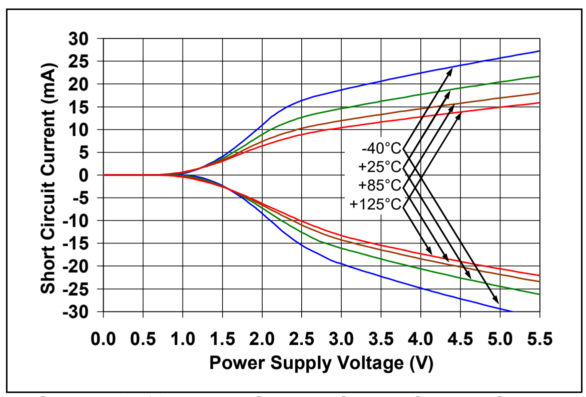

FIGURE 2-12: *Output Short-Circuit Current vs. Power Supply Voltage.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, V_{CM} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

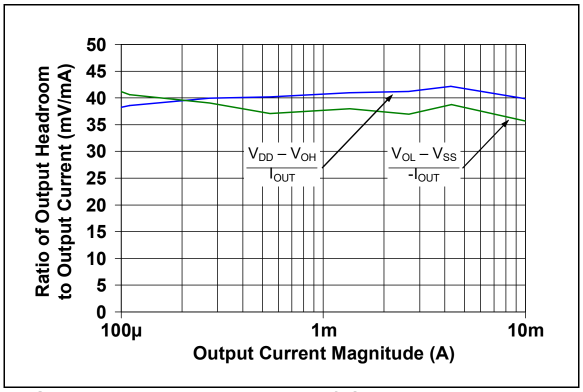

FIGURE 2-13: Ratio of Output Voltage Headroom to Output Current vs. Output Current.

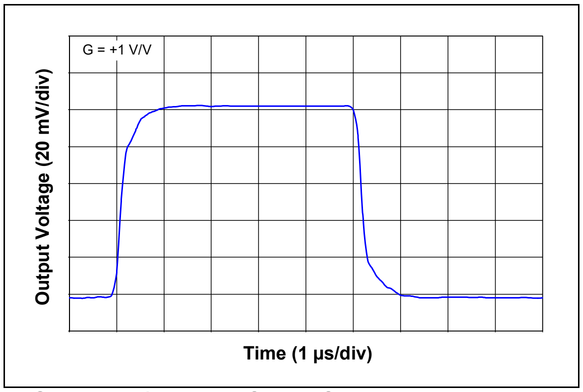

FIGURE 2-14: Small Signal, Noninverting Pulse Response.

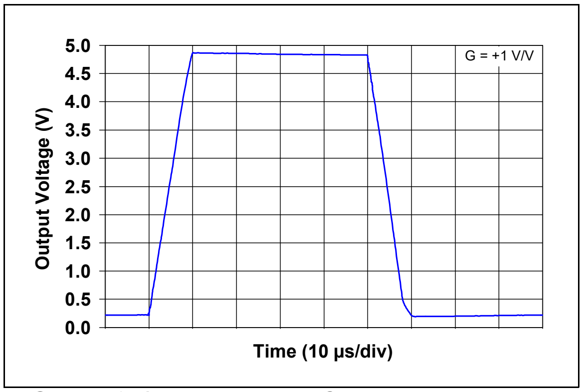

FIGURE 2-15: Large Signal, Noninverting Pulse Response.

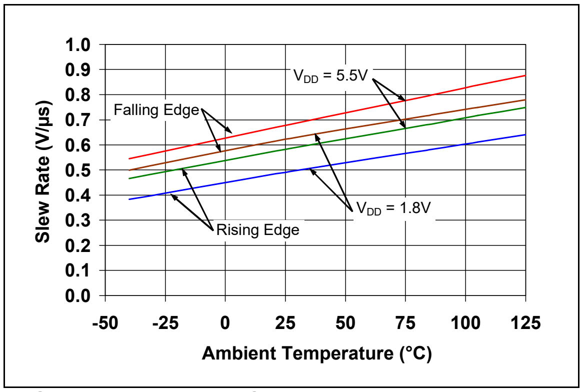

FIGURE 2-16: Slew Rate vs. Ambient Temperature.

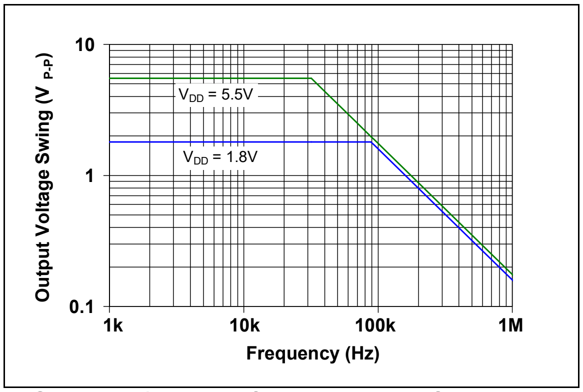

FIGURE 2-17: Output Voltage Swing vs. Frequency.

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6L01	MCP6L01R	MCP6L01U	MCP6L02	MCP6L04	Symbol	Description
5-Lead SC70, SOT-23	5-Lead SOT-23	5-Lead SOT-23	8-Lead SOIC, MSOP	14-Lead SOIC, TSSOP		
1	1	4	1	1	V_{OUT}, V_{OUTA}	Output (Op Amp A)
4	4	3	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (Op Amp A)
3	3	1	3	3	$V_{IN}+$, $V_{INA}+$	Noninverting Input (Op Amp A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	$V_{INB}+$	Noninverting Input (Op Amp B)
—	—	—	6	6	$V_{INB}-$	Inverting Input (Op Amp B)
—	—	—	7	7	V_{OUTB}	Output (Op Amp B)
—	—	—	—	8	V_{OUTC}	Output (Op Amp C)
—	—	—	—	9	$V_{INC}-$	Inverting Input (Op Amp C)
—	—	—	—	10	$V_{INC}+$	Noninverting Input (Op Amp C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Noninverting Input (Op Amp D)
—	—	—	—	13	$V_{IND}-$	Inverting Input (Op Amp D)
—	—	—	—	14	V_{OUTD}	Output (Op Amp D)
—	—	—	—	—	NC	No Internal Connection

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The noninverting and inverting inputs ($V_{IN}+$, $V_{IN}-$, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

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4.0 APPLICATION INFORMATION

The MCP6L01/1R/1U/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process. It is designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6L01/1R/1U/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

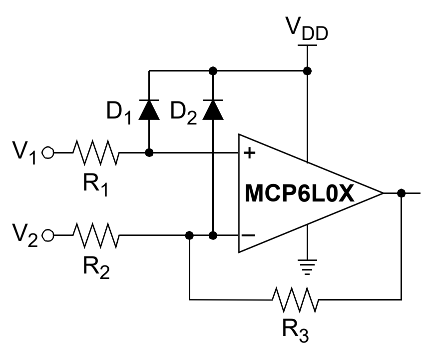
4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6L01/1R/1U/2/4 op amps are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-10 shows an input voltage exceeding both supplies without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit they are in must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings†"**). Figure 4-1 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors, R_1 and R_2, limit the possible current drawn out of the input pins. Diodes, D_1 and D_2, prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above V_{DD}, and dump any currents onto V_{DD}.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-1: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common-mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-7. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6L01/1R/1U/2/4 op amps uses two differential CMOS input stages in parallel. One operates at low Common-mode input voltage (V_{CM}), while the other operates at high V_{CM}. With this topology, and at room temperature, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS} (typically at +25°C).

The transition between the two input stages occurs when $V_{CM} = V_{DD} - 1.1V$. For the best distortion and gain linearity, with noninverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6L01/1R/1U/2/4 op amps is V_{DD} – 35 mV (minimum) and V_{SS} + 35 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$, and V_{DD} = 5.0V. Refer to Figure 2-13 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., >100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-2) improves the feedback loop's stability by making the output load resistive at higher frequencies; the bandwidth will usually be decreased.

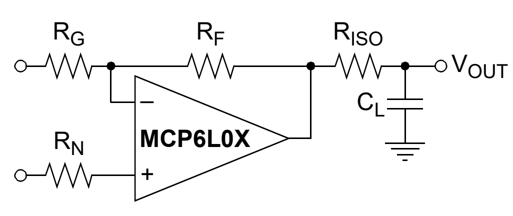


FIGURE 4-2: *Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.*

Bench measurements are helpful in choosing R_{ISO}. Adjust R_{ISO} so that a small signal step response (see Figure 2-14) has reasonable overshoot (e.g., 4%).

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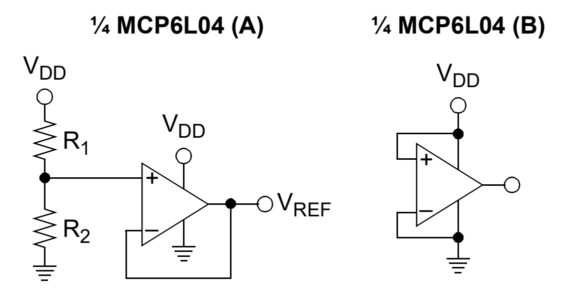
4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF), within 2 mm, for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (e.g., MCP6L04) should be configured as shown in Figure 4-3. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



$$V_{REF} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

FIGURE 4-3: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; this is greater than this family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-4 shows an example of this type of layout.

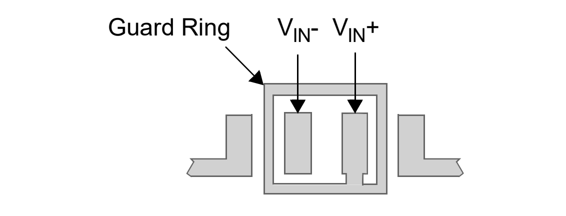


FIGURE 4-4: *Example Guard Ring Layout.*

1. Inverting Amplifiers (Figure 4-4) and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors).
   a) Connect the guard ring to the noninverting input pin ($V_{IN}+$); this biases the guard ring to the same reference voltage as the op amp's input (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}-$) to the input with a wire that does not touch the PCB surface.
2. Noninverting Gain and Unity Gain Buffer.
   a) Connect the guard ring to the inverting input pin ($V_{IN}-$); this biases the guard ring to the Common-mode input voltage.
   b) Connect the noninverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuit

4.7.1 ACTIVE LOW-PASS FILTER

The MCP6L01/1R/1U/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Figure 4-5 shows a second-order Bessel filter with 100 Hz cutoff frequency and a gain of +1 V/V. The component values were selected using Microchip's FilterLab® software; the capacitor values were reduced to a more common range.

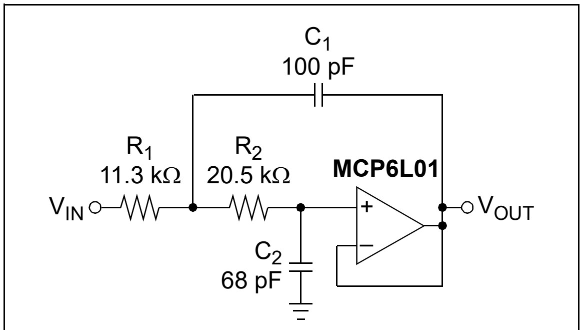


FIGURE 4-5: *Bessel Filter.*

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5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6L01/1R/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6L01/1R/1U/2/4 op amp is available on the Microchip website at www.microchip.com. The model was written and tested in official Orcad™ (Cadence®) owned PSpice®. For other simulators, translation may be required.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be ensured to match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip website at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip website at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990

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NOTES:

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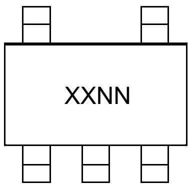
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

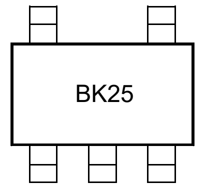
5-Lead SC70 (**MCP6L01**)



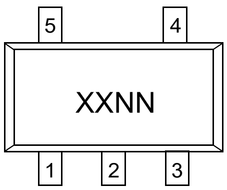
Device	Code
MCP6L01	BKNN

Note: Applies to 5-Lead SC-70.

Example:



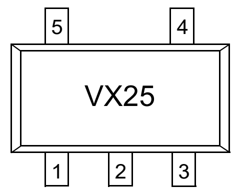
5-Lead SOT-23 (**MCP6L01/1R/1U**)



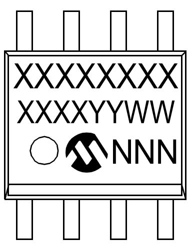
Device	Code
MCP6L01	VXNN
MCP6L01R	VYNN
MCP6L01U	VZNN

Note: Applies to 5-Lead SOT-23.

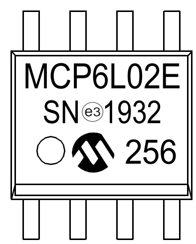
Example:



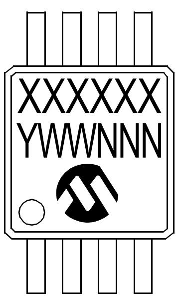
8-Lead SOIC (150 mil) **(MCP6L02)**



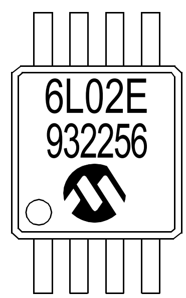
Example:



8-Lead MSOP **(MCP6L02)**



Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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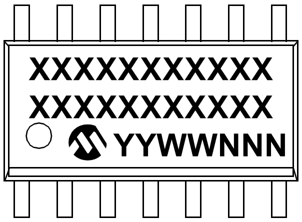
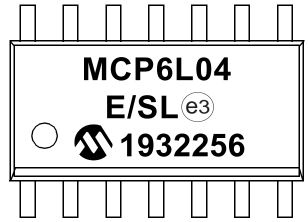
Package Marking Information

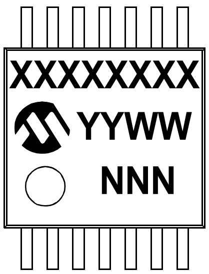
14-Lead SOIC (150 mil) **(MCP6L04)**



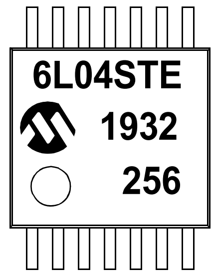
Example:



14-Lead TSSOP **(MCP6L04)**



Example:



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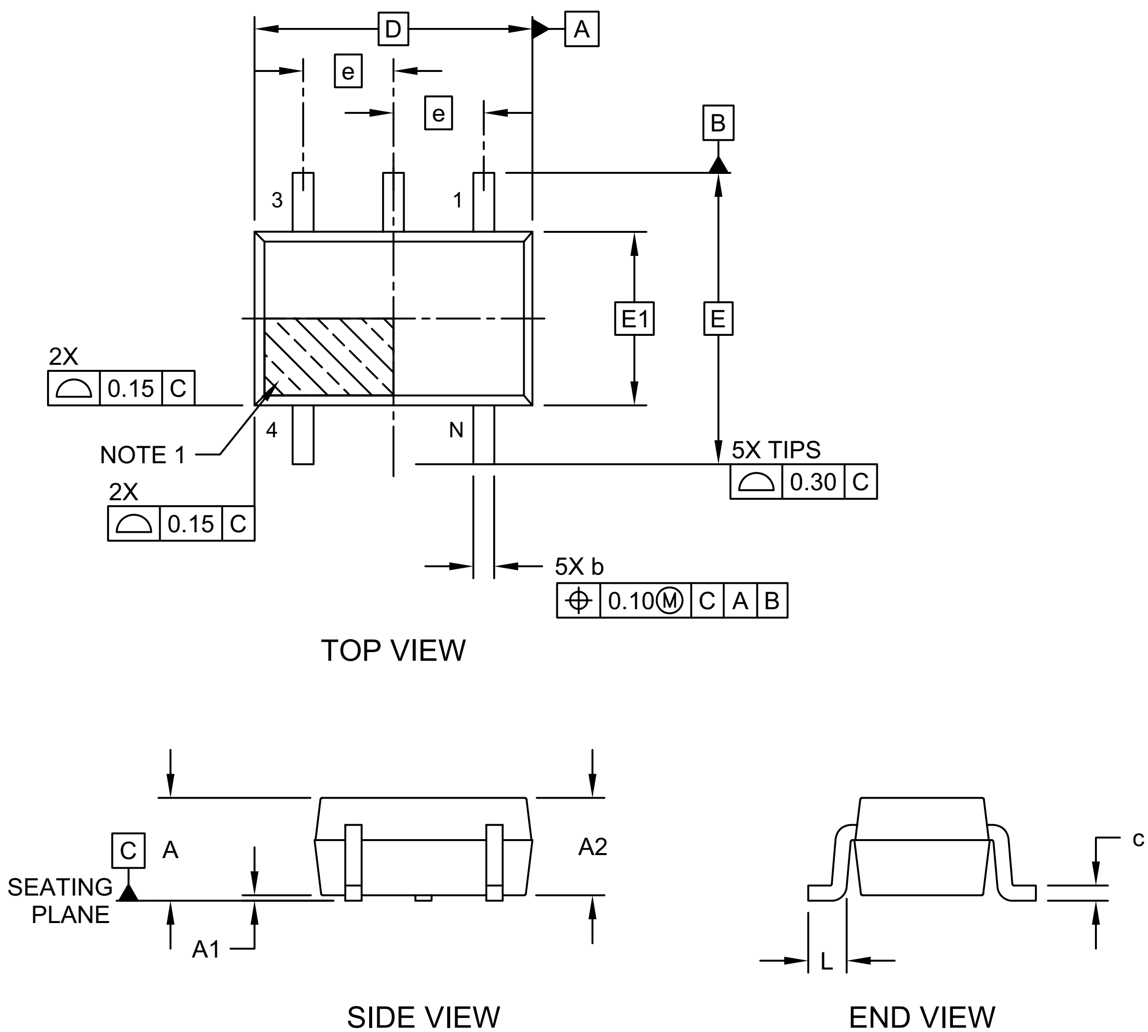
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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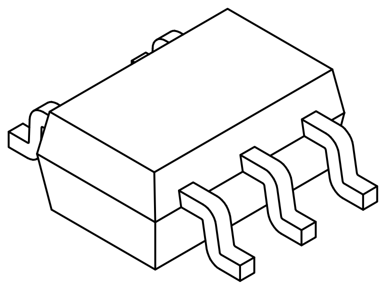
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D	2.00 BSC		
Overall Width	E	2.10 BSC		
Molded Package Width	E1	1.25 BSC		
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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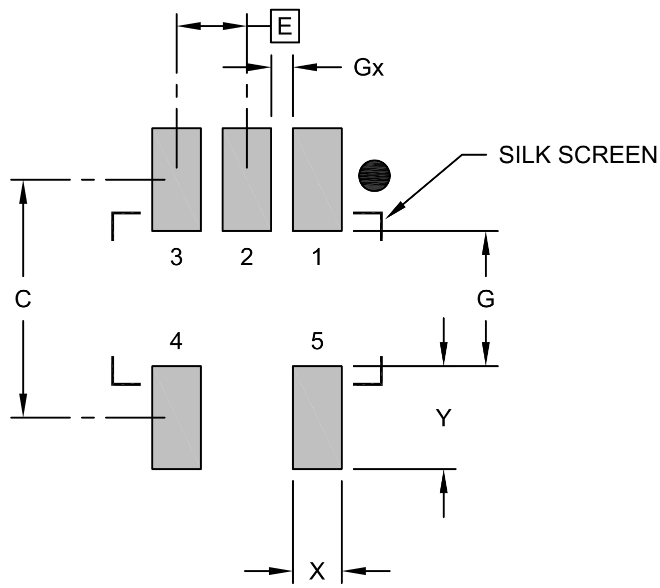
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LT Rev E

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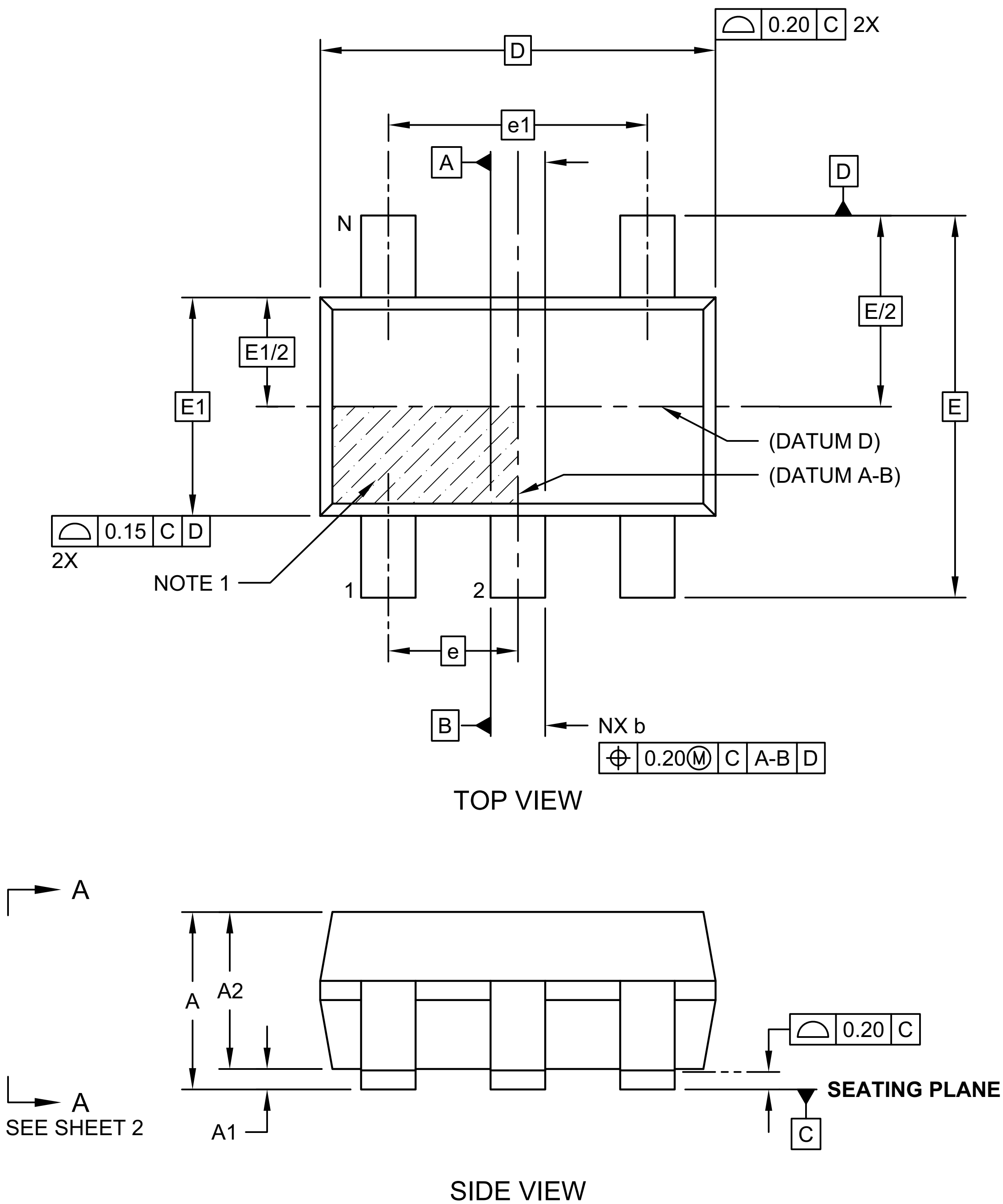
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

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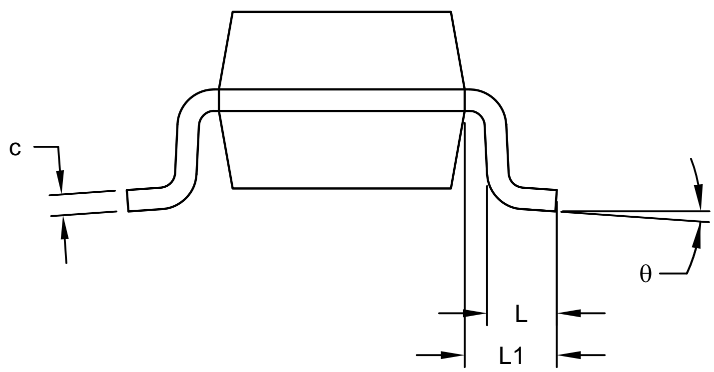
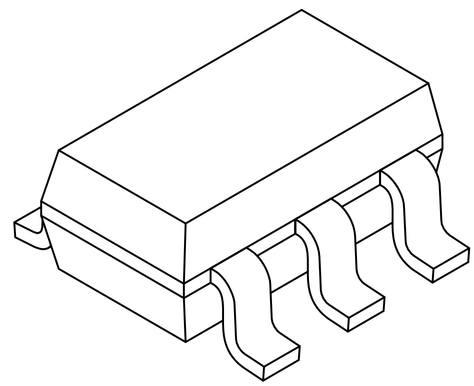
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

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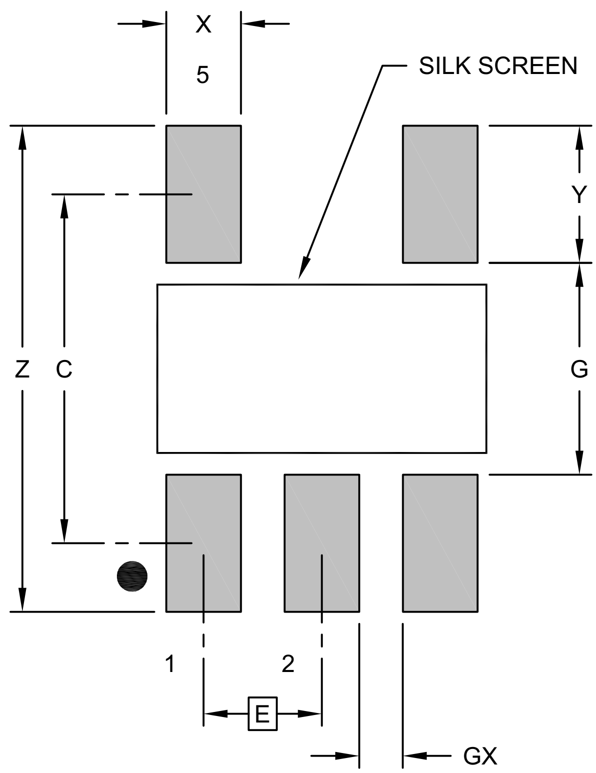
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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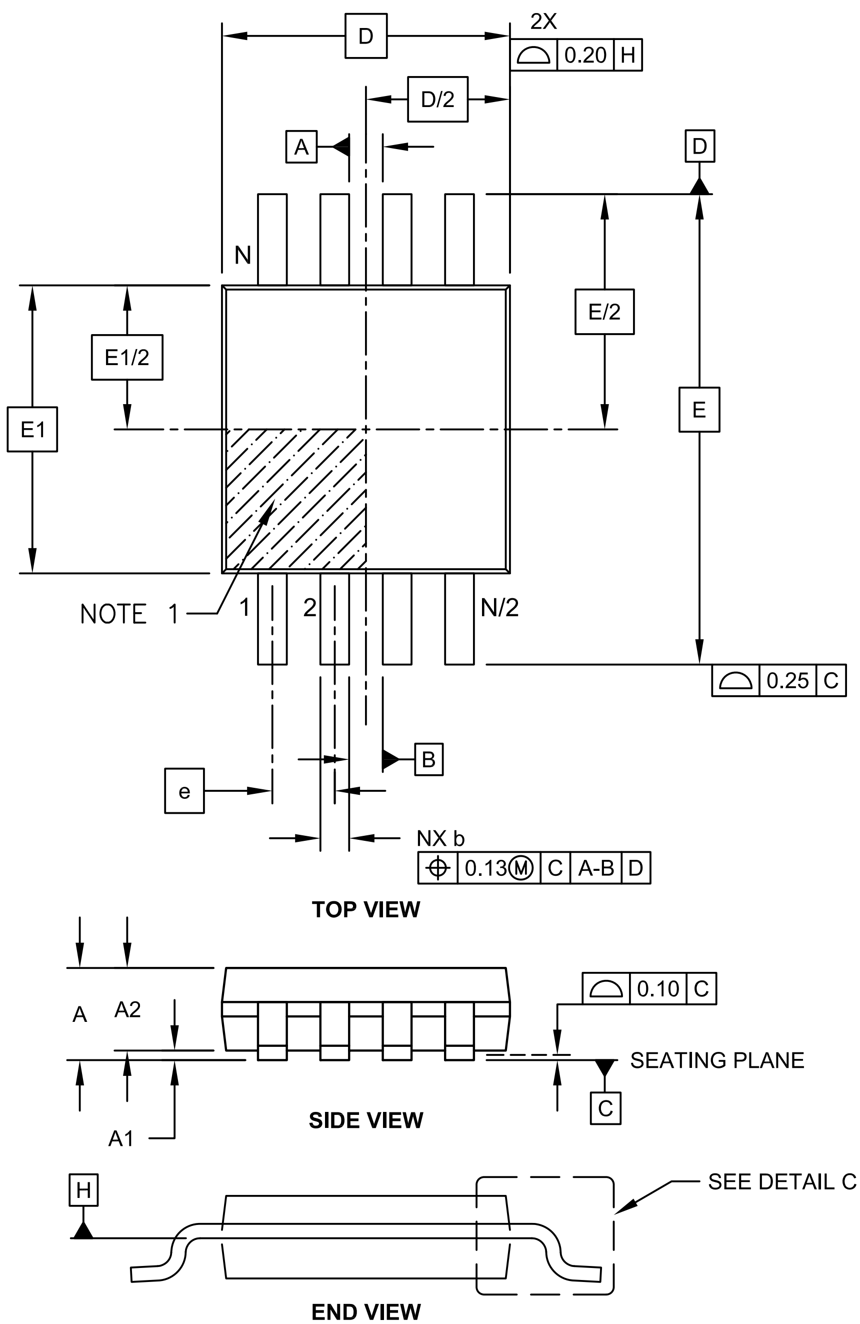
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

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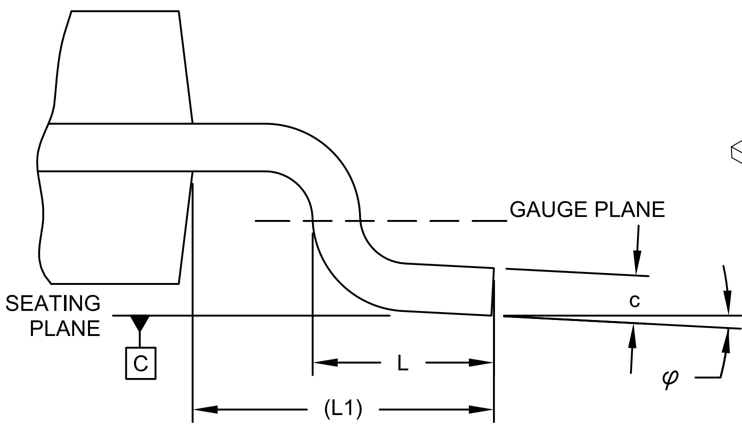
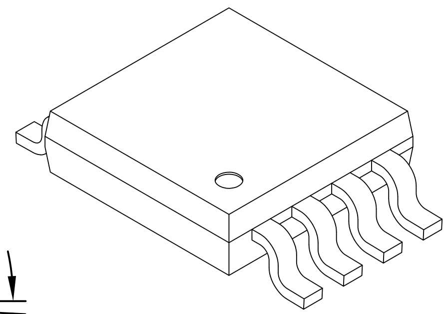
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C



		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

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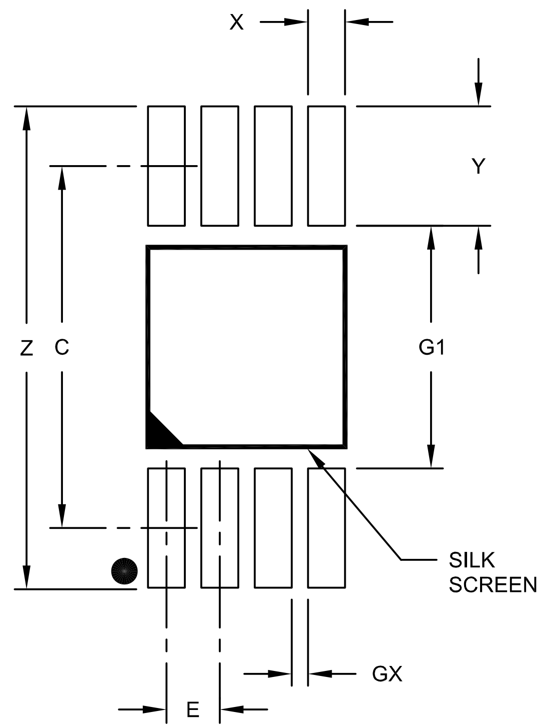
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

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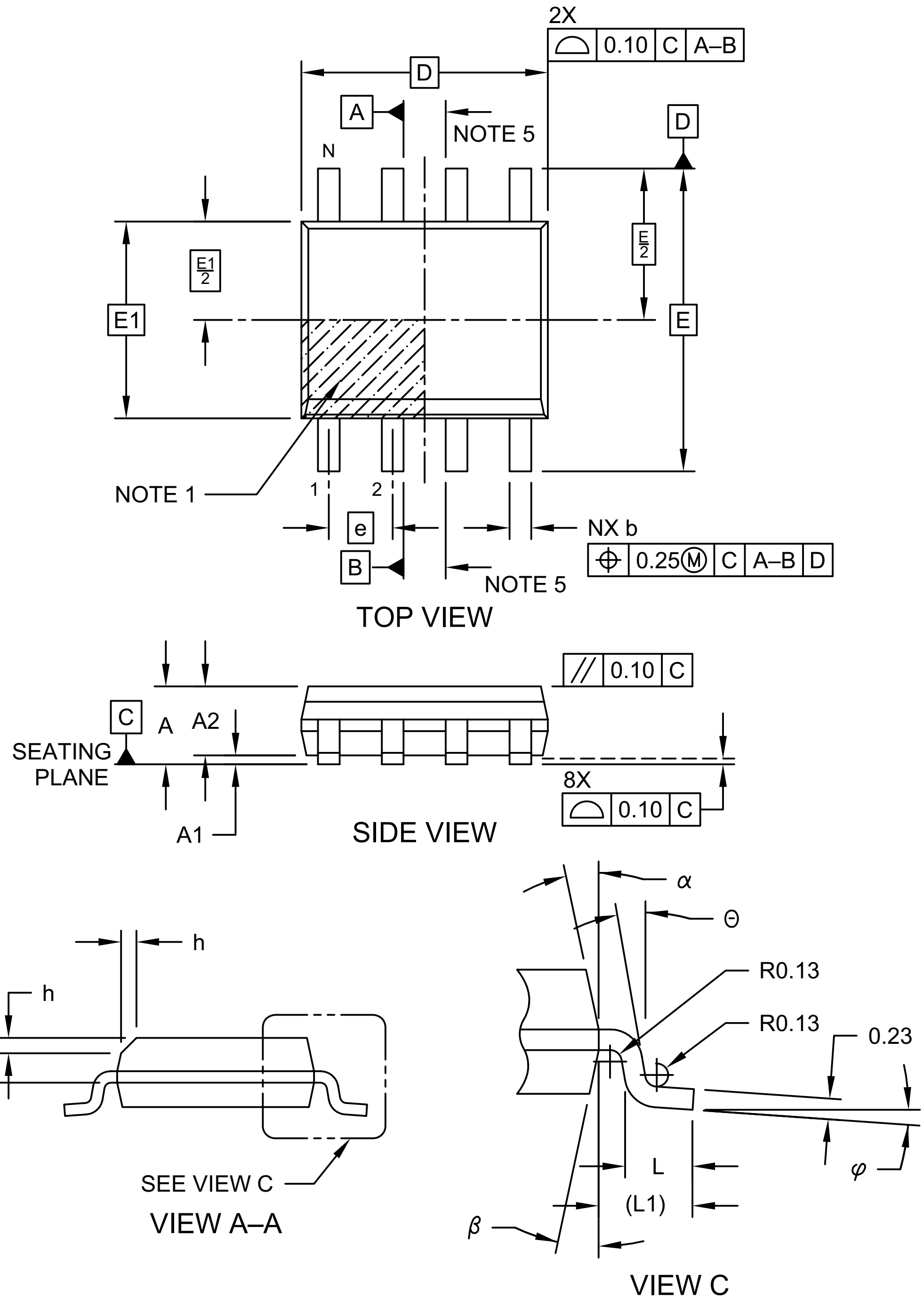
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

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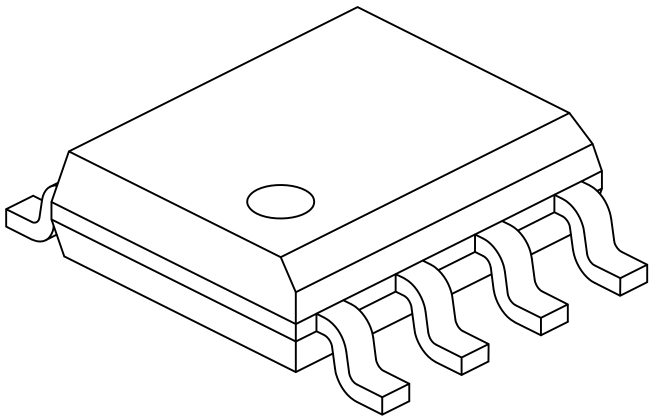
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

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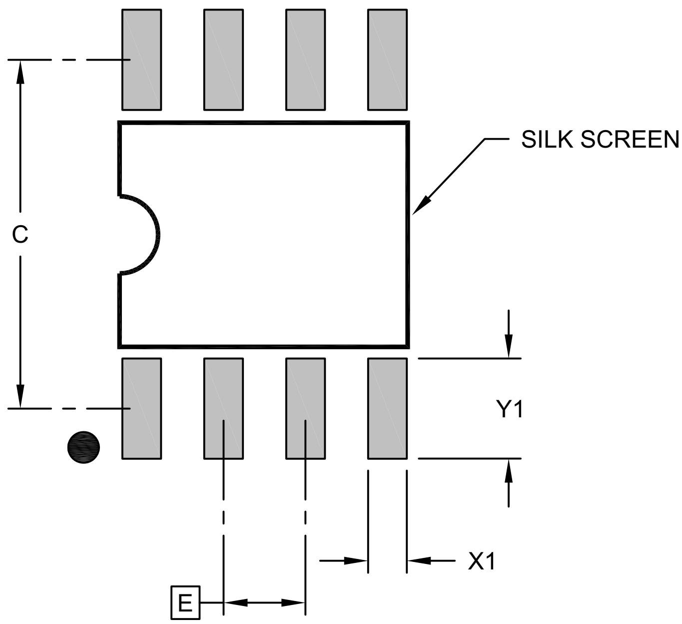
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

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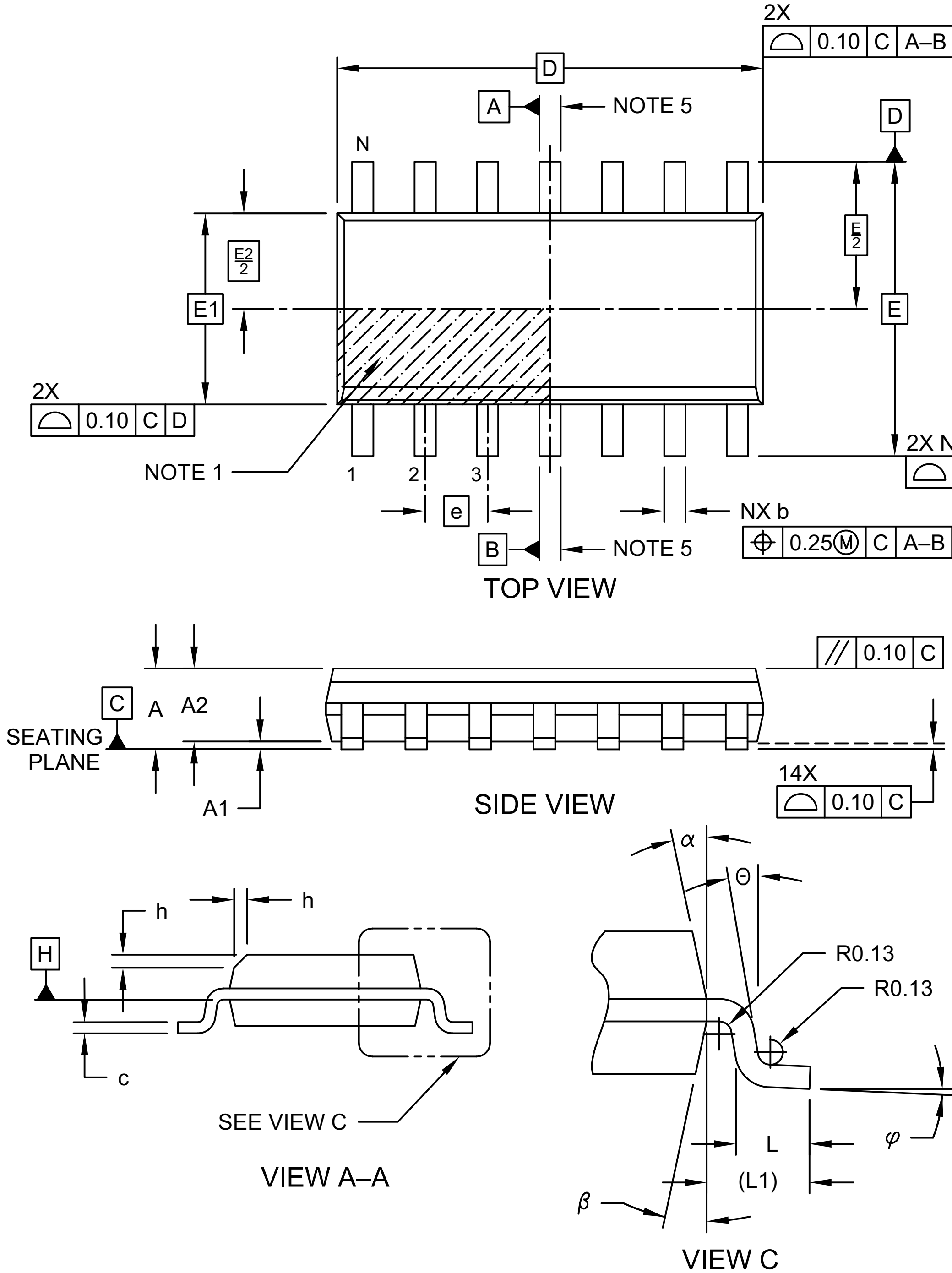
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

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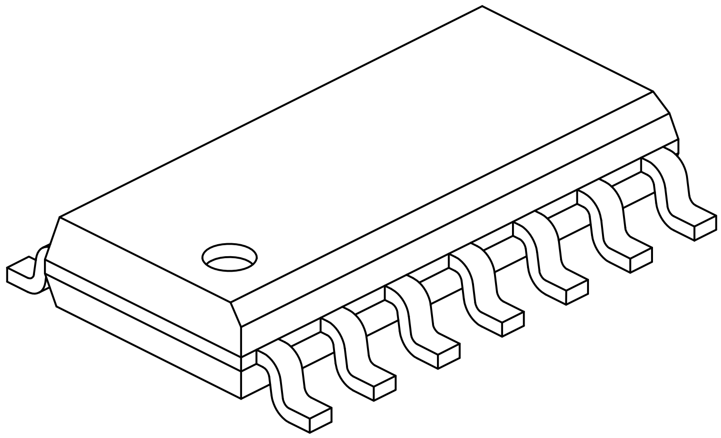
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

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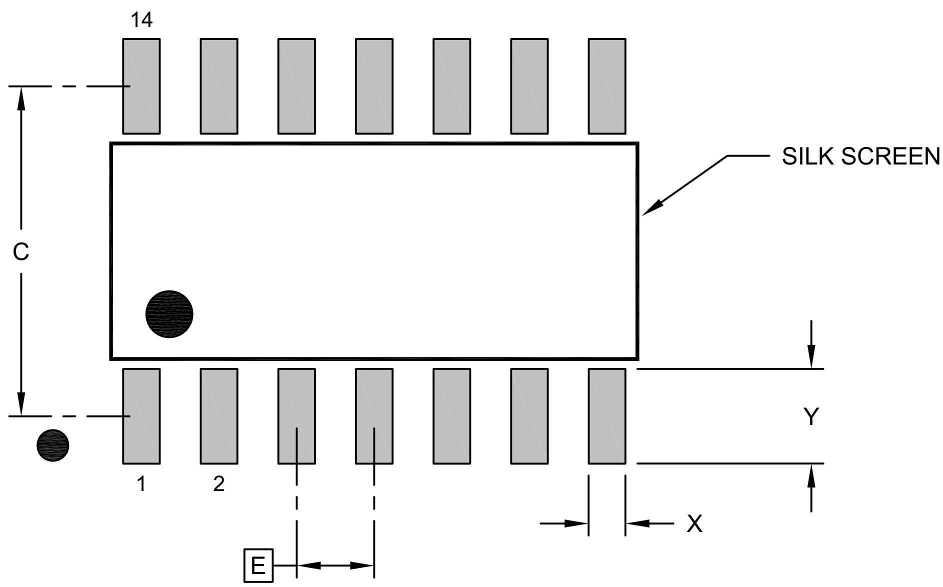
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

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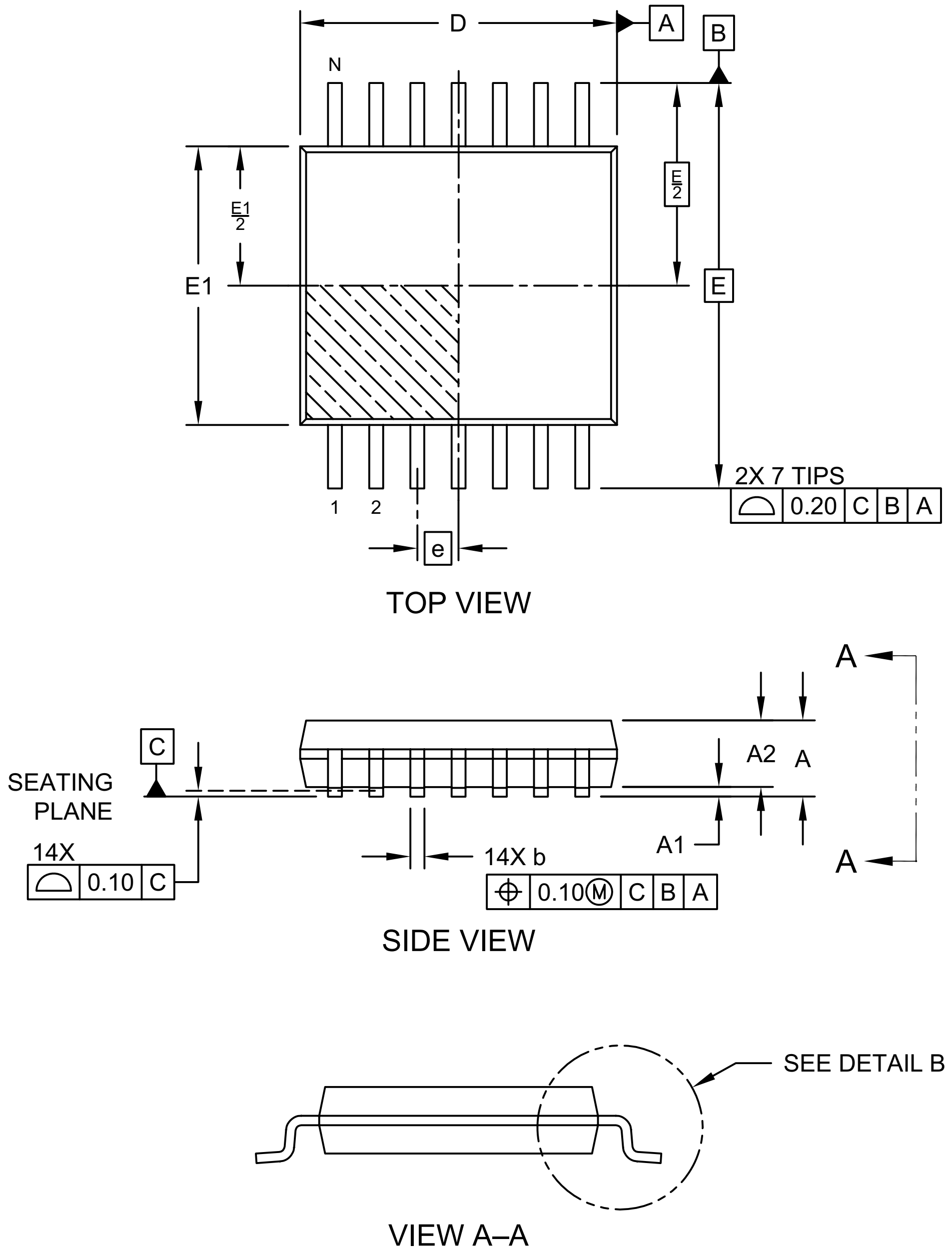
14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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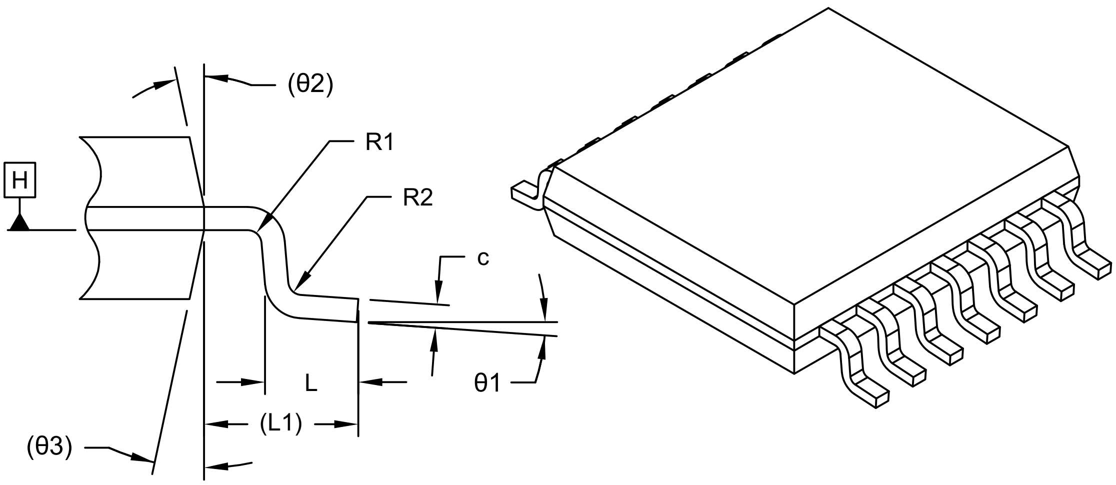
14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087 Rev D Sheet 2 of 2

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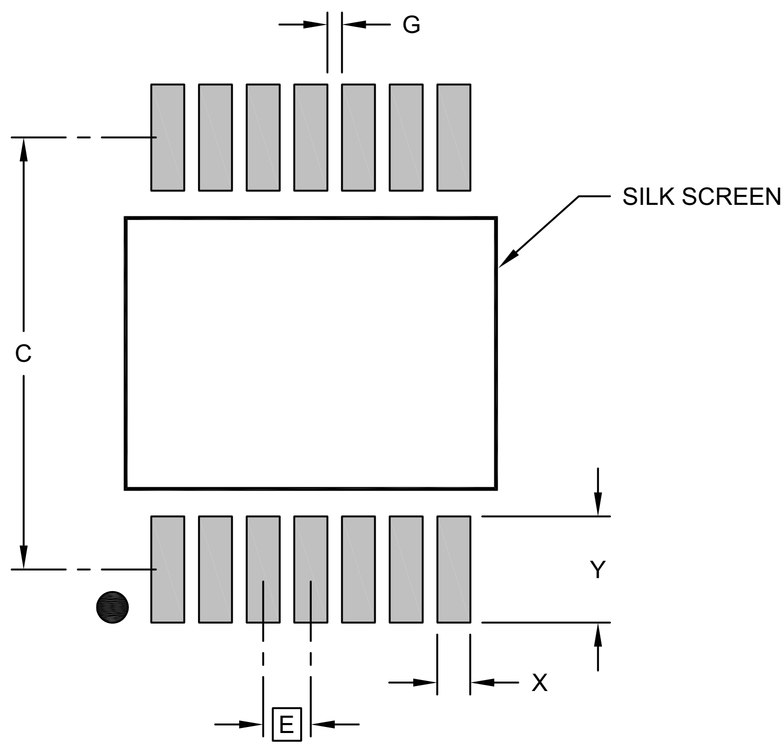
14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev D

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APPENDIX A: REVISION HISTORY

Revision D (March 2020)

The following is the list of modifications:

1. Updated package drawings for the 5-lead SC70 and 14-Lead TSSOP packages in **Section 6.0 “Packaging Information”**.

Revision C (October 2019)

The following is the list of modifications:

1. Updated **Section 6.0 “Packaging Information”**.

Revision B (September 2011)

The following is the list of modifications:

2. Updated the value for the Current at Output and Supply Pins parameter in the **1.1 “Absolute Maximum Ratings†”**section.
3. Added **Section 5.1 “SPICE Macro Model”**.

Revision A (March 2009)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:

MCP6L01T:	Single Op Amp (Tape and Reel) (SC70, SOT-23)
MCP6L01RT:	Single Op Amp (Tape and Reel) (SOT-23)
MCP6L01UT:	Single Op Amp (Tape and Reel) (SOT-23)
MCP6L02T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
MCP6L04T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)

Temperature Range: E = -40°C to +125°C

Package:

LT	=	Plastic Package (SC70), 5-Lead (MCP6L01 only)
OT	=	Plastic Small Outline Transistor (SOT-23), 5-Lead
MS	=	Plastic MSOP, 8-Lead
SN	=	Plastic SOIC (3.90 mm body), 8-Lead
SL	=	Plastic SOIC (3.90 mm body), 14-Lead
ST	=	Plastic TSSOP (4.4 mm body), 14-Lead

Examples:

a) MCP6L01T-E/LT: Tape and Reel, Extended Temperature, 5-Lead SC70 Package.

b) MCP6L01T-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package.

a) MCP6L01RT-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package.

a) MCP6L01UT-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package.

a) MCP6L02T-E/MS: Tape and Reel, Extended Temperature, 8-Lead MSOP Package.

b) MCP6L02T-E/SN: Tape and Reel, Extended Temperature, 8-Lead SOIC Package.

a) MCP6L04T-E/SL: Tape and Reel, Extended Temperature, 14-Lead SOIC Package.

b) MCP6L04T-E/ST: Tape and Reel, Extended Temperature, 14-Lead TSSOP Package.

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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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