

Switchtec PSX PCIe Gen3 Storage Switch Family

PM8546, PM8545, PM8544, PM8543, PM8542, and PM8541

The Switchtec PSX PCIe Gen3 Storage Switch family comprises programmable and high-reliability PCIe Base Specification 3.1-compliant switches supporting up to 96 lanes, 48 ports, 24 virtual switch partitions, 48 Non-Transparent Bridges (NTBs), and hot- and surprise-plug controllers for each port. The switch family also features advanced error containment, comprehensive diagnostics and debug capabilities, a wide breadth of I/O interfaces, and an integrated MIPS processor. PSX switches utilize a system-on-chip architecture that optionally enables customer-differentiated solutions through firmware customization and enhancements.

Applications for the PSX family include PCIe SSD enclosures, flash arrays, multi-host architectures, high-density servers, blade servers, pooled storage/compute, and applications that require customized, high-reliability PCIe switching.

Features

High-Performance Non-Blocking Switches

- Up to 174 GB/s switching capacity
- 96-lane, 80-lane, 64-lane, 48-lane, 32-lane, and 24-lane variants
- Ports bifurcate from x2 to x16 lanes
- Up to 48 NTBs assignable to any port
- Logical Non-Transparent (NT) interconnect allows for larger topologies
- Supports 1+1 and N+1 failover mechanisms
- NT address translation using direct windows and multiple sub-windows per BAR
- Supports multicast groups per port

Error Containment

- Advanced Error Reporting (AER) on all ports
- Downstream Port Containment (DPC) on all downstream ports
- Poisoned TLP blocking
- Completion Timeout Synthesis (CTS) to prevent an error state in an upstream host due to incomplete non-posted transactions
- Upstream Error Containment (UEC), a programmable feature protecting errors from propagating upstream
- Hot- and surprise-plug controllers per port
- GPIOs configurable for different cable/connector standards

PCIe Interfaces

- Passive, managed, and optical cables
- SFF-8644, SFF-8643, SFF-8639, OcuLink, and other connectors

Diagnostics and Debug

- Transaction Layer Packet (TLP) generator for testing and debugging of links and error handling
- Built-in PCIe analyzer with flexible triggering
- Real-time eye capture
- Any-to-any port mirroring for debug purposes



Highlights

- High-reliability PCIe: robust error containment, hot- and surprise-plug controllers per port, end-to-end data integrity protection, ECC protection on RAMs, high-quality, low-power SERDES
- PSX Software Development Kit (SDK): enables customer-differentiated solutions in areas such as error containment and surprise-plug
- Integrated enclosure management processor and I/O interfaces, SDK, and a turn-key enclosure management solution
- Comprehensive diagnostics and debugging: PCIe generator and analyzer, per-port performance and error counters, multiple loopback modes, and real-time eye capture
- Significant power, cost, and board space savings with support for:
 - Up to 48 ports, 48 NTBs, and 24 virtual switch partitions
 - Flexible x2, x4, x8 and x16 port bifurcation with no restrictions on configuring ports as either upstream or downstream, or on mapping ports to NTBs

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Diagnostics and Debug (Continued)

- External loopback at PHY and TLP layers
- Errors, statistics, performance, and TLP latency counters

Peripheral I/O Interfaces

- Up to 11 Two-Wire Interfaces (TWIs) with SMBus support
- Up to 4 SFF-8485-compliant SGPIO ports
- Up to 106 parallel GPIO pins
- 10/100 Ethernet MAC port (MII/RMII) (PSX 96x/80x/64xG3)
- 16-bit local bus interface with ECC protection
- Up to 4 UARTs
- JTAG and EJTAG interface

High-speed I/O

- PCIe Gen3 8 GT/s
- Supports PCIe-compliant link training and manual PHY configuration

Chiplink Diagnostic Tools

- Extensive debug, diagnostics, configuration, and analysis tools with an intuitive GUI
- Access to configuration data, management capabilities, and signal integrity analysis tools (such as real-time eye capture)
- Connects to device over in-band PCIe or sideband signals (UART and EJTAG)

Ordering Information

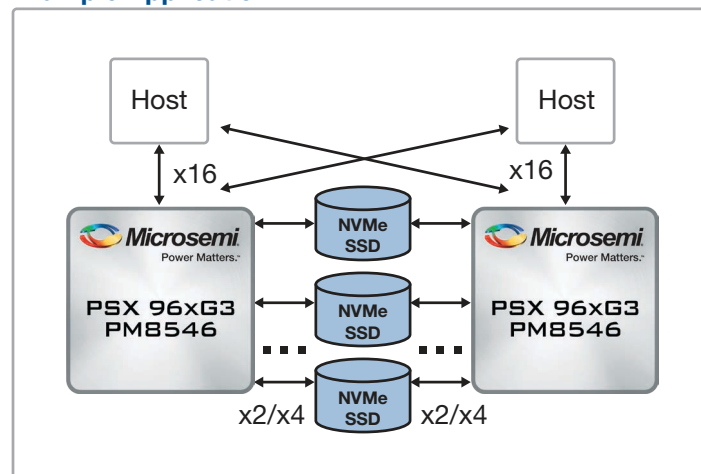
Product	Lanes	Ports/NTBs	Partitions	Hot-plug Controllers	Package	Ordering No.
PSX 96xG3 PCIe Storage Switch	96	48	24	48	37.5 mm x 37.5 mm	PM8546B-FEI
PSX 80xG3 PCIe Storage Switch	80	40	20	40	37.5 mm x 37.5 mm	PM8545B-FEI
PSX 64xG3 PCIe Storage Switch	64	32	16	32	37.5 mm x 37.5 mm	PM8544B-FEI
PSX 48xG3 PCIe Storage Switch	48	24	12	24	27.0 mm x 27.0 mm	PM8543B-F3EI
PSX 32xG3 PCIe Storage Switch	32	16	8	16	27.0 mm x 27.0 mm	PM8542B-F3EI
PSX 24xG3 PCIe Storage Switch	24	12	6	12	27.0 mm x 27.0 mm	PM8541B-F3EI

Evaluation Kits

The evaluation kits are used to evaluate and test device functionality, measure signal integrity, and customize and develop PSX firmware. The following kits are available:

- PM5461-KIT—PSX/PFX 96/80/64xG3, 1-Slot, 16 HD Evaluation Kit (PMC-2151996)
- PM5462-KIT—PSX/PFX 48/32/24xG3, 3-Slot Evaluation Kit (PMC-2151645)

Example Application



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