MCP6V06/7/8

300 µA, Auto-Zeroed Op Amps

Features

- High DC Precision:
  - V_{OS} Drift: ±50 nV/°C (maximum)
  - V_{OS}: ±3 µV (maximum)
  - A_{OL}: 125 dB (minimum)
  - PSRR: 125 dB (minimum)
  - CMRR: 120 dB (minimum)
  - E_{ni}: 1.7 μV_{P-P} (typical), f = 0.1 Hz to 10 Hz
  - E_{ni}: 0.54 µVp-p (typical), f = 0.01 Hz to 1 Hz
- Low Power and Supply Voltages:
  - I_Q: 300 µA/amplifier (typical)
  - Wide Supply Voltage Range: 1.8V to 5.5V
- Easy to Use:
  - Rail-to-Rail Input/Output
  - Gain Bandwidth Product: 1.3 MHz (typical)
  - Unity Gain Stable
  - Available in Single and Dual
  - Single with Chip Select ($\overline{CS}$): MCP6V08
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Portable Instrumentation
- Sensor Conditioning
- Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Parts

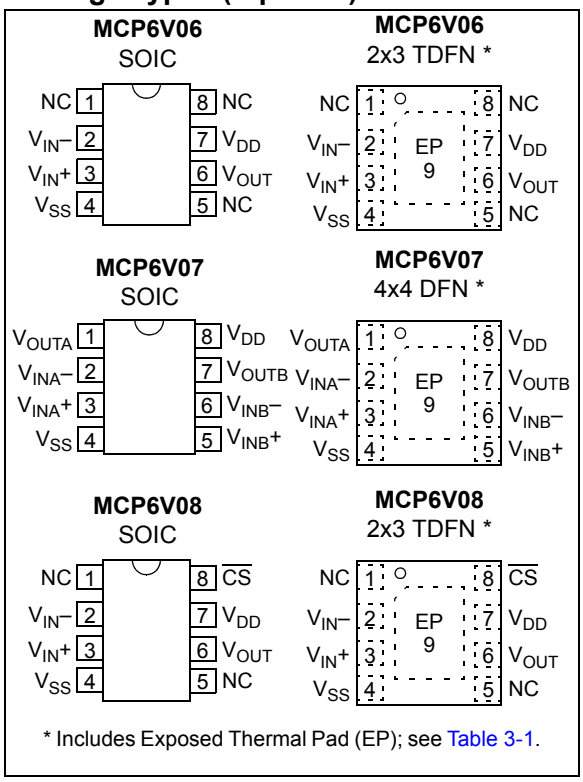
- MCP6V01/2/3: Spread clock, lower offset

Description

The Microchip Technology Inc. MCP6V06/7/8 family of operational amplifiers has input offset voltage correction for very low offset and offset drift. These devices have a wide gain bandwidth product (1.3 MHz, typical) and strongly reject switching noise. They are unity gain stable, have no 1/f noise, and have good PSRR and CMRR. These products operate with a single supply voltage as low as 1.8V, while drawing 300 µA/amplifier (typical) of quiescent current.

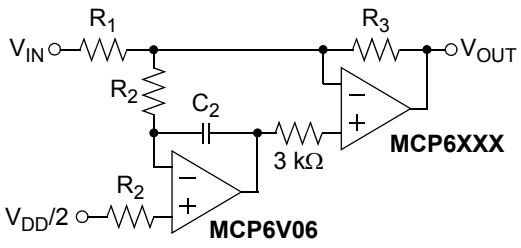
The Microchip Technology Inc. MCP6V06/7/8 op amps are offered in single (MCP6V06), single with Chip Select ($\overline{CS}$) (MCP6V08), and dual (MCP6V07). They are designed in an advanced CMOS process.

Package Types (top view)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application Circuit



Offset Voltage Correction for Power Driver

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† ... V_{SS} – 1.0V to V_{DD}+1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD}+0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 4 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.1 "Rail-to-Rail Inputs"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3	—	+3	µV	T_A = +25°C **(Note 1)**
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC_1	-50	—	+50	nV/°C	T_A = -40 to +125°C **(Note 1)**
Input Offset Voltage Quadratic Temp. Co.	TC_2	—	±0.15	—	nV/°C^2	T_A = -40 to +125°C
Power Supply Rejection	PSRR	125	142	—	dB	**(Note 1)**
Input Bias Current and Impedance						
Input Bias Current	I_B	—	+6	—	pA	
Input Bias Current across Temperature	I_B	—	+140	—	pA	T_A = +85°C
	I_B	—	+1500	+5000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	-85	—	pA	
Input Offset Current across Temperature	I_{OS}	—	-85	—	pA	T_A = +85°C
	I_{OS}	-1000	-190	1000	pA	T_A = +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common-Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.20	—	V_{DD} + 0.20	V	**(Note 2)**
Common-Mode Rejection	CMRR	120	136	—	dB	V_{DD} = 1.8V, V_{CM} = -0.2V to 2.0V **(Note 1, Note 2)**
	CMRR	130	147	—	dB	V_{DD} = 5.5V, V_{CM} = -0.2V to 5.7V **(Note 1, Note 2)**
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	125	147	—	dB	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V **(Note 1)**
	A_{OL}	135	158	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V **(Note 1)**

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CMR} changed across temperature for the first three production lots.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 15	mV	G = +2, 0.5V input overdrive
Output Short Circuit Current	I_{SC}	—	±7	—	mA	V_{DD} = 1.8V
	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per amplifier	I_Q	200	300	400	µA	I_O = 0
POR Trip Voltage	V_{POR}	1.15	—	1.65	V	

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CMR} changed across temperature for the first three production lots.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier AC Response						
Gain Bandwidth Product	GBWP	—	1.3	—	MHz	
Slew Rate	SR	—	0.5	—	V/µs	
Phase Margin	PM	—	65	—	°	G = +1
Amplifier Noise Response						
Input Noise Voltage	E_{ni}	—	0.54	—	$µV_{P-P}$	f = 0.01 Hz to 1 Hz
	E_{ni}	—	1.7	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	82	—	nV/√Hz	f < 2.5 kHz
	e_{ni}	—	52	—	nV/√Hz	f = 100 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	
Amplifier Distortion (Note 1)						
Intermodulation Distortion (AC)	IMD	—	32	—	$µV_{PK}$	V_{CM} tone = 50 mV_{PK} at 1 kHz, G_N = 1, V_{DD} = 1.8V
	IMD	—	25	—	$µV_{PK}$	V_{CM} tone = 50 mV_{PK} at 1 kHz, G_N = 1, V_{DD} = 5.5V
Amplifier Step Response						
Start Up Time	t_{STR}	—	500	—	µs	V_{OS} within 50 µV of its final value
Offset Correction Settling Time	t_{STL}	—	300	—	µs	G = +1, V_{IN} step of 2V, V_{OS} within 50 µV of its final value
Output Overdrive Recovery Time	t_{ODR}	—	100	—	µs	G = -100, ±0.5V input overdrive to V_{DD}/2, V_{IN} 50% point to V_{OUT} 90% point **(Note 2)**

Note 1: These parameters were characterized using the circuit in Figure 1-7. Figure 2-37 and Figure 2-38 show both an IMD tone at DC and a residual tone at1 kHz; all other IMD and clock tones are spread by the randomization circuitry.

2: t_{ODR} includes some uncertainty due to clock edge timing.

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Pull-Down Resistor (MCP6V08)						
$\overline{CS}$ Pull-Down Resistor	R_{PD}	3	5	—	MΩ	
$\overline{CS}$ Low Specifications (MCP6V08)						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.3V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications (MCP6V08)						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.7V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	V_{DD}/R_{PD}	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current per amplifier	I_{SS}	—	-0.7	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 1.8V
	I_{SS}	—	-2.3	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 5.5V
Amplifier Output Leakage, $\overline{CS}$ High	I_{O_LEAK}	—	20	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications (MCP6V08)						
$\overline{CS}$ Low to Amplifier Output On Turn-on Time	t_{ON}	—	11	100	µs	$\overline{CS}$ Low = V_{SS}+0.3 V, G = +1 V/V, V_{OUT} = 0.9 V_{DD}/2
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ High = V_{DD} – 0.3 V, G = +1 V/V, V_{OUT} = 0.1 V_{DD}/2
Internal Hysteresis	V_{HYST}	—	0.25	—	V	

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	41	—	°C/W	
Thermal Resistance, 8L-4x4 DFN	θ_{JA}	—	44	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (150°C).

2: Measured on a standard JC51-7, four layer printed circuit board with ground plane and vias.

1.3 Timing Diagrams

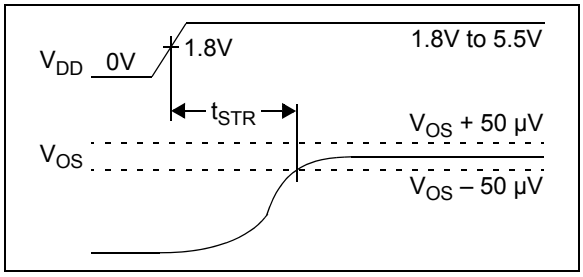


FIGURE 1-1: *Amplifier Start Up.*

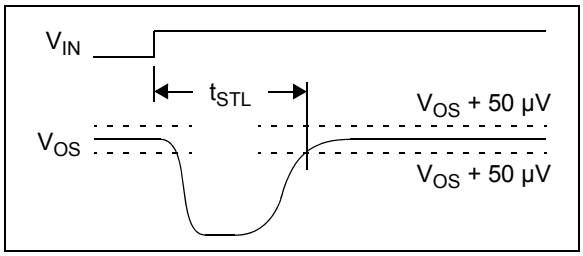


FIGURE 1-2: *Offset Correction Settling Time.*

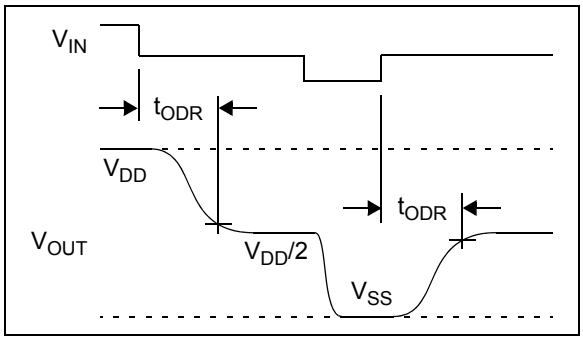


FIGURE 1-3: *Output Overdrive Recovery.*

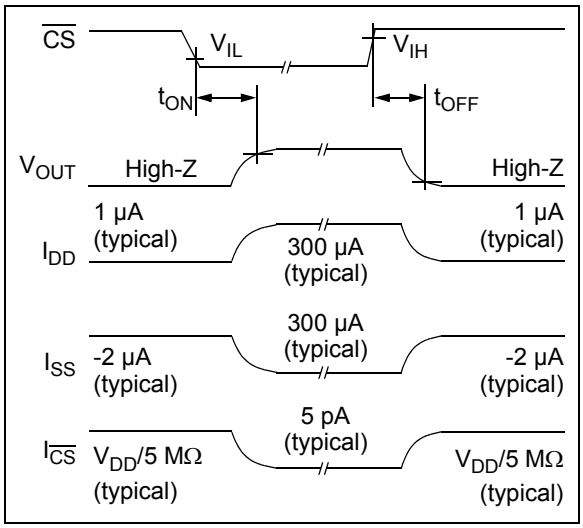


FIGURE 1-4: *Chip Select (MCP6V08).*

1.4 Test Circuits

The circuits used for the DC and AC tests are shown in Figure 1-5 and Figure 1-6. Lay the bypass capacitors out as discussed in **Section 4.3.8 "Supply Bypassing and Filtering"**. R_N is equal to the parallel combination of R_F and R_G to minimize bias current effects.

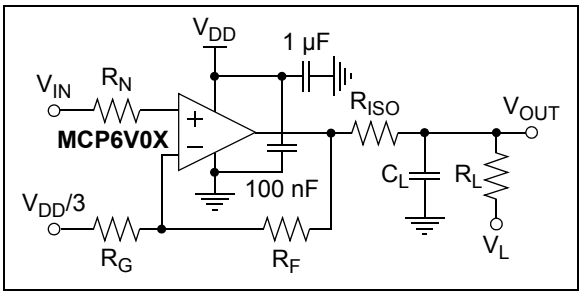


FIGURE 1-5: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

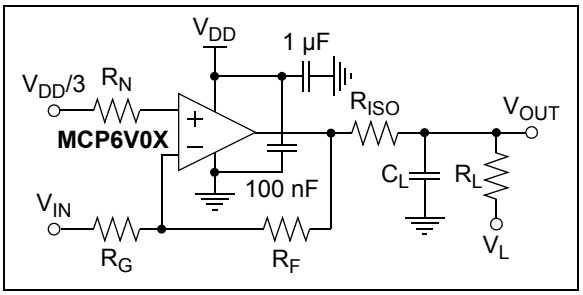


FIGURE 1-6: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

The circuit in Figure 1-7 tests the op amp input's dynamic behavior (i.e., IMD, t_{STR}, t_{STL} and t_{ODR}). The potentiometer balances the resistor network (V_{OUT} should equal V_{REF} at DC). The op amp's common mode input voltage is $V_{CM} = V_{IN}/2$. The error at the input (V_{ERR}) appears at V_{OUT} with a noise gain of 10 V/V.

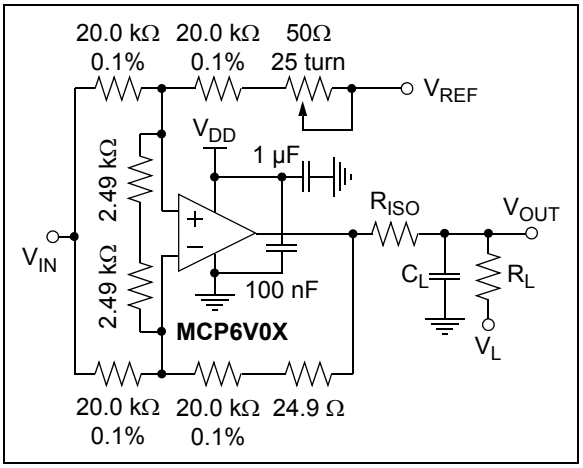


FIGURE 1-7: *Test Circuit for Dynamic Input Behavior.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.1 DC Input Precision

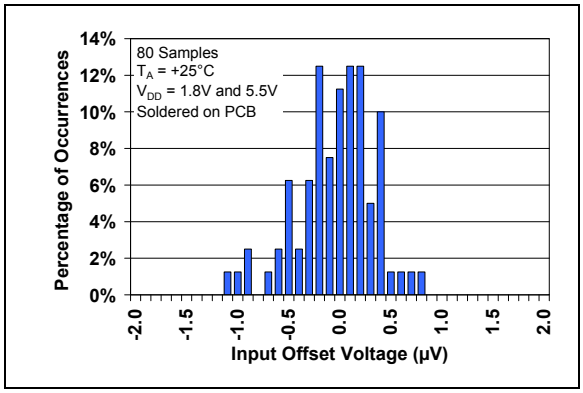


FIGURE 2-1: *Input Offset Voltage.*

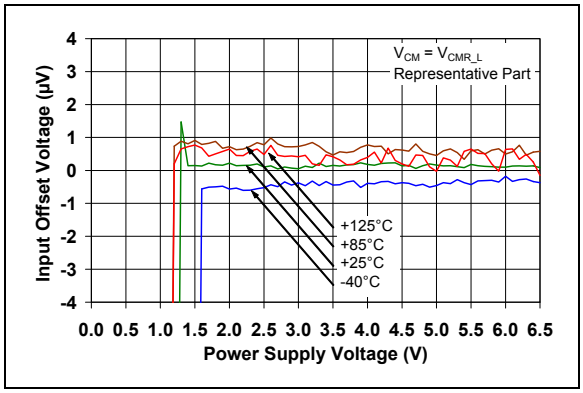


FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = V_{CMR_L}.*

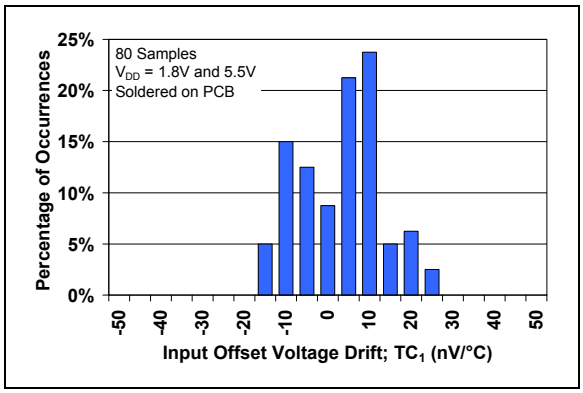


FIGURE 2-2: *Input Offset Voltage Drift.*

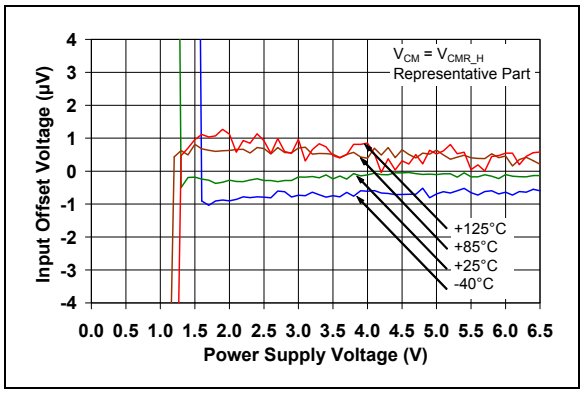


FIGURE 2-5: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = V_{CMR_H}.*

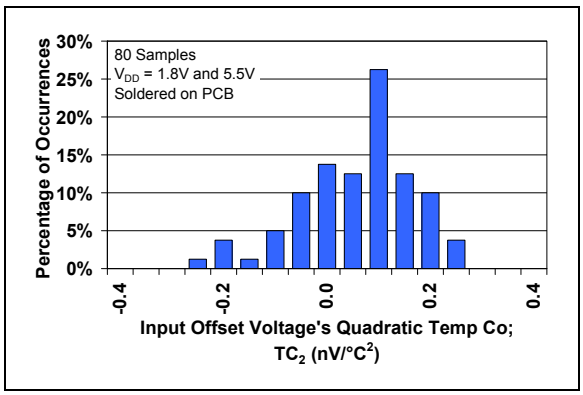


FIGURE 2-3: *Input Offset Voltage Quadratic Temp Co.*

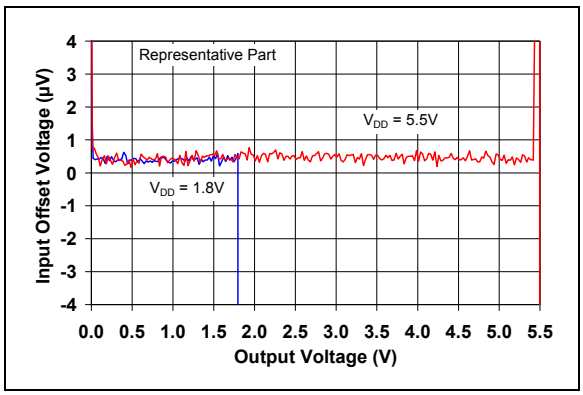


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

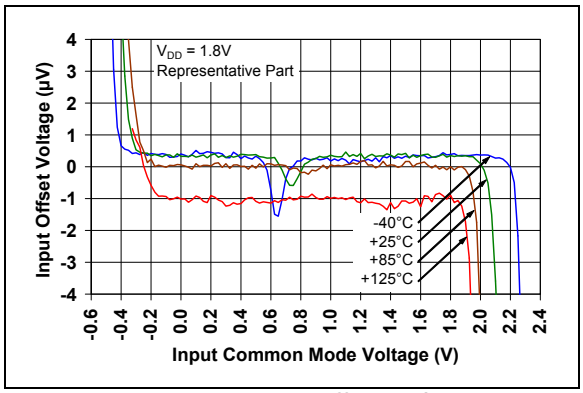


FIGURE 2-7: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 1.8V.*

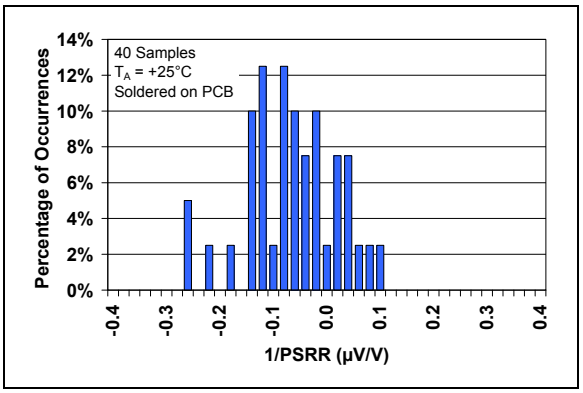


FIGURE 2-10: *PSRR.*

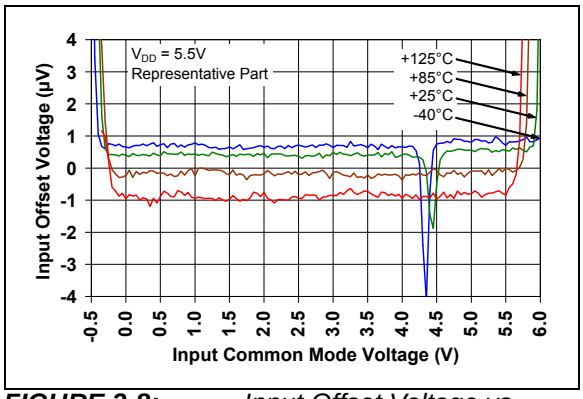


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 5.5V.*

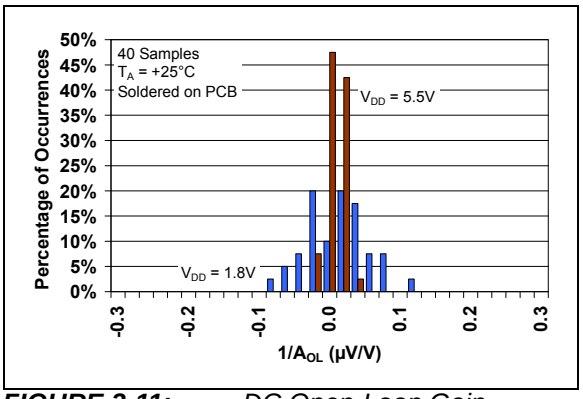


FIGURE 2-11: *DC Open-Loop Gain.*

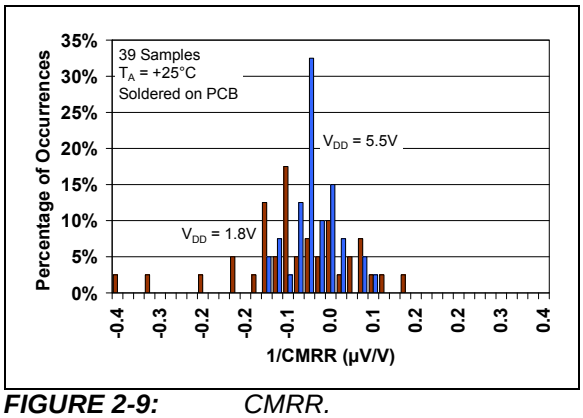


FIGURE 2-9: *CMRR.*

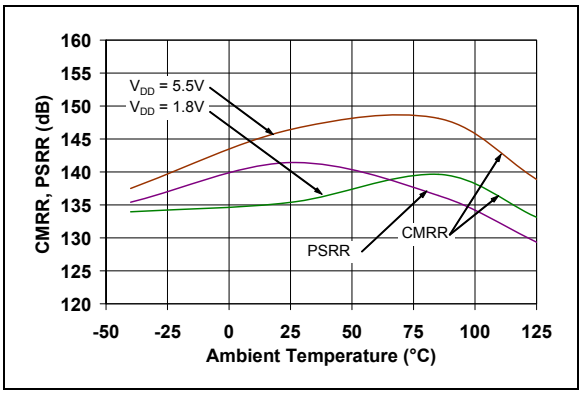


FIGURE 2-12: *CMRR and PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

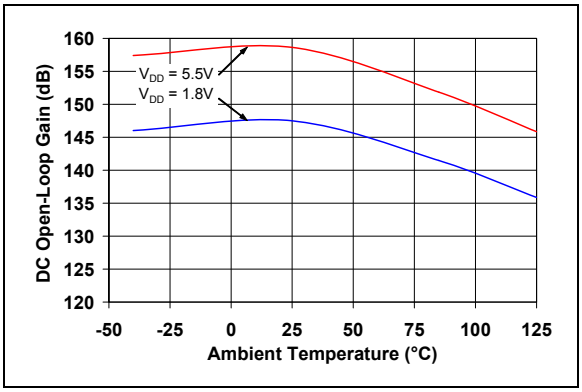


FIGURE 2-13: *DC Open-Loop Gain vs. Ambient Temperature.*

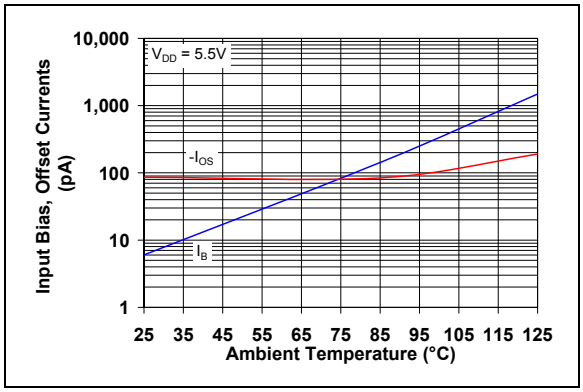


FIGURE 2-16: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = +5.5V.*

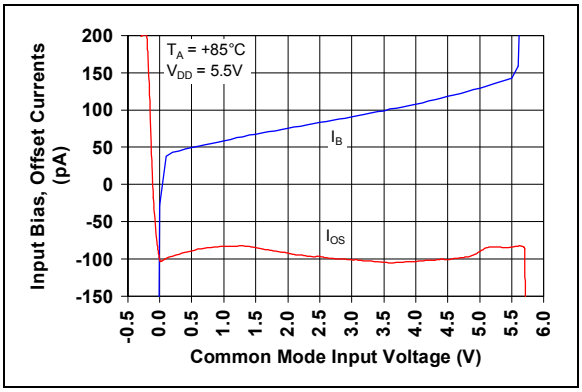


FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

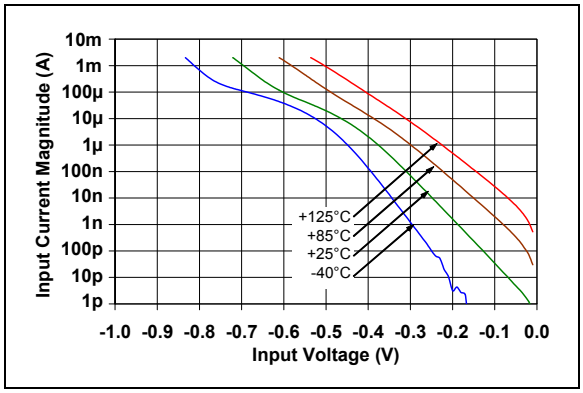


FIGURE 2-17: *Input Bias Current vs. Input Voltage (below V_{SS}).*

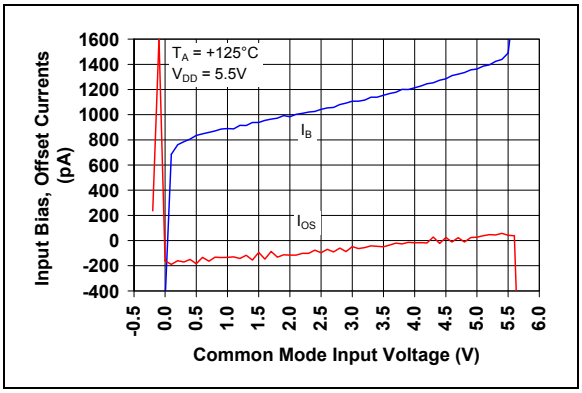


FIGURE 2-15: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.2 Other DC Voltages and Currents

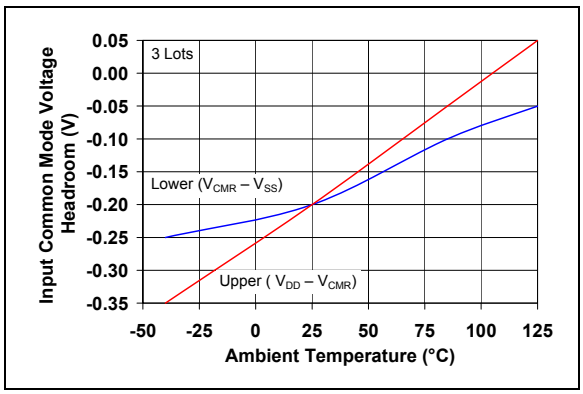


FIGURE 2-18: *Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.*

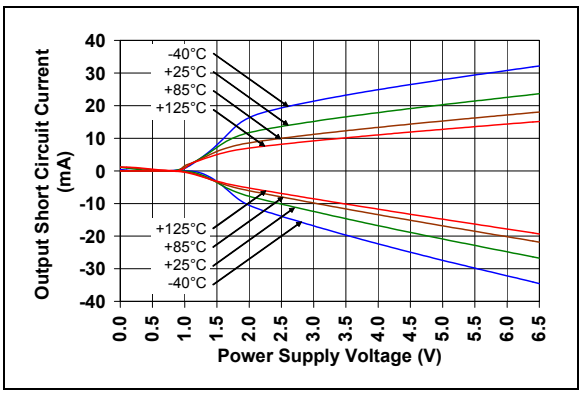


FIGURE 2-21: *Output Short Circuit Current vs. Power Supply Voltage.*

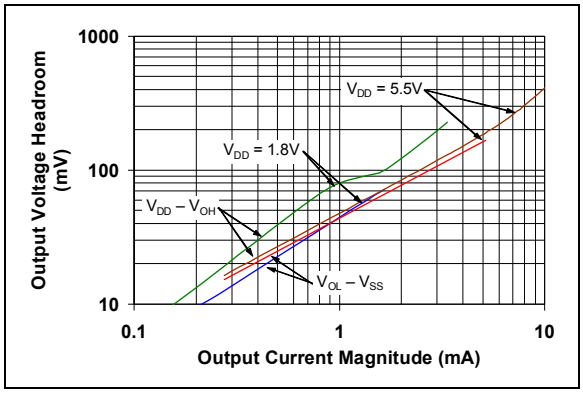


FIGURE 2-19: *Output Voltage Headroom vs. Output Current.*

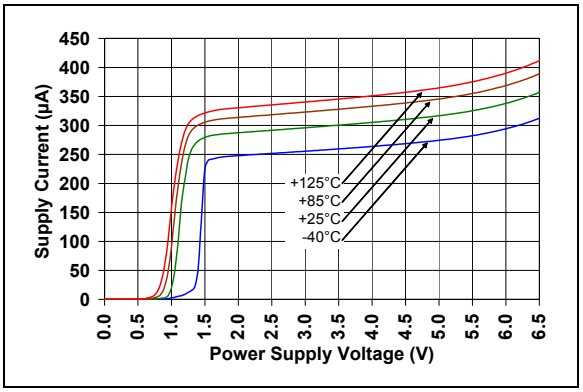


FIGURE 2-22: *Supply Current vs. Power Supply Voltage.*

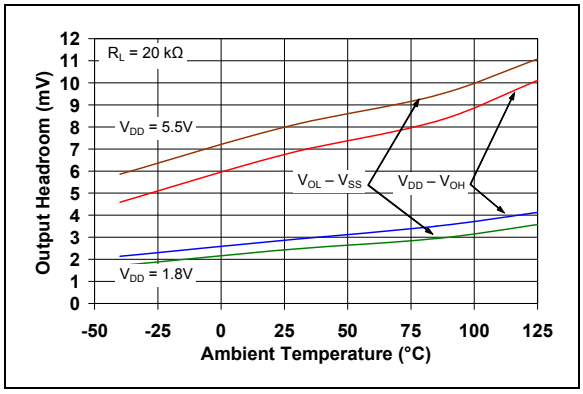


FIGURE 2-20: *Output Voltage Headroom vs. Ambient Temperature.*

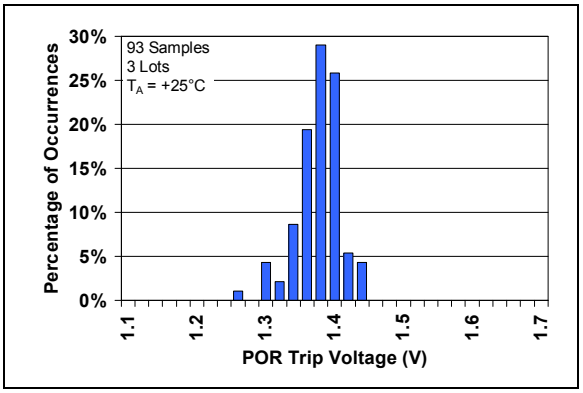


FIGURE 2-23: *Power On Reset Trip Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

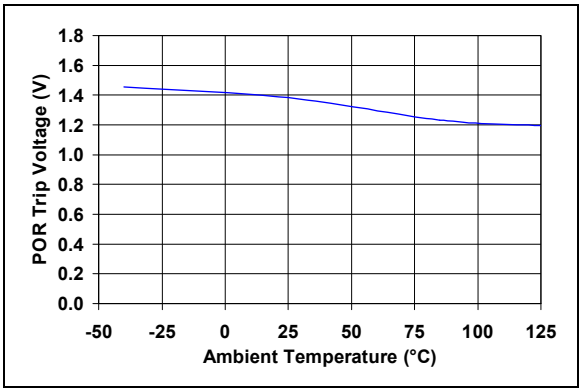


FIGURE 2-24: *Power On Reset Voltage vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.3 Frequency Response

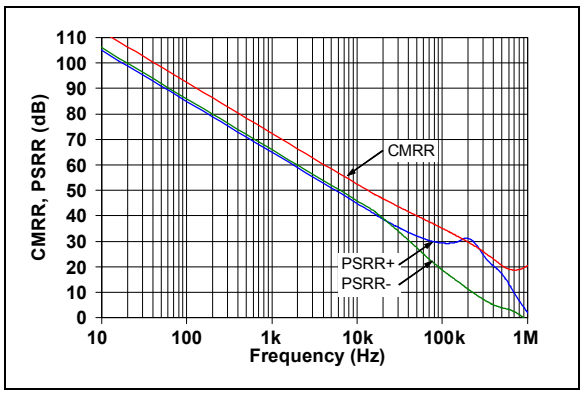


FIGURE 2-25: *CMRR and PSRR vs. Frequency.*

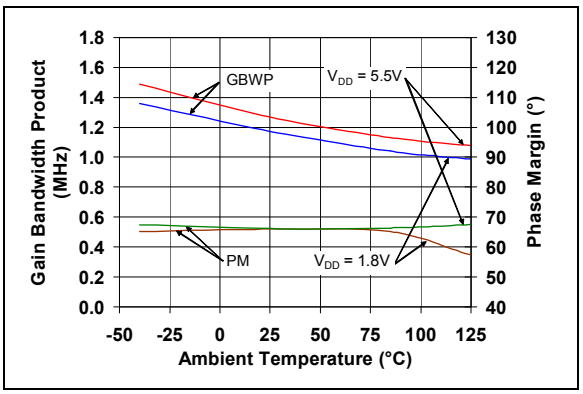


FIGURE 2-28: *Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

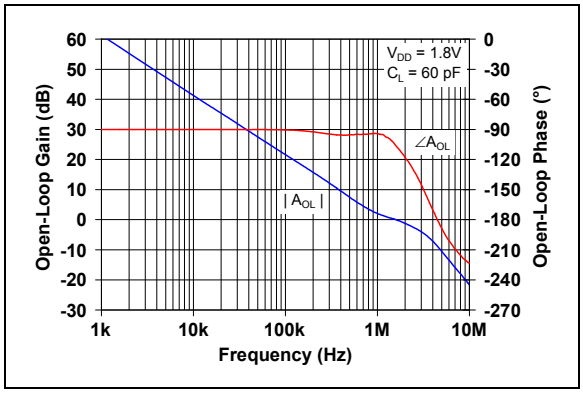


FIGURE 2-26: *Open-Loop Gain vs. Frequency with V_{DD} = 1.8V.*

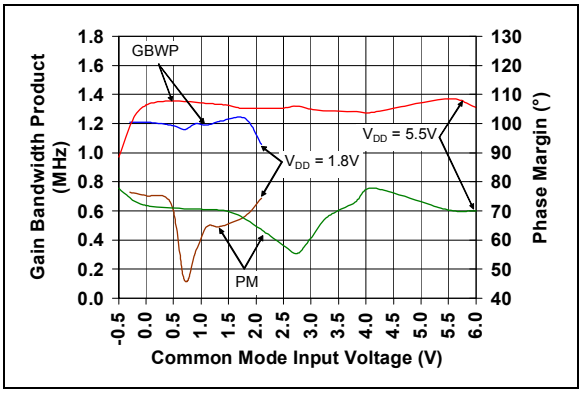


FIGURE 2-29: *Gain Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.*

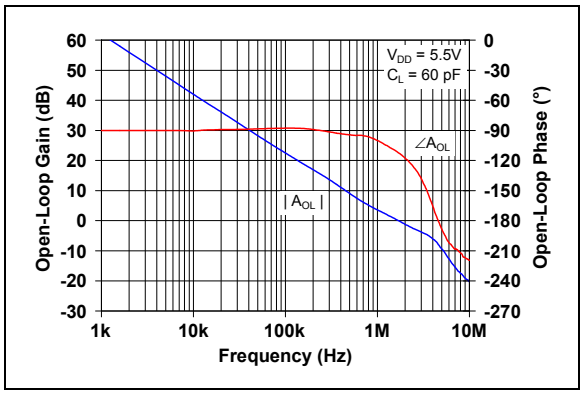


FIGURE 2-27: *Open-Loop Gain vs. Frequency with V_{DD} = 5.5V.*

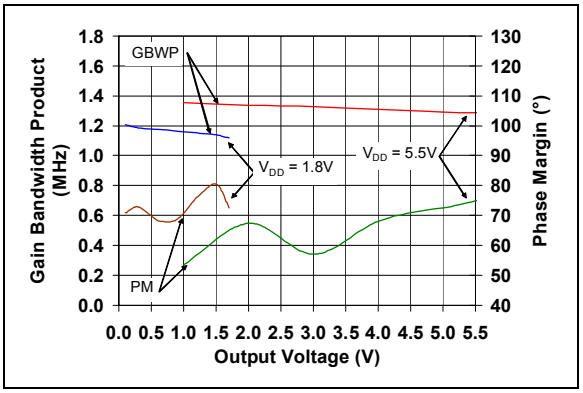


FIGURE 2-30: *Gain Bandwidth Product and Phase Margin vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

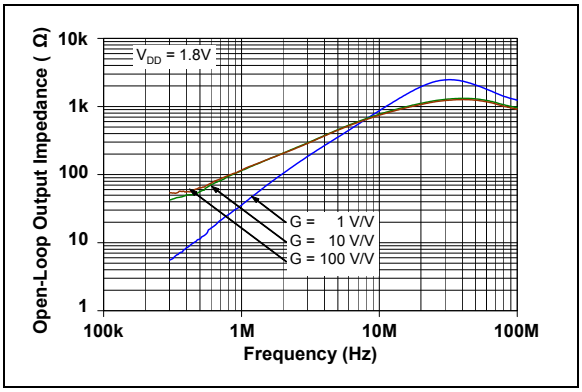


FIGURE 2-31: *Closed-Loop Output Impedance vs. Frequency with V_{DD} = 1.8V.*

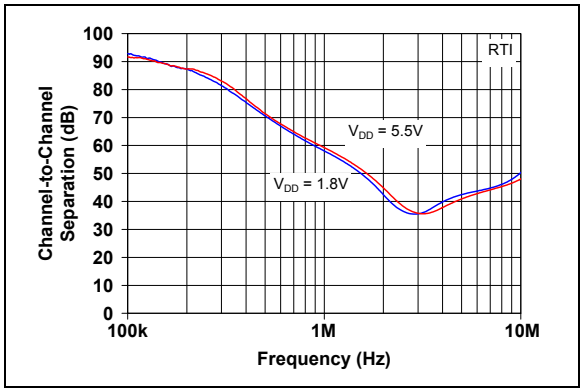


FIGURE 2-33: *Channel-to-Channel Separation vs. Frequency.*

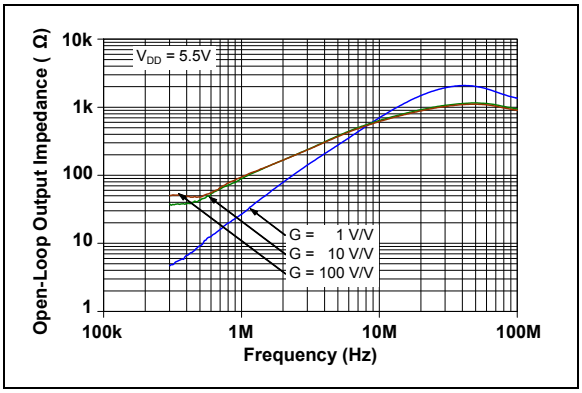


FIGURE 2-32: *Closed-Loop Output Impedance vs. Frequency with V_{DD} = 5.5V.*

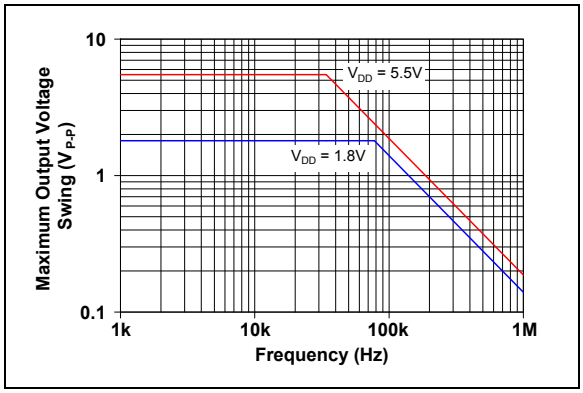


FIGURE 2-34: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.4 Input Noise and Distortion

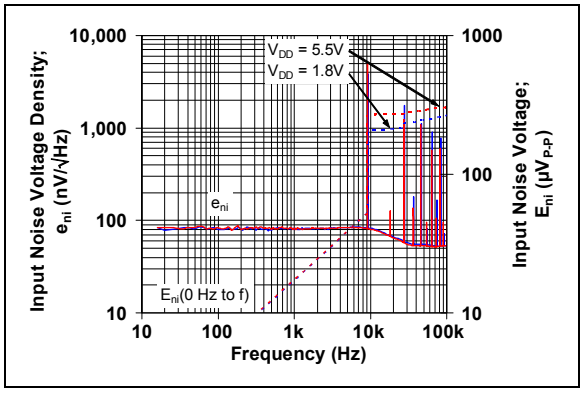


FIGURE 2-35: *Input Noise Voltage Density vs. Frequency.*

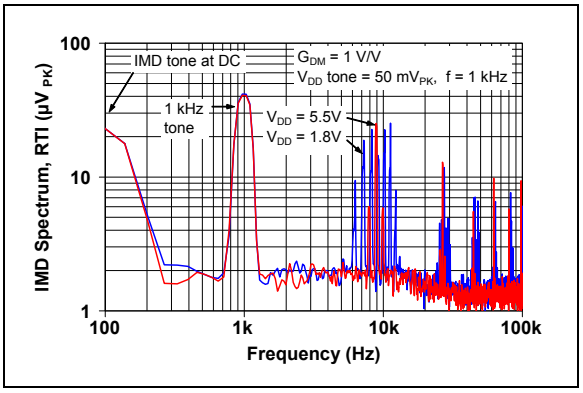


FIGURE 2-38: *Inter-Modulation Distortion vs. Frequency with V_{DD} Disturbance (see Figure 1-7).*

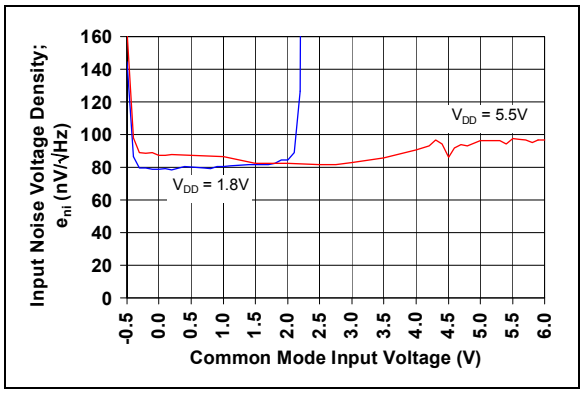


FIGURE 2-36: *Input Noise Voltage Density vs. Input Common Mode Voltage.*

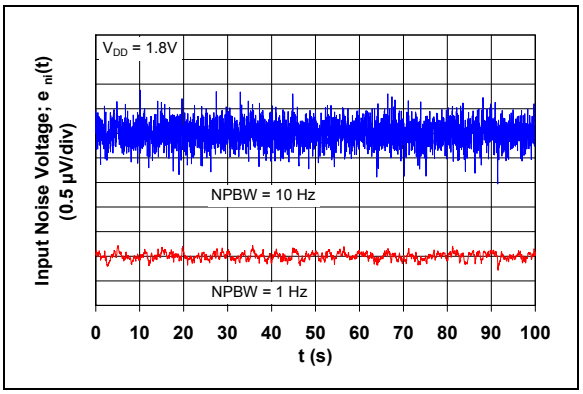


FIGURE 2-39: *Input Noise vs. Time with 1 Hz and 10 Hz Filters and V_{DD} =1.8V.*

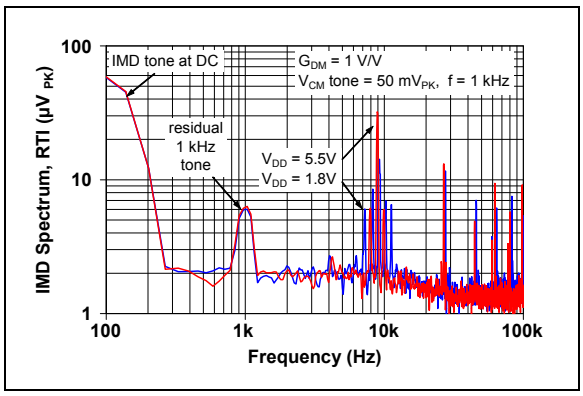


FIGURE 2-37: *Inter-Modulation Distortion vs. Frequency with V_{CM} Disturbance (see Figure 1-7).*

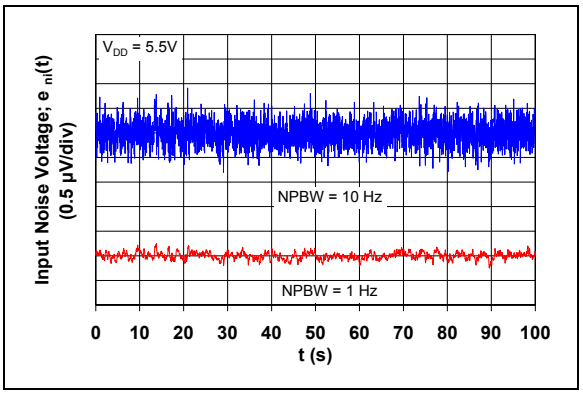


FIGURE 2-40: *Input Noise vs. Time with 1 Hz and 10 Hz Filters and V_{DD} =5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.5 Time Response

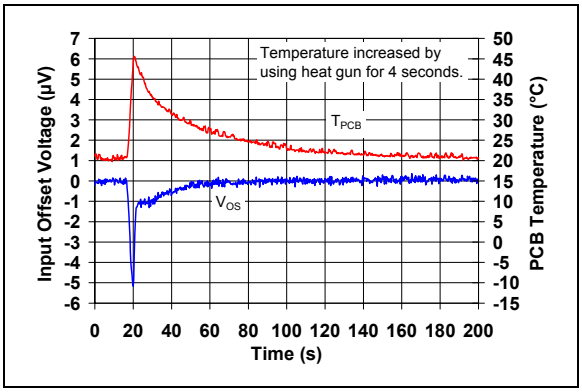


FIGURE 2-41: *Input Offset Voltage vs. Time with Temperature Change.*

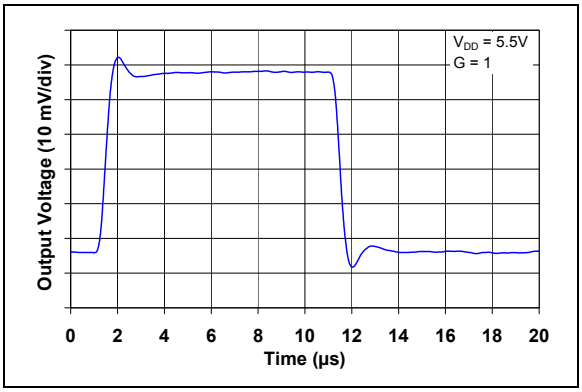


FIGURE 2-44: *Non-inverting Small Signal Step Response.*

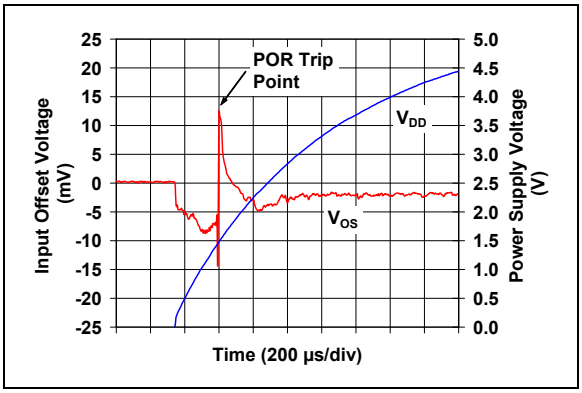


FIGURE 2-42: *Input Offset Voltage vs. Time at Power Up.*

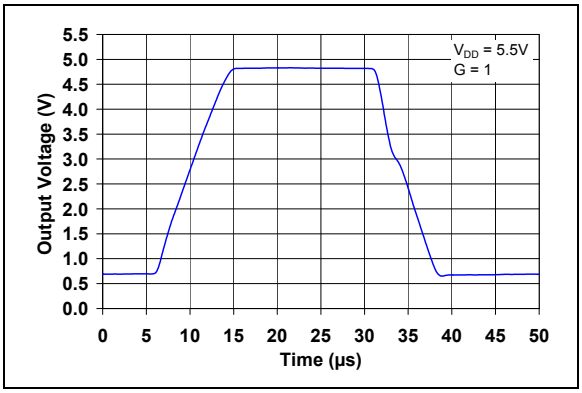


FIGURE 2-45: *Non-inverting Large Signal Step Response.*

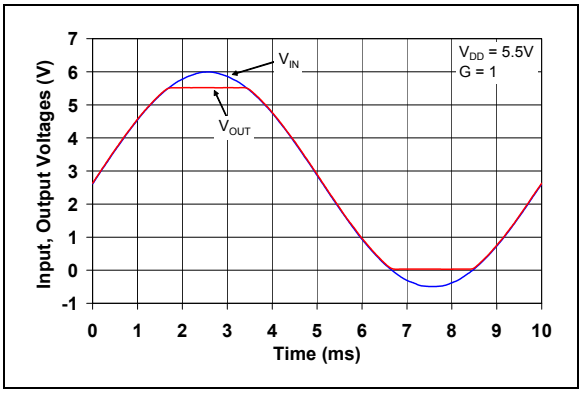


FIGURE 2-43: *The MCP6V06/7/8 family shows no input phase reversal with overdrive.*

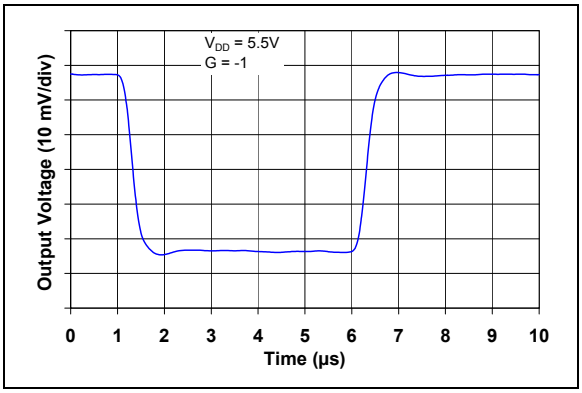


FIGURE 2-46: *Inverting Small Signal Step Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

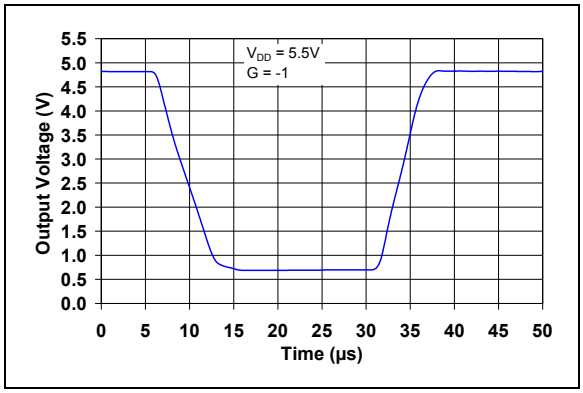


FIGURE 2-47: *Inverting Large Signal Step Response.*

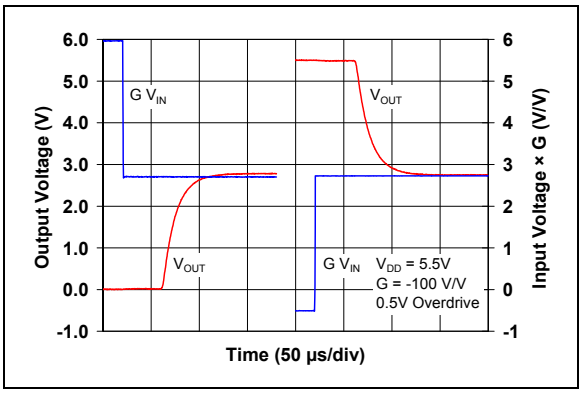


FIGURE 2-49: *Output Overdrive Recovery vs. Time with G = -100 V/V.*

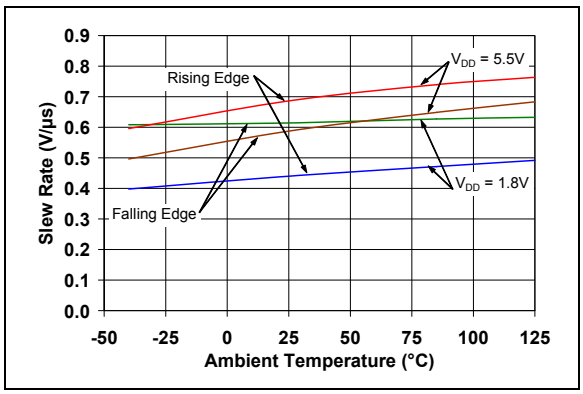


FIGURE 2-48: *Slew Rate vs. Ambient Temperature.*

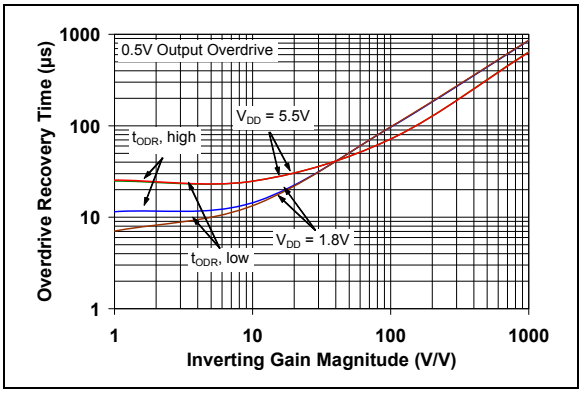


FIGURE 2-50: *Output Overdrive Recovery Time vs. Inverting Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.6 Chip Select Response (MCP6V08 only)

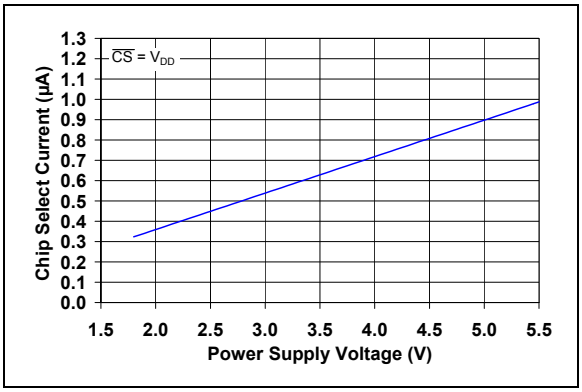


FIGURE 2-51: *Chip Select Current vs. Power Supply Voltage.*

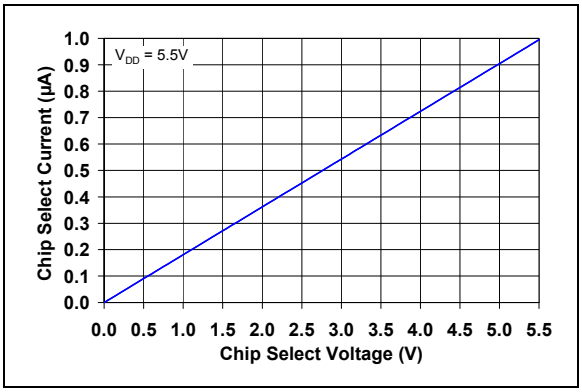


FIGURE 2-54: *Chip Select Current vs. Chip Select Voltage.*

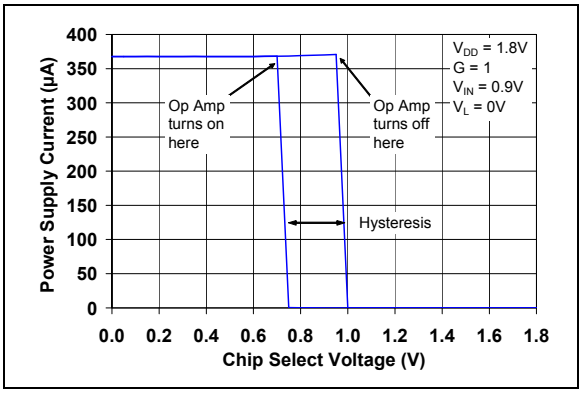


FIGURE 2-52: *Power Supply Current vs. Chip Select Voltage with V_{DD} = 1.8V.*

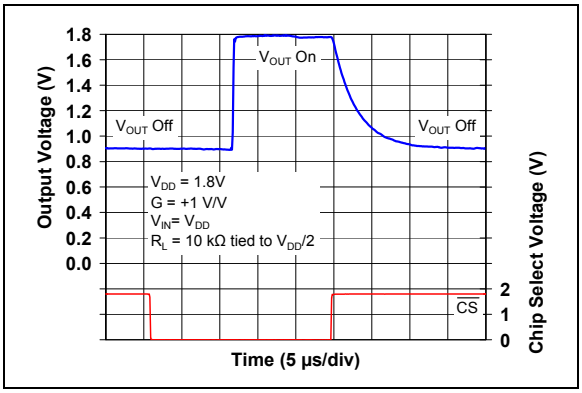


FIGURE 2-55: *Chip Select Voltage, Output Voltage vs. Time with V_{DD} = 1.8V.*

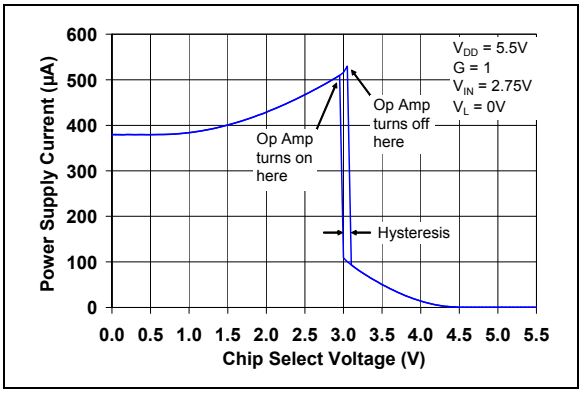


FIGURE 2-53: *Power Supply Current vs. Chip Select Voltage with V_{DD} = 5.5V.*

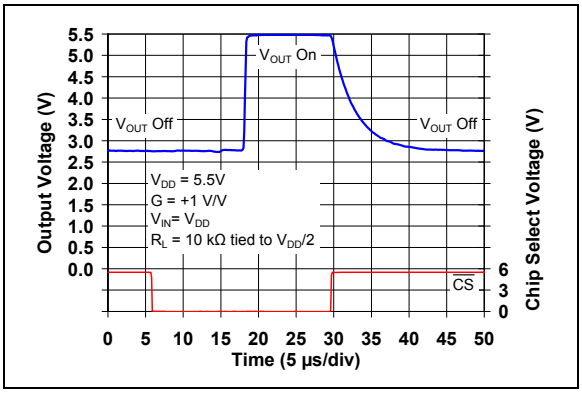


FIGURE 2-56: *Chip Select Voltage, Output Voltage vs. Time with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

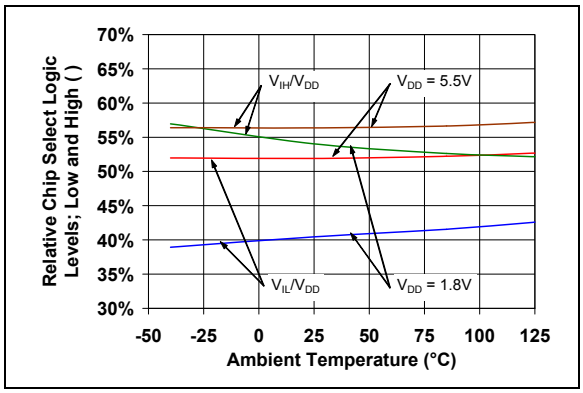


FIGURE 2-57: *Chip Select Relative Logic Thresholds vs. Ambient Temperature.*

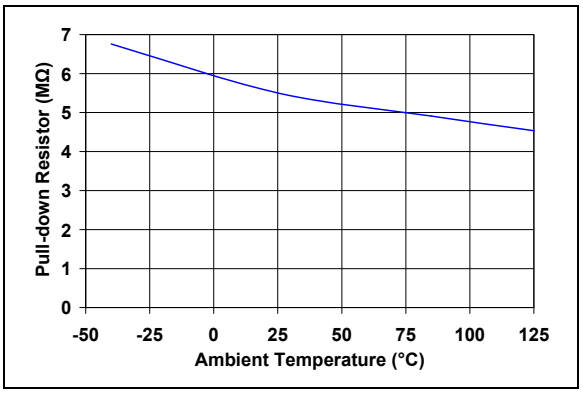


FIGURE 2-60: *Chip Select's Pull-down Resistor (R_{PD}) vs. Ambient Temperature.*

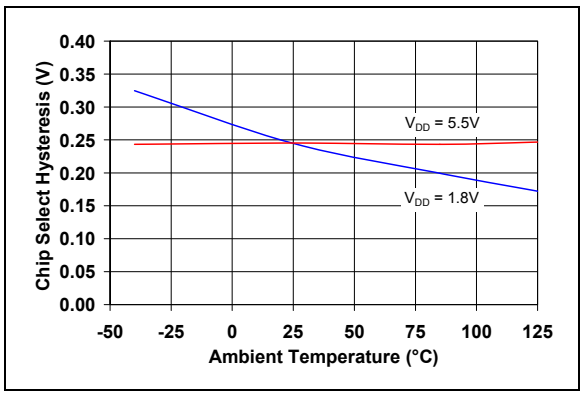


FIGURE 2-58: *Chip Select Hysteresis.*

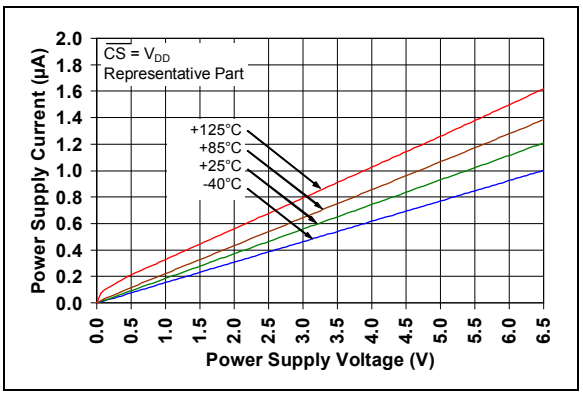


FIGURE 2-61: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

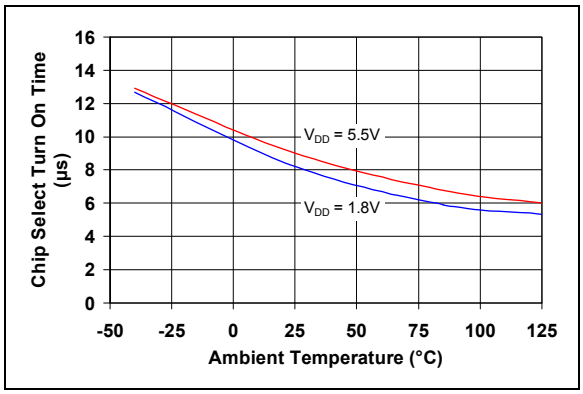


FIGURE 2-59: *Chip Select Turn On Time vs. Ambient Temperature.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6V06		MCP6V07		MCP6V08		Symbol	Description
TDFN	SOIC	DFN	SOIC	TDFN	SOIC		
6	6	1	1	6	6	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	2	2	2	2	V_{IN}–, V_{INA}–	Inverting Input (op amp A)
3	3	3	3	3	3	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
4	4	4	4	4	4	V_{SS}	Negative Power Supply
—	—	5	5	—	—	V_{INB}+	Non-inverting Input (op amp B)
—	—	6	6	—	—	V_{INB}–	Inverting Input (op amp B)
—	—	7	7	—	—	V_{OUTB}	Output (op amp B)
7	7	8	8	7	7	V_{DD}	Positive Power Supply
—	—	—	—	—	8	$\overline{CS}$	Chip Select (op amp A)
1, 5, 8	1, 5, 8	—	—	1, 5, 8	1, 5	NC	No Internal Connection
9	—	9	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs (V_{IN}+, V_{IN}–, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Chip Select ($\overline{CS}$) Digital Input

This pin ($\overline{CS}$) is a CMOS, Schmitt-triggered input that places the MCP6V08 op amps into a low power mode of operation.

3.5 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

NOTES:

4.0 APPLICATIONS

The MCP6V06/7/8 family of auto-zeroed op amps is manufactured using Microchip's state of the art CMOS process. It is designed for low cost, low power and high precision applications. Its low supply voltage, low quiescent current and wide bandwidth makes the MCP6V06/7/8 ideal for battery-powered applications.

4.1 Overview of Auto-zeroing Operation

Figure 4-1 shows a simplified diagram of the MCP6V06/7/8 auto-zeroed op amps. This will be used to explain how the DC voltage errors are reduced in this architecture.

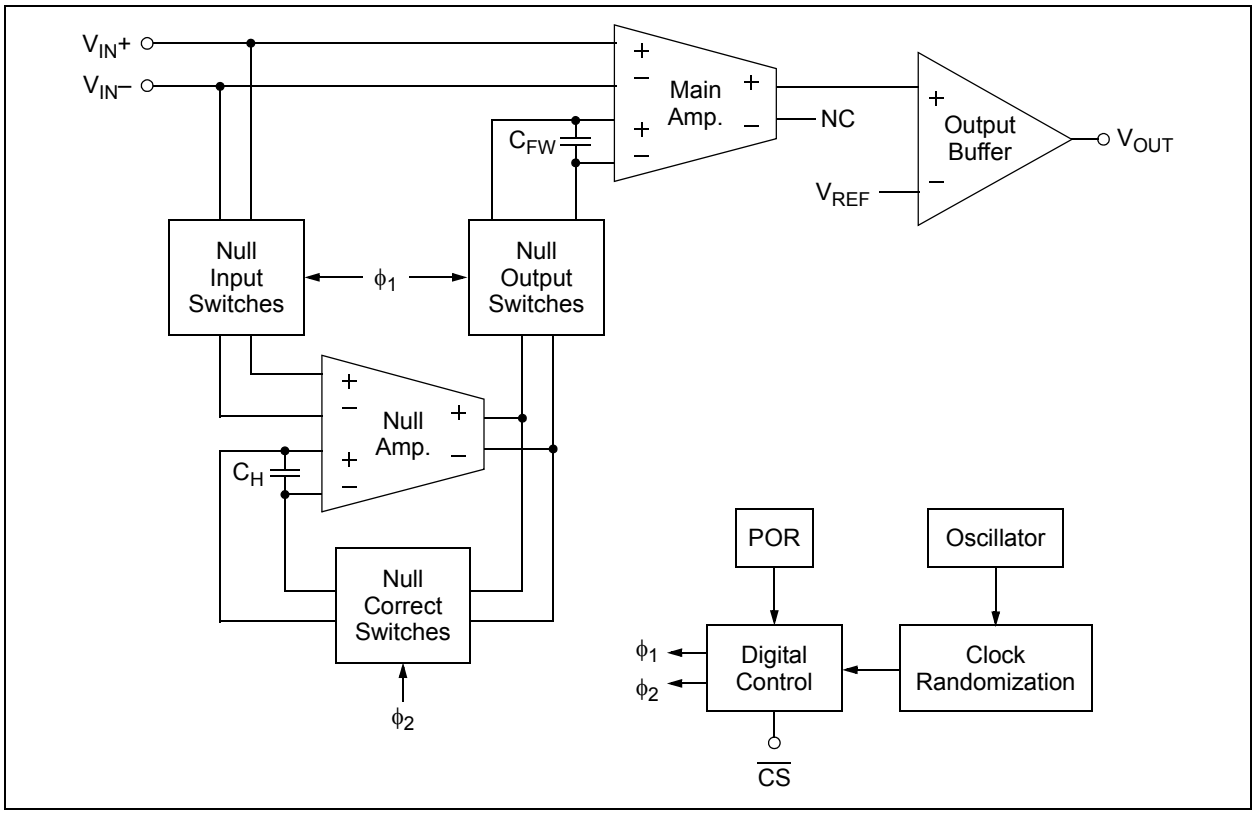


FIGURE 4-1: *Simplified Auto-zeroed Op Amp Functional Diagram.*

4.1.1 BUILDING BLOCKS

The Null Amp. and Main Amp. are designed for high gain and accuracy using a differential topology. They have an auxiliary input (bottom left) used for correcting the offset voltages. Both inputs are added together internally. The capacitors at the auxiliary inputs (C_{FW} and C_H) hold the corrected values during normal operation.

The Output Buffer is designed to drive external loads at the V_{OUT} pin. It also produces a single ended output voltage (V_{REF} is an internal reference voltage).

All of these switches are make-before-break in order to minimize glitch-induced errors. They are driven by two clock phases (ϕ_1 and ϕ_2) that select between normal mode and auto-zeroing mode.

The clock is derived from an internal R-C oscillator running at a rate of f_{OSC1} = 650 kHz. The oscillator's output is divided down to the desired rate. It is also randomized to minimize (spread) undesired clock tones in the output.

The internal POR ensures the part starts up in a known good state. It also provides protection against power supply brown out events.

The Chip Select input places the op amp in a low power state when it is high. When it goes low, it powers the op amp at its normal level and starts operation properly.

The Digital Control circuitry takes care of all of the housekeeping details of the switching operation. It also takes care of Chip Select and POR events.

4.1.2 AUTO-ZEROING ACTION

Figure 4-2 shows the connections between amplifiers during the Normal Mode of operation (ϕ_1). The hold capacitor (C_H) corrects the Null Amplifier's input offset. Since the Null Amplifier has very high gain, it dominates the signal seen by the Main Amplifier. This greatly reduces the impact of the Main Amplifier's input offset voltage on overall performance. Essentially, the Null Amplifier and Main Amplifier behave as a regular op amp with very high gain (A_{OL}) and very low offset voltage (V_{OS}).

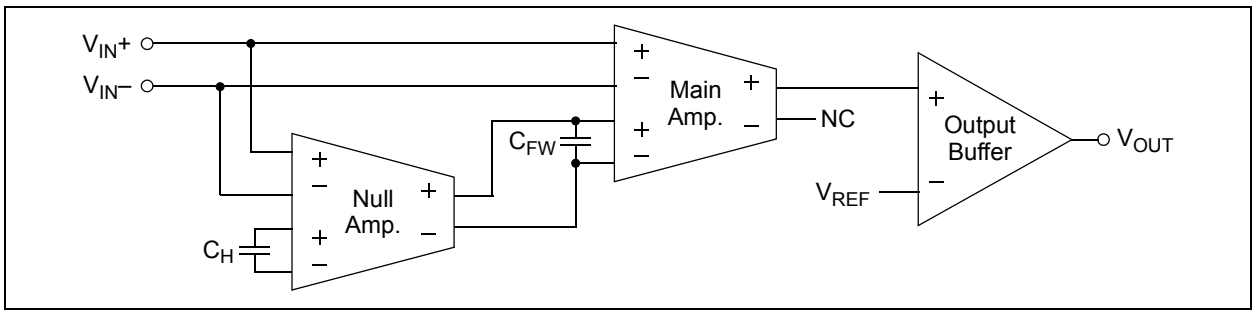


FIGURE 4-2: *Normal Mode of Operation (ϕ_1); Equivalent Amplifier Diagram.*

Figure 4-3 shows the connections between amplifiers during the Auto-zeroing Mode of operation (ϕ_2). The signal goes directly through the Main Amplifier, and the flywheel capacitor (C_{FW}) maintains a constant correction on the Main Amplifier's offset.

The Null Amplifier uses its own high open loop gain to drive the voltage across C_H to the point where its input offset voltage is almost zero. Because the principal input is connected to $V_{IN}+$, the auto-zeroing action corrects the offset at the current common mode input voltage (V_{CM}) and supply voltage (V_{DD}). This makes the DC CMRR and PSRR very high also.

Since these corrections happen every 50 µs, or so, we also minimize slow errors, including offset drift with temperature ($\Delta V_{OS}/\Delta T_A$), 1/f noise, and input offset aging.

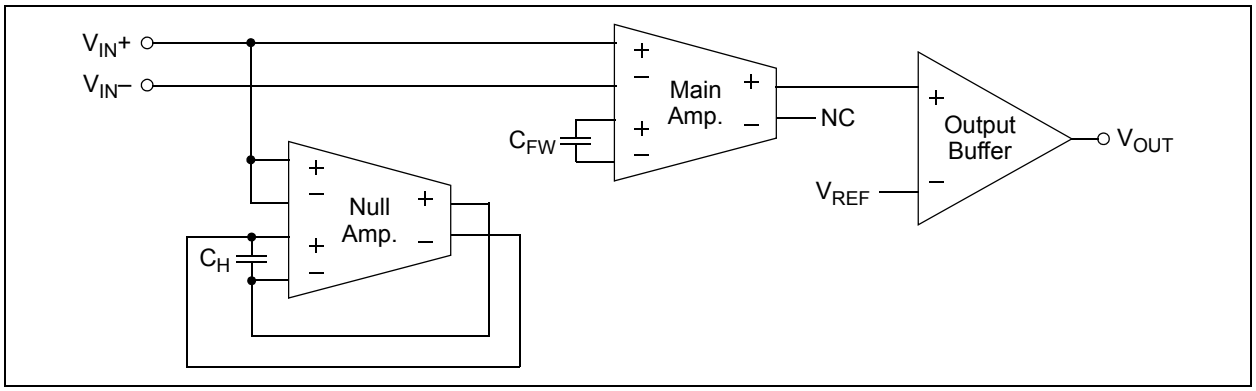


FIGURE 4-3: *Auto-zeroing Mode of Operation (ϕ_2); Equivalent Diagram.*

4.1.3 INTERMODULATION DISTORTION (IMD)

The MCP6V06/7/8 op amps will show intermodulation distortion (IMD), products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the auto-zeroing circuitry's non-linear response to produce IMD tones at sum and difference frequencies. IMD distortion tones are generated about all of the square wave clock's harmonics. See Figure 2-37 and Figure 2-38.

4.2 Other Functional Blocks

4.2.1 RAIL-TO-RAIL INPUTS

The input stage of the MCP6V06/7/8 op amps uses two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}, which is approximately equal to $V_{IN}+$ and $V_{IN}–$ in normal operation) and the other at high V_{CM}. With this topology, the input operates with V_{CM} up to 0.2V past either supply rail at +25°C (see Figure 2-18). The input offset voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.2V$ and $V_{DD} + 0.2V$ to ensure proper operation.

The transition between the input stages occurs when $V_{CM} \approx V_{DD} – 0.9V$ (see Figure 2-7 and Figure 2-8). For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-43 shows an input voltage exceeding both supplies with no phase inversion.

4.2.1.2 Input Voltage and Current Limits

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

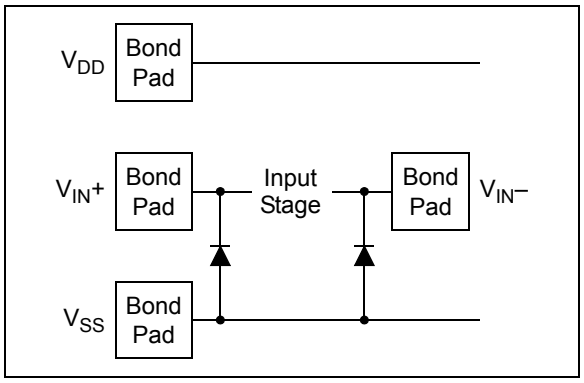


FIGURE 4-4: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). Figure 4-5 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

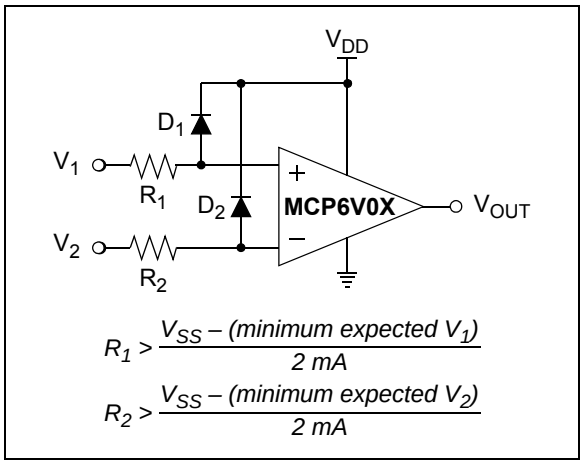


FIGURE 4-5: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}–$) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-17. Applications that are high impedance may need to limit the usable voltage range.

4.2.2 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V06/7/8 auto-zeroed op amps is $V_{DD} – 15$ mV (minimum) and $V_{SS} + 15$ mV (maximum) when $R_L = 20$ kΩ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figure 2-19 and Figure 2-20 for more information.

These op amps are designed to drive light loads; use another amplifier to buffer the output from heavy loads.

4.2.3 CHIP SELECT ($\overline{CS}$)

The single MCP6V08 has a Chip Select ($\overline{CS}$) pin. When $\overline{CS}$ is pulled high, the supply current for the corresponding op amp drops to about 1 µA (typical), and is pulled through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the internal pull-down resistor (about 5 MΩ) will keep the part on. Figure 1-4 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.3 Application Tips

4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1 gives both the linear and quadratic temperature coefficients (TC_1 and TC_2) of input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

EQUATION 4-1:

$$V_{OS}(T_A) = V_{OS} + TC_1\Delta T + TC_2\Delta T^2$$

Where:

ΔT	=	T_A – 25°C
$V_{OS}(T_A)$	=	input offset voltage at T_A
V_{OS}	=	input offset voltage at +25°C
TC_1	=	linear temperature coefficient
TC_2	=	quadratic temperature coefficient

4.3.2 DC GAIN PLOTS

Figure 2-9, Figure 2-10 and Figure 2-11 are histograms of the reciprocals (in units of µV/V) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).

The $1/A_{OL}$ histogram is centered near 0 µV/V because the measurements are dominated by the op amp's input noise. The negative values shown represent noise, *not* unstable behavior. We validate the op amps' stability by making multiple measurements of V_{OS}; instability would manifest itself as a greater unexplained variability in V_{OS} or as the railing of the output.

4.3.3 SOURCE RESISTANCES

The input bias currents have two significant components; switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

4.3.4 SOURCE CAPACITANCE

The capacitances seen by the two inputs should be small and matched. The internal switches connected to the inputs dump charges on these capacitors; an offset can be created if the capacitances do not match.

4.3.5 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These auto-zeroed op amps have a different output impedance than most op amps, due to their unique topology.

When driving a capacitive load with these op amps, a series resistor at the output (R_{ISO} in Figure 4-6) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

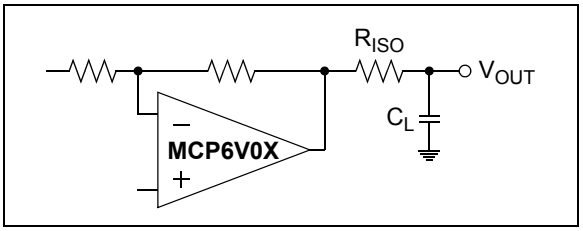


FIGURE 4-6: *Output Resistor, R_{ISO}, Stabilizes Capacitive Loads.*

Figure 4-7 gives recommended R_{ISO} values for different capacitive loads and is independent of the gain.

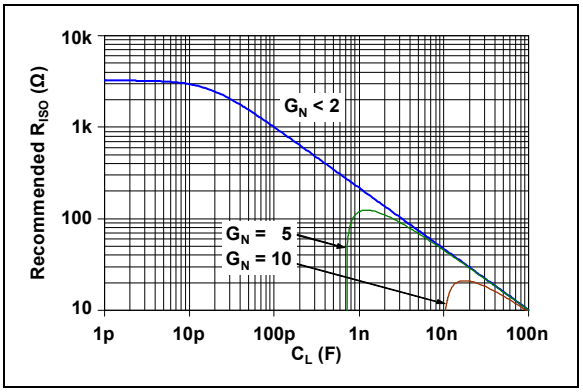


FIGURE 4-7: *Recommended R_{ISO} values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6V06 SPICE macro model (good for all of the MCP6V06/7/8 op amps) are helpful.

4.3.6 STABILIZING OUTPUT LOADS

This family of auto-zeroed op amps has an output impedance (Figure 2-31 and Figure 2-32) that has a double zero when the gain is low. This can cause a large phase shift in feedback networks that have low resistance near the part's bandwidth. This large phase shift can cause stability problems.

Figure 4-8 shows one circuit example that has low resistance near the part's bandwidth. R_F and C_F set a pole at 0.16 kHz, so the noise gain (G_N) is 1 V/V at the circuit's bandwidth (roughly 1.3 MHz). The load seen by the op amp's output at 1.3 MHz is $R_G||R_L$ (99Ω). This is low enough to be a real concern.

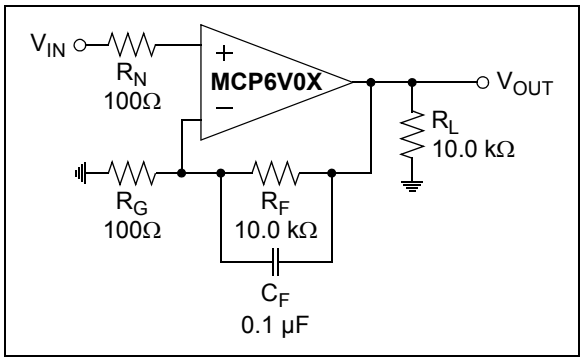


FIGURE 4-8: *Output Load Issue.*

To solve this problem, increase the resistive load to at least 3 kΩ. Methods to accomplish this task include:

- Increase R_G
- Remove C_F (relocate the filter)
- Add a 3 kΩ resistor at the op amp's output that is not in the signal path; see Figure 4-9

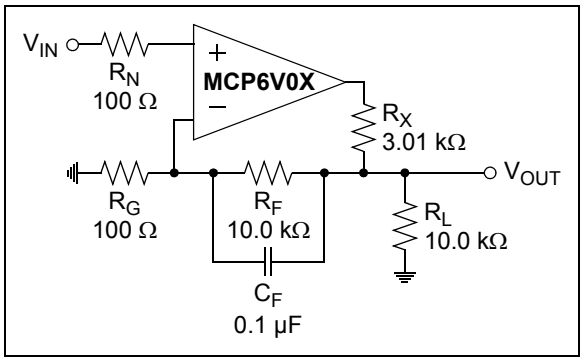


FIGURE 4-9: *One Solution To Output Load Issue.*

4.3.7 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low bandwidth signal filters:
  - Minimizes random analog noise
  - Reduces interfering signals
- Good PCB layout techniques:
  - Minimizes crosstalk
  - Minimizes parasitic capacitances and inductances that interact with fast switching edges
- Good power supply design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

4.3.8 SUPPLY BYPASSING AND FILTERING

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm of the pin for good high-frequency performance.

These parts also need a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other low noise, analog parts.

Additional filtering of high frequency power supply noise (e.g., switched mode power supplies) can be achieved using resistors. The resistors need to be small enough to prevent a large drop in V_{DD} for the op amp, which would cause a reduced output range and possible load-induced power supply noise. The resistors also need to be large enough to dissipate little power when V_{DD} is turned on and off quickly. The circuit in Figure 4-10 gives good rejection out to 1 MHz for switched mode power supplies. Smaller resistors and capacitors are a better choice for designs where the power supply is reasonably quiet.

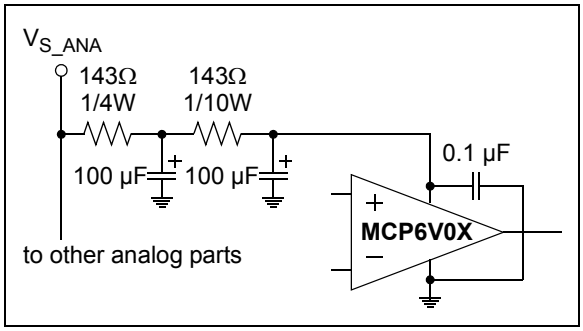


FIGURE 4-10: *Additional Supply Filtering.*

4.3.9 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of ±1 µV, many physical errors need to be minimized. The design of the Printed Circuit Board (PCB), the wiring, and the thermal environment has a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6V06/7/8 op amps minimum and maximum specifications.

4.3.9.1 Thermo-junctions

Any time two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (the Seebeck or thermo-junction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermo-junctions on a PCB:

- Components (resistors, op amps, …) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermo-junctions have temperature to voltage conversion coefficients of 10 to 100 µV/°C (sometimes higher).

There are three basic approaches to minimizing thermo-junction effects:

- Minimize thermal gradients
- Cancel thermo-junction voltages
- Minimize difference in thermal potential between metals

4.3.9.2 Non-inverting and Inverting Amplifier Layout for Thermo-junctions

Figure 4-11 shows the recommended non-inverting and inverting gain amplifier circuits on one schematic. Usually, to minimize the input bias current related offset, R_1 is chosen to be $R_2||R_3$.

The guard traces (with ground vias at the ends) help minimize the thermal gradients. The resistor layout cancels the resistor thermal voltages, assuming the temperature gradient is constant near the resistors:

EQUATION 4-2:

$$V_{OUT} \approx V_P G_P, \quad V_M = GND$$
$$\approx -V_M G_M, \quad V_P = GND$$

Where:

G_M = R_3/R_2, inverting gain magnitude

G_P = $1 + G_M$, non-inverting gain magnitude

V_{OS} is neglected

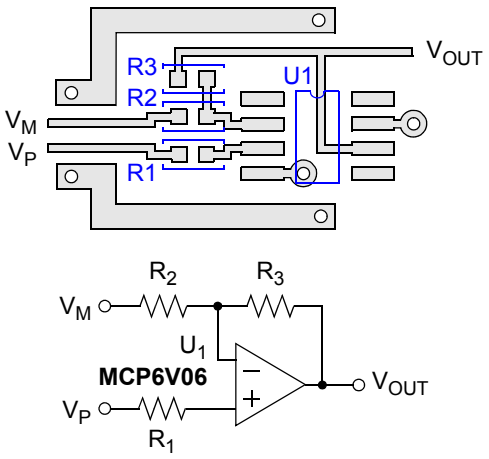


FIGURE 4-11: *PCB Layout and Schematic for Single Non-inverting and Inverting Amplifiers.*

Note: Changing the orientation of the resistors will usually cause a significant decrease in the cancellation of the thermal voltages.

4.3.9.3 Difference Amplifier Layout for Thermo-junctions

Figure 4-12 shows the recommended difference amplifier circuit. Usually, we choose $R_1 = R_2$ and $R_3 = R_4$.

The guard traces (with ground vias at the ends) help minimize the thermal gradients. The resistor layout cancels the resistor thermal voltages, assuming the temperature gradient is constant near the resistors:

EQUATION 4-3:

$$V_{OUT} \approx V_{REF} + (V_P - V_M)G_{DM}$$

Where:

Thermal voltages are approximately equal

G_{DM} = $R_3/R_1 = R_4/R_2$, difference gain

V_{OS} is neglected

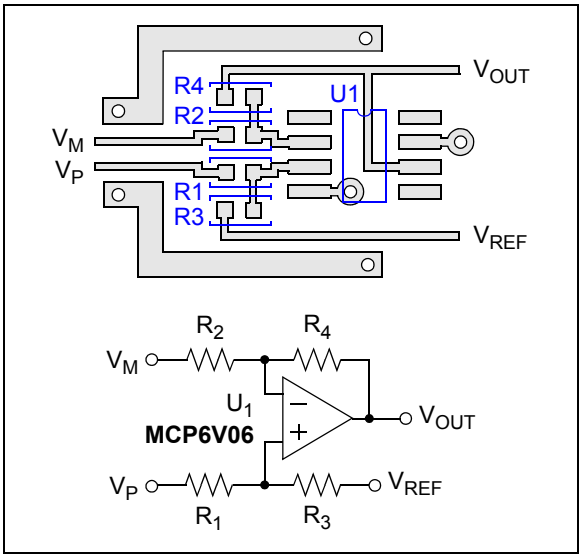


FIGURE 4-12: *PCB Layout and Schematic for Single Difference Amplifier.*

Note:	Changing the orientation of the resistors will usually cause a significant decrease in the cancellation of the thermal voltages.

4.3.9.4 Dual Non-inverting Amplifier Layout for Thermo-junctions

The dual op amp amplifiers shown in Figure 4-16 and Figure 4-17 produce a non-inverting difference gain greater than 1, and a common mode gain of 1 .They can use the layout shown in Figure 4-13. The gain setting resistors (R_2) between the two sides are not combined so that the thermal voltages can be canceled.

The guard traces (with ground vias at the ends) help minimize the thermal gradients. The resistor layout cancels the resistor thermal voltages, assuming the temperature gradient is constant near the resistors:

EQUATION 4-4:

$$(V_{OA} - V_{OB}) \approx (V_{IA} - V_{IB})G_{DM}$$
$$(V_{OA} + V_{OB})/2 \approx (V_{IA} + V_{IB})/2$$

Where:

Thermal voltages are approximately equal

G_{DM} = $1 + R_3/R_2$, differential mode gain

G_{CM} = 1, common mode gain

V_{OS} is neglected

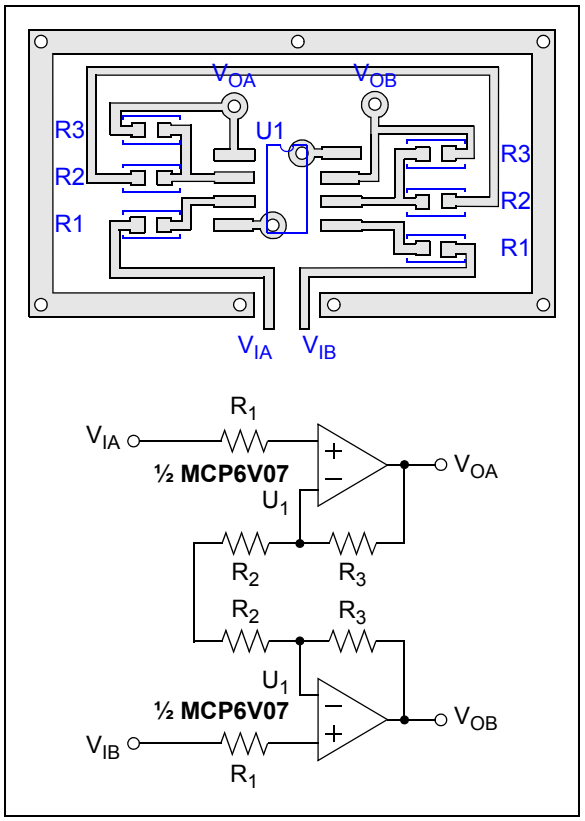


FIGURE 4-13: *PCB Layout and Schematic for Dual Non-inverting Amplifier.*

Note:	Changing the orientation of the resistors will usually cause a significant decrease in the cancellation of the thermal voltages.

4.3.9.5 Other PCB Thermal Design Tips

In cases where an individual resistor needs to have its thermo-junction voltage cancelled, it can be split into two equal resistors as shown in Figure 4-14. To keep the thermal gradients near the resistors as small as possible, the layouts are symmetrical with a ring of metal around the outside. Make $R_{1A} = R_{1B} = R_1/2$ and $R_{2A} = R_{2B} = 2R_2$.

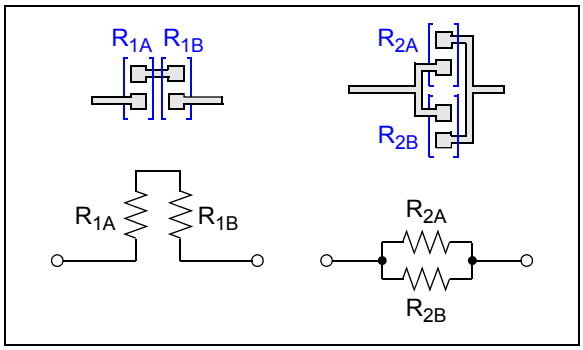


FIGURE 4-14: *PCB Layout for Individual Resistors.*

Note:	Changing the orientation of the resistors will usually cause a significant decrease in the cancellation of the thermal voltages.

Minimize temperature gradients at critical components (resistors, op amps, heat sources, etc.):

- Minimize exposure to gradients
  - Small components
  - Tight spacing
  - Shield from air currents
- Align with constant temperature (contour) lines
  - Place on PCB center line
- Minimize magnitude of gradients
  - Select parts with lower power dissipation
  - Use same metal junctions on thermo-junctions that need to match
  - Use metal junctions with low temperature to voltage coefficients
  - Large distance from heat sources
  - Ground plane underneath (large area)
  - FR4 gaps (no copper for thermal insulation)
  - Series resistors inserted into traces (adds thermal and electrical resistance)
  - Use heat sinks

Make the temperature gradient point in one direction:

- Add guard traces
  - Constant temperature curves follow the traces
  - Connect to ground plane
- Shape any FR4 gaps
  - Constant temperature curves follow the edges

4.3.9.6 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources, can also affect the DC performance. Non-linear distortion can convert these signals to multiple tones, included a DC shift in voltage. When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding (e.g., encapsulant)
- Use ground plane (at least a star ground)
- Place the input signal source near to the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these auto-zeroed op amps

4.3.9.7 Miscellaneous Effects

Keep the resistances seen by the input pins as small and as near to equal as possible to minimize bias current related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center or (the tribo-electric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as ceramic) to output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electro-chemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

4.4 Typical Applications

4.4.1 WHEATSTONE BRIDGE

Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples. These signals can be small and the common mode noise large. Amplifier designs with high differential gain are desirable.

Figure 4-15 shows how to interface to a Wheatstone bridge with a minimum of components. Because the circuit is not symmetric, the ADC input is single ended, and there is a minimum of filtering, the CMRR is good enough for moderate common mode noise.

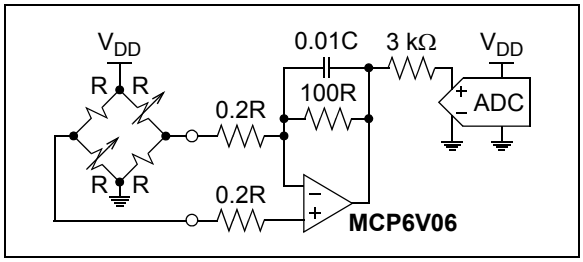


FIGURE 4-15: *Simple Design.*

Figure 4-16 shows a higher performance circuit for Wheatstone bridges. This circuit is symmetric and has high CMRR. Using a differential input to the ADC helps with the CMRR.

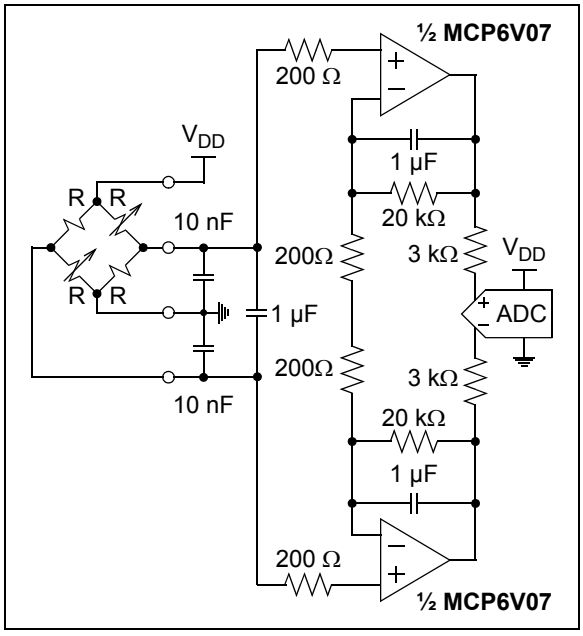


FIGURE 4-16: *High Performance Design.*

4.4.2 RTD SENSOR

The ratiometric circuit in Figure 4-17 conditions a three wire RTD. It corrects for the sensor's wiring resistance by subtracting the voltage across the middle R_W. The top R1 does not change the output voltage; it balances the op amp inputs. Failure (open) of the RTD is detected by an out-of-range voltage.

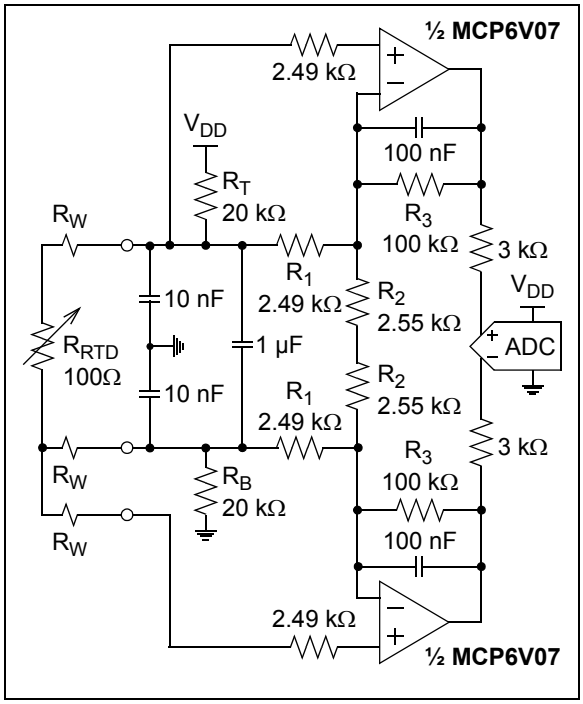


FIGURE 4-17: *RTD Sensor.*

The voltages at the input of the ADC can be calculated with the following:

$$G_{RTD} = 1 + 2 \cdot R_3 / R_2$$
$$G_W = G_{RTD} - R_3 / R_1$$
$$V_{DM} = G_{RTD}(V_T - V_B) + G_W V_W$$
$$V_{CM} = \frac{V_T + V_B + (G_{RTD} + 1 - G_W)V_W}{2}$$

Where:

V_T	=	Voltage at the top of R_{RTD}
V_B	=	Voltage at the bottom of R_{RTD}
V_W	=	Voltage across top and middle R_W's
V_{CM}	=	ADC's common mode input
V_{DM}	=	ADC's differential mode input

4.4.3 THERMOCOUPLE SENSOR

Figure 4-18 shows a simplified diagram of an amplifier and temperature sensor used in a thermocouple application. The type K thermocouple senses the temperature at the hot junction (T_{HJ}), and produces a voltage at V_1 proportional to T_{HJ} (in °C). The amplifier's gain is is set so that V_4/T_{HJ} is 10 mV/°C. V_3 represents the output of a temperature sensor, which produces a voltage proportional to the temperature (in °C) at the cold junction (T_{CJ}), and with a 0.50V offset. V_2 is set so that V_4 is 0.50V when $T_{HJ} - T_{CJ}$ is 0°C.

EQUATION 4-5:

$$V_1 \approx T_{HJ}(40\ \mu V/°C)$$
$$V_2 = (1.00V)$$
$$V_3 = T_{CJ}(10\ mV/°C) + (0.50V)$$
$$V_4 = 250V_1 + (V_2 - V_3)$$
$$\approx (10\ mV/°C)\ (T_{HJ} - T_{CJ}) + (0.50V)$$

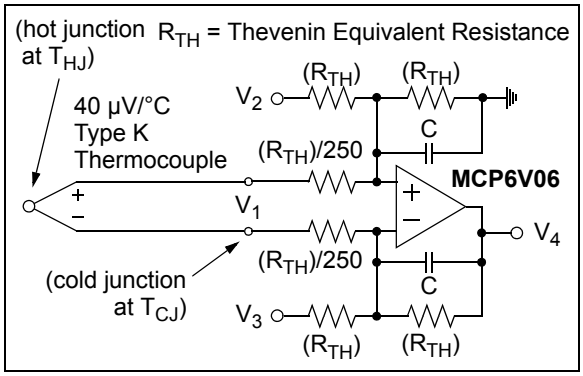


FIGURE 4-18: *Thermocouple Sensor; Simplified Circuit.*

Figure 4-19 shows a more complete implementation of this circuit. The dashed red arrow indicates a thermally conductive connection between the thermocouple and the MCP9700A; it needs to be very short and have low thermal resistance.

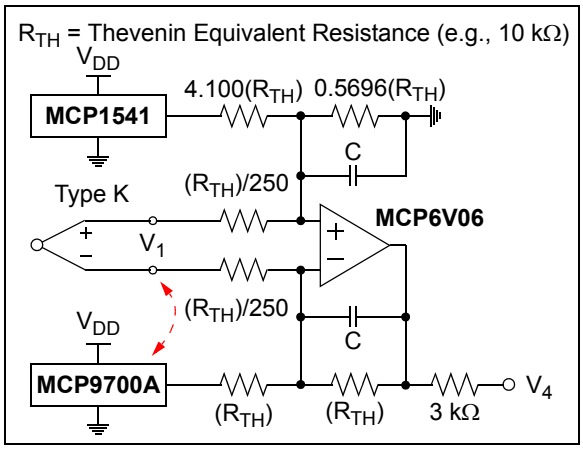


FIGURE 4-19: *Thermocouple Sensor.*

The MCP9700A senses the temperature at its physical location. It needs to be at the same temperature as the cold junction (T_{CJ}), and produces V_3 (Figure 4-16).

The MCP1541 produces a 4.10V output, assuming V_{DD} is at 5.0V. This voltage, tied to a resistor ladder of 4.100(R_{TH}) and 1.3224(R_{TH}), would produce a Thevenin equivalent of 1.00V and 250(R_{TH}). The 1.3224(R_{TH}) resistor is combined in parallel with the top right R_{TH} resistor (in Figure 4-18), producing the 0.5696(R_{TH}) resistor.

V_4 should be converted to digital, then corrected for the thermocouple's non-linearity. The ADC can use the MCP1541 as its voltage reference. Alternately, an absolute reference inside a PICmicro® can be used instead of the MCP1541.

4.4.4 OFFSET VOLTAGE CORRECTION

Figure 4-20 shows a MCP6V06 correcting the input offset voltage of another op amp. R_2 and C_2 integrate the offset error seen at the other op amp's input; the integration needs to be slow enough to be stable (with the feedback provided by R_1 and R_3).

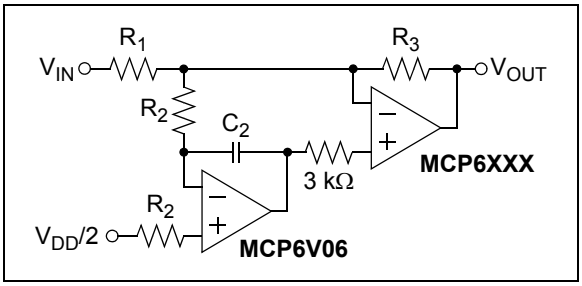


FIGURE 4-20: *Offset Correction.*

4.4.5 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter's performance. Do not use MCP6V06/7/8 as a comparator by itself; the V_{OS} correction circuitry does not operate properly without a feedback loop.

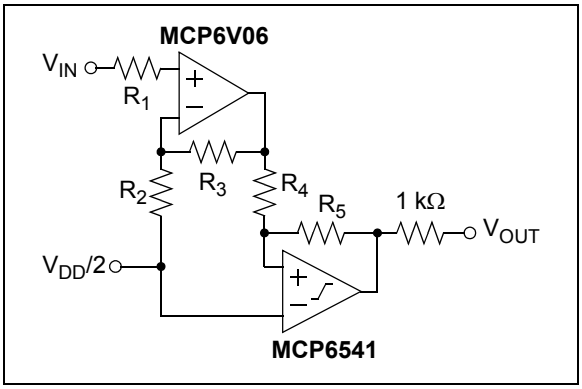


FIGURE 4-21: *Precision Comparator.*

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6V06/7/8 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6V06/7/8 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the Filter-Lab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, and simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

Some boards that are especially useful are:

- MCP6V01 Thermocouple Auto-Zeroed Reference Design
- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- P/N SOIC8EV: 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board
- P/N SOIC14EV: 14-Pin SOIC/TSSOP/DIP Evaluation Board

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications"*, DS00722

AN723: *"Operational Amplifier AC Specifications and Applications"*, DS00723

AN884: *"Driving Capacitive Loads With Op Amps"*, DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990

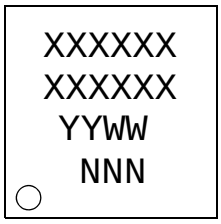
These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

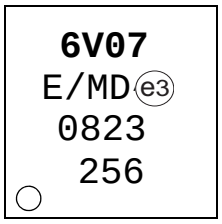
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

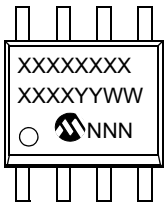
8-Lead DFN (4x4) **(MCP6V07)**



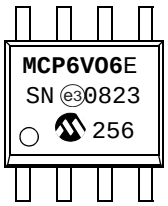
Example



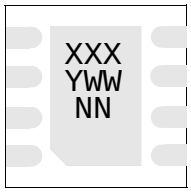
8-Lead SOIC (150 mil)



Example:



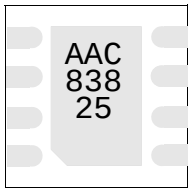
8-Lead TDFN (2x3) **(MCP6V06, MCP6V08)**



Device	Code
MCP6V06	AAC
MCP6V08	AAD

Note: Applies to 8-Lead 2x3 TDFN

Example:

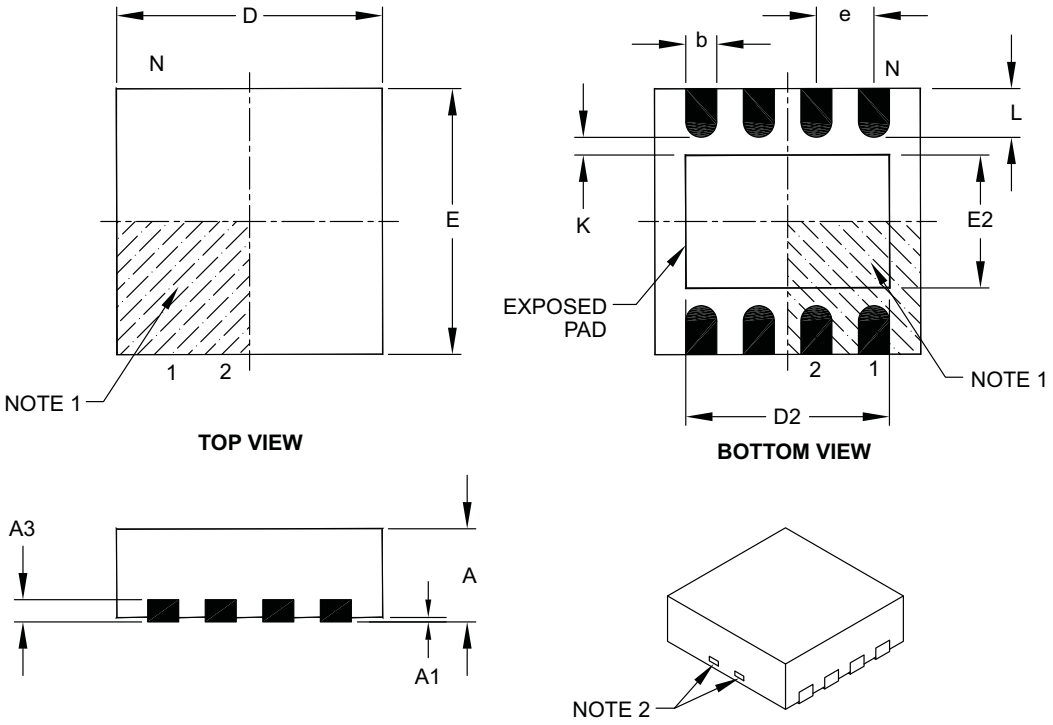


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

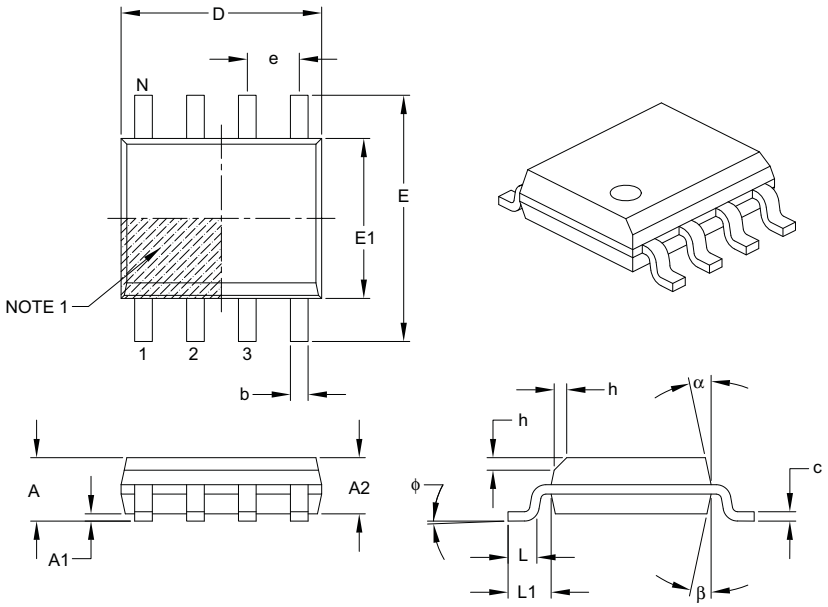
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

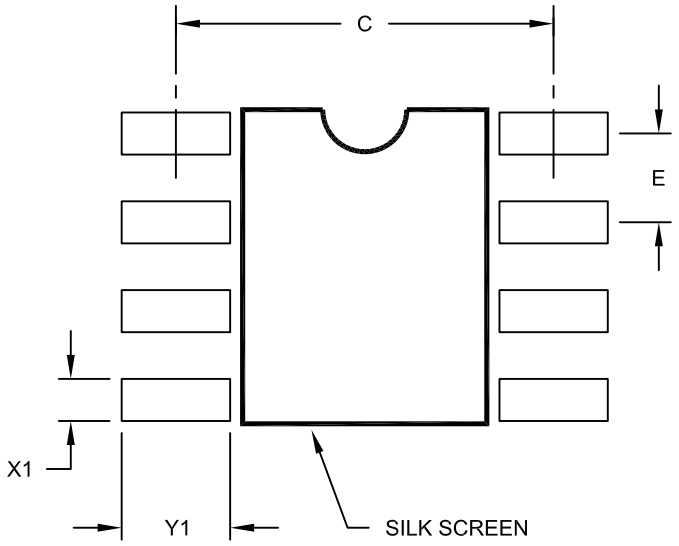
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

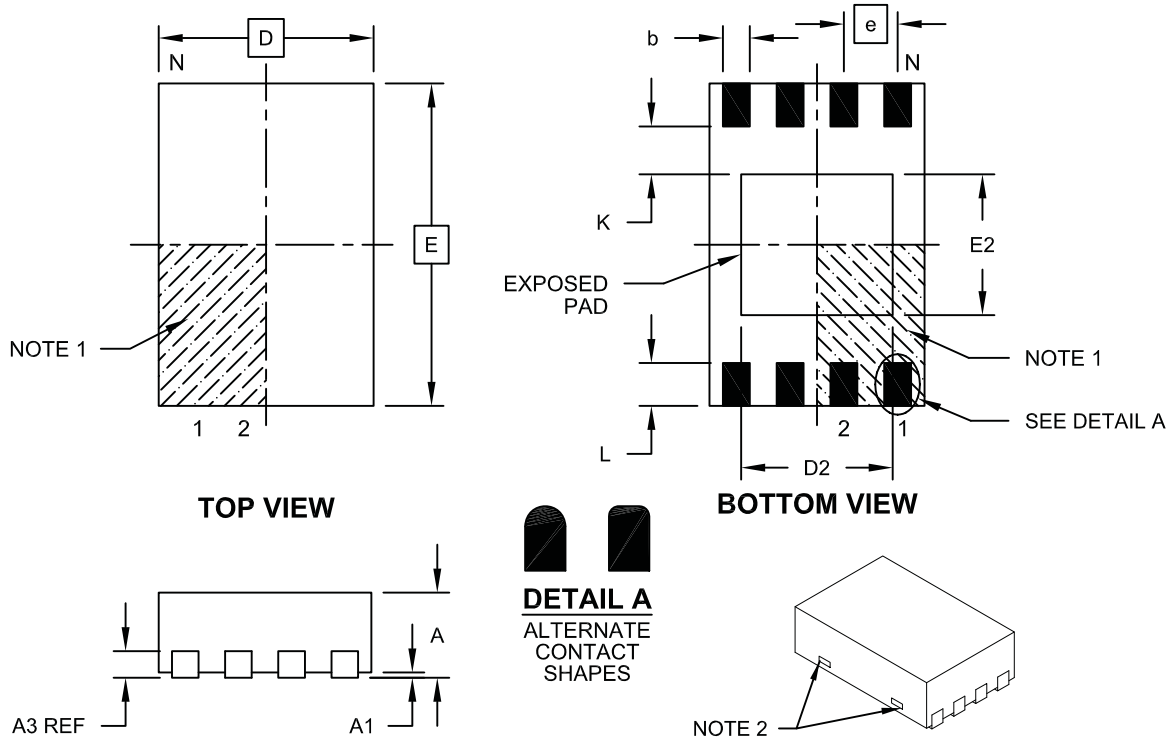
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

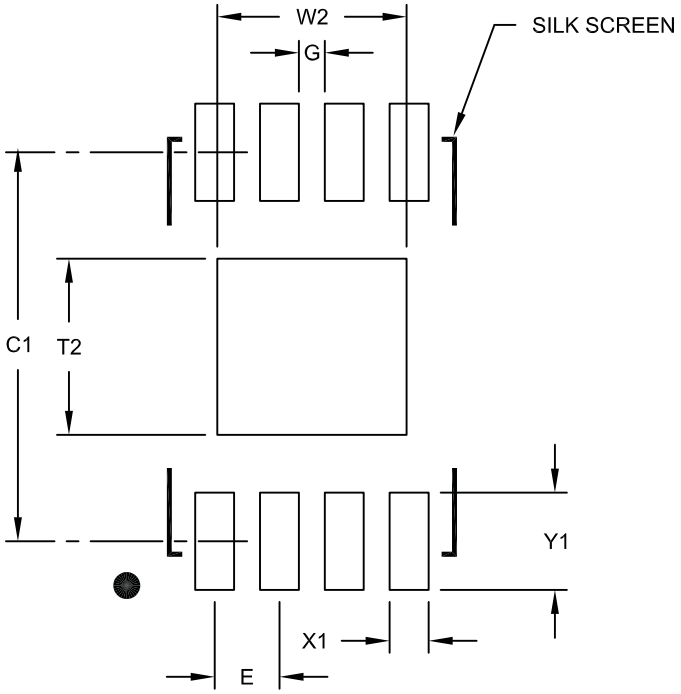
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (December 2008)

The following is the list of modifications:

1. Added the 8-lead, 2x3 TDFN package for the MCP6V01 and MCP6V03 devices.
2. Added 8-lead, 2x3 TDFN package information to Thermal Characteristic table.
3. Added information on the Exposed Thermal Pad (EP) for the 8-lead, 2x3 TDFN and 8-lead, 4x4 DFN packages.
4. Added **Section 4.3.6 "Stabilizing Output Loads"**.
5. Other minor typographical corrections.

Revision A (June 2008)

- Original Release of this Document.

APPENDIX B: OFFSET RELATED TEST SCREENS

Input offset voltage related specifications in the DC spec table (Table 1-1) are based on bench measurements (see **Section 2.1 "DC Input Precision"**). These measurements are much more accurate because:

- More compact circuit
- Soldered parts on the PCB
- More time spent averaging (reduces noise)
- Better temperature control
  - Reduced temperature gradients
  - Greater accuracy

We use production screens to ensure the quality of our outgoing products. These screens are set at wider limits to eliminate any fliers; see Table B-1.

TABLE B-1: OFFSET RELATED TEST SCREENS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Max	Units	Conditions
Input Offset					
Input Offset Voltage	V_{OS}	-10	+10	µV	T_A = +25°C **(Note 1, Note 2)**
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC_1	—	—	nV/°C	T_A = -40 to +125°C **(Note 3)**
Power Supply Rejection	PSRR	115	—	dB	**(Note 1)**
Common Mode					
Common Mode Rejection	CMRR	106	—	dB	V_{DD} = 1.8V, V_{CM} = -0.2V to 2.0V **(Note 1)**
	CMRR	116	—	dB	V_{DD} = 5.5V, V_{CM} = -0.2V to 5.7V **(Note 1)**
Open-Loop Gain					
DC Open-Loop Gain (large signal)	A_{OL}	114	—	dB	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V **(Note 1)**
	A_{OL}	122	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V **(Note 1)**

Note 1: Due to thermal junctions and other errors in the production environment, these specifications are only screened in production.

2: V_{OS} is also sample screened at +125°C.

3: TC_1 is not measured in production.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XXX
Device	Temperature Range	Package

Device:	MCP6V06	Single Op Amp
	MCP6V06T	Single Op Amp (Tape and Reel for 2x3 TDFN and SOIC)
	MCP6V07	Dual Op Amp
	MCP6V07T	Dual Op Amp (Tape and Reel for 4×4 DFN and SOIC)
	MCP6V08	Single Op Amp with Chip Select
	MCP6V08T	Single Op Amp with Chip Select (Tape and Reel for SOIC)
Temperature Range:	E =	-40°C to +125°C
Package:	MD =	Plastic Dual Flat, No-Lead (4×4x0.9 mm), 8-lead (MCP6V07 only)
	MNY * =	Plastic Dual Flat, No-Lead (2×3x0.75 mm), 8-lead (MCP6V06, MCP6V08)
	SN =	Plastic SOIC (150mil Body), 8-lead

* Y = nickel palladium gold manufacturing designator. Only available on the TDFN package.

Examples:

a) MCP6V06T-E/SN: Extended temperature, 8LD SOIC package.

b) MCP6V06-E/MNY: Extended temperature, 8LD 2x3 TDFN package.

a) MCP6V07-E/MD: Extended temperature, 8LD 4x4 DFN package..

b) MCP6V07T-E/SN: Tape and Reel, Extended temperature, 8LD SOIC package.

a) MCP6V08-E/SN: Extended temperature, 8LD SOIC package.

b) MCP6V08-E/MNY: Extended temperature, 8LD 2x3 TDFN package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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