



**9-BIT LATCHED  
TTL-TO-ECL**

**SY10H602  
SY100H602**

**FEATURES**

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with MC10H/100H602
- Available in 28-pin PLCC package

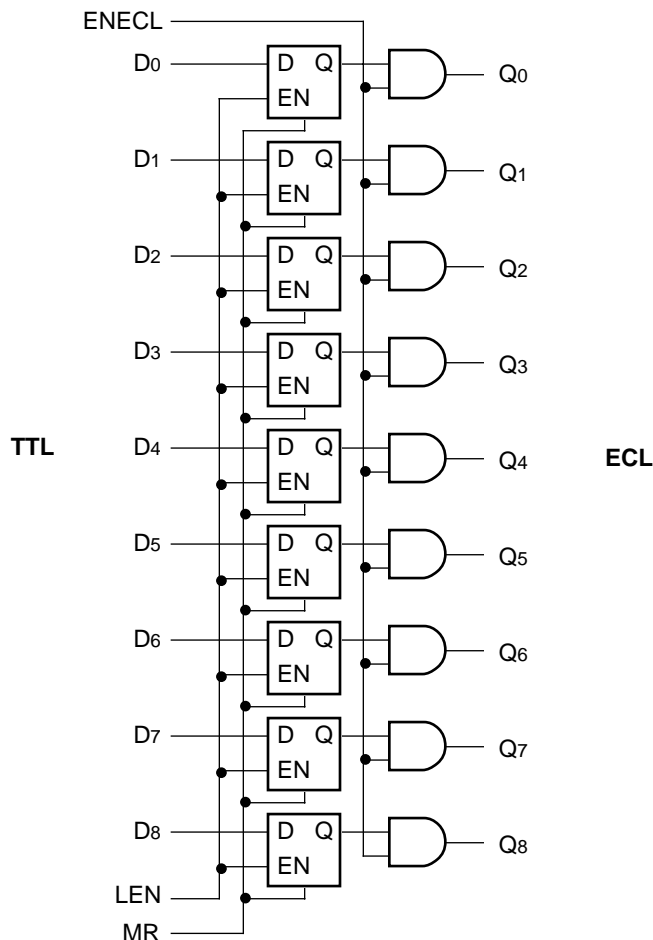
**DESCRIPTION**

The SY10/100H602 are 9-bit, dual supply TTL-to-ECL translators with latches. Devices in the Micrel 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

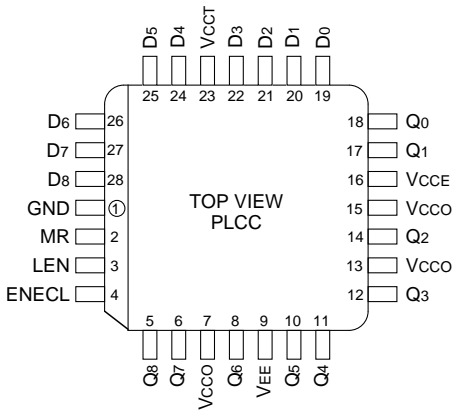
**BLOCK DIAGRAM**



**PIN NAMES**

Pin	Function
GND	TTL Ground (0V)
V <sub>CCE</sub>	ECL V <sub>cc</sub> (0V)
V <sub>CCO</sub>	ECL V <sub>cc</sub> (0V) — Outputs
V <sub>CCT</sub>	TTL Supply (+5.0V)
V <sub>EE</sub>	ECL Supply (-5.2/-4.5V)
D <sub>0</sub> -D <sub>8</sub>	Data Inputs (TTL)
Q <sub>0</sub> -Q <sub>8</sub>	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10H602JC	J28-1	Commercial	SY10H602JC	Sn-Pb
SY10H602JCTR <sup>(2)</sup>	J28-1	Commercial	SY10H602JC	Sn-Pb
SY100H602JC	J28-1	Commercial	SY100H602JC	Sn-Pb
SY100H602JCTR <sup>(2)</sup>	J28-1	Commercial	SY100H602JC	Sn-Pb
SY10H602JZ <sup>(3)</sup>	J28-1	Commercial	SY10H602JZ with Pb-Free bar-line indicator	Matte-Sn
SY10H602JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10H602JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H602JZ <sup>(3)</sup>	J28-1	Commercial	SY100H602JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H602JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100H602JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**TRUTH TABLE**

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q <sub>0</sub>
X	X	H	H	L
X	X	X	L	L

**DC ELECTRICAL CHARACTERISTICS**

VCCT = 5.0V ± 10%; VEE = -4.75V to -5.5V (10H Version); VEE = -4.2V to -5.5V (100H Version)

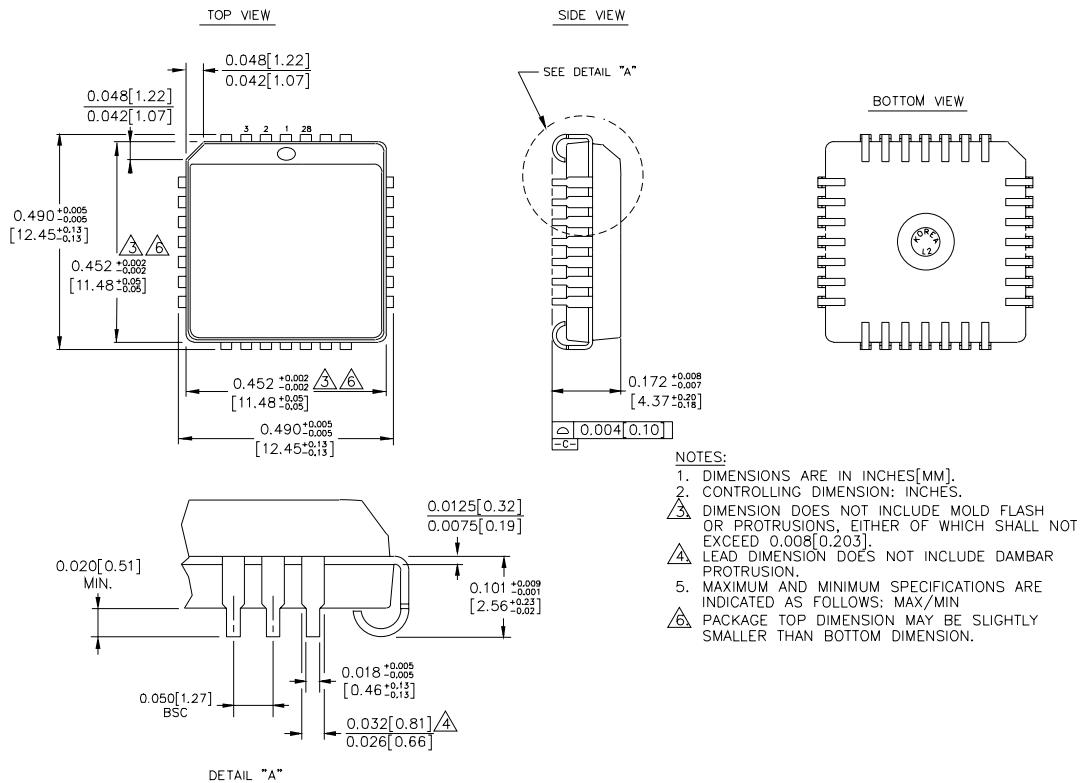
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
IEE	Power Supply Current, ECL 10H 100H	—	125	—	125	—	125	mA	—
		—	122	—	123	—	132		
ICCH ICCL	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
		—	50	—	50	—	50		

**AC ELECTRICAL CHARACTERISTICS**

VCCT = 5.0V ± 10%; VEE = -4.75V to -5.5V (10H Version); VEE = -4.2V to -5.5V (100H Version)

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PD</sub>	Propagation Delay to Output D	1.4	3.0	1.5	3.2	1.7	3.5	ns	—
	LEN	2.0	3.4	2.1	3.5	2.4	3.7		
	MR	2.0	3.4	2.1	3.5	2.5	3.9		
	ENECL	1.6	3.2	1.7	3.3	1.8	3.7		
t <sub>S</sub>	Set-up Time, D to LEN	2.0	—	2.0	—	2.0	—	ns	—
t <sub>H</sub>	Hold Time, D to LEN	1.0	—	1.0	—	1.0	—	ns	—
t <sub>w(L)</sub>	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—	ns	—
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Time 20% to 80%, 80% to 20%	0.5	1.5	0.5	1.5	0.5	1.5	ns	—

**28-PIN PLCC (J28-1)**



Rev. 03

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