USB7216

6-Port USB 3.1 Gen 2 Type-C® Controller Hub

Highlights

- 6-Port USB Smart Hub with:
  - Native USB Gen 2 Type-C® support on downstream port 1
  - Three Standard USB 3.1 Gen 2 downstream ports
  - Two Standard USB 2.0 downstream ports
  - Internal Hub Feature Controller device which enables:
    - USB to I^2C/SPI/I^2S/GPIO bridge endpoint support
    - USB to internal hub register write and read
- USB Link Power Management (LPM) support
- USB-IF Battery Charger revision 1.2 support on downstream ports (DCP, CDP, SDP)
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 100-pin (12mm x 12mm) VQFN RoHS compliant package
- Commercial and industrial grade temperature support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 2 Peripherals

Key Benefits

- USB 3.1 Gen 2 compliant 10 Gbps, 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
  - 5V tolerant USB 2.0 pins
  - 1.21V tolerant USB 3.1 Gen 2 pins
  - Integrated termination and pull-up/down resistors
- Native USB Type-C Support
  - Type-C CC Pin with integrated Rp and Rd resistors
  - Integrated multiplexer on USB Type-C enabled ports. USB 3.1 Gen 2 PHYs are disabled until a valid Type-C attach is detected, saving idle power.
  - Control for external VCONN supply

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- Supports battery charging of most popular battery powered devices on all ports
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006/2009 charger emulation
  - European Union universal mobile charger support
  - Supports additional portable devices
- On-chip Microcontroller
  - manages I/Os, VBUS, and other signals
- 96kB RAM, 256kB ROM
- 8kB One-Time-Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI external memory, or SMBus
- **FlexConnect**
  - The roles of the upstream and all downstream ports are reversible on command
- **Multi-Host Endpoint Reflector**
  - Integrated host-controller endpoint reflector via CDC/NCM device class for automotive applications
- **USB Bridging**
  - USB to I^2C, SPI, I^2S, and GPIO
- **PortSwap**
  - Configurable USB 2.0 differential pair signal swap
- **PHYBoost**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense**
  - Programmable USB receive sensitivity
- **USB Power Delivery Billboard Device Support**
  - Internal port can enumerate as a Power Delivery Billboard device to communicate Power Delivery Alternate Mode negotiation failure cases to host
- Compatible with Microsoft Windows 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- 100-pin VQFN package (12mm x 12mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DFP	Downstream Facing Port
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UFP	Upstream Facing Port
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.
A	Analog.
P	Power pin.

1.3 Reference Documents

1. *Universal Serial Bus Revision 3.1 Specification*, http://www.usb.org
2. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
3. *I²C-Bus Specification*, Version 1.1, http://www.nxp.com/documents/user_manual/UM10204.pdf
4. *I²S-Bus Specification*, https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

Note:	Additional USB7216 resources can be found on the Microchip USB7216 product page at www.microchip.com/USB7216.

2.0 INTRODUCTION

2.1 General Description

The Microchip USB7216 hub is a low-power, OEM configurable, USB 3.1 Gen 2 hub controller with 6 downstream ports and advanced features for embedded USB applications. The USB7216 is fully compliant with the Universal Serial Bus Revision 3.1 Specification and USB 2.0 Link Power Management Addendum. The USB7216 supports 10 Gbps SuperSpeed+ (SS+), 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on four standard USB 3.1 Gen 2 downstream ports and only legacy speeds (HS/FS/LS) on two standard USB 2.0 downstream ports.

The USB7216 is a standard USB 3.1 Gen 2 hub that supports native basic Type-C with integrated CC logic on downstream port 1. The downstream Type-C port includes an internal USB 3.1 Gen 2 multiplexer; no external multiplexer is required for Type-C support.

The USB7216 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of seven generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 controller, decoupling the 10/5 Gbps SS+/SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB7216 enables OEMs to configure their system using "Configuration Straps." These straps simplify the configuration process assigning default values to USB 3.1 Gen 2 ports and GPIOs. OEMs can disable ports, enable battery charging and define GPIO functions as default assignments on power up removing the need for OTP or external SPI ROM.

The USB7216 supports downstream battery charging. The USB7216 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB7216 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A[USB 2.0]/0.9A[USB 3.1] with data)

Additionally, the USB7216 includes many powerful and unique features such as:

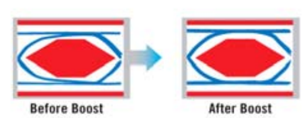
The Hub Feature Controller, an internal USB device dedicated for use as a USB to I^2C/SPI/GPIO interface that allows external circuits or devices to be monitored, controlled, or configured via the USB interface.

Multi-Host Endpoint Reflector, which provides unique USB functionality whereby USB data can be "mirrored" between two USB hosts (Multi-Host) in order to perform a single USB transaction.This capability is fully covered by Microchip intellectual property (U.S. Pat. Nos. 7,523,243 and 7,627,708) and is instrumental in enabling Apple CarPlay™, where the Apple iPhone® becomes a USB Host.

FlexConnect, which provides flexible connectivity options. One of the USB7216's downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



VariSense, which controls the Hi-Speed USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

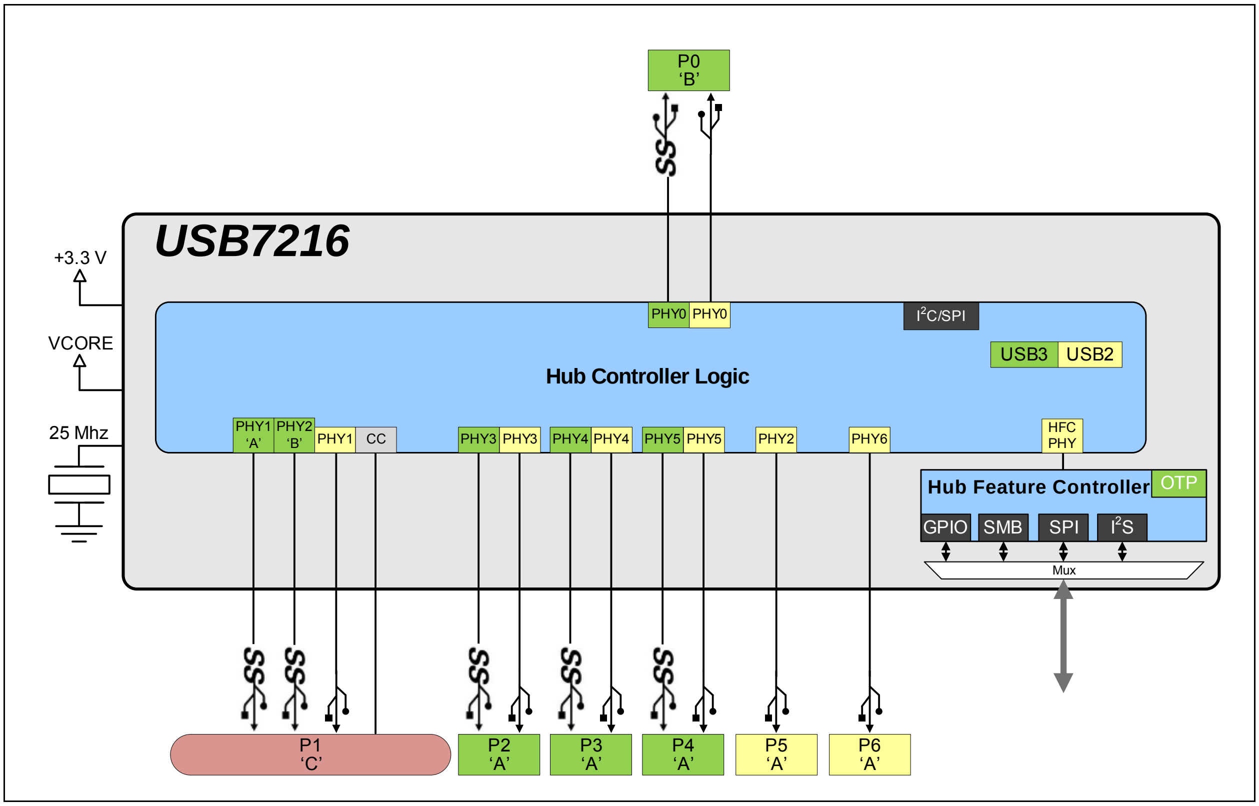
Port Split, which allows for the USB 3.1 Gen 2 and USB 2.0 portions of downstream ports 2, 3, and 4 in Configuration 1 and downstream port 4 (only) in Configuration 2 to operate independently and enumerate two separate devices in parallel in special applications.

USB Power Delivery Billboard Device, which allows an internal device to enumerate as a Billboard class device when a Power Delivery Alternate Mode negotiation has failed. The Billboard device will enumerate temporarily to the host PC when a failure occurs, as indicated by a digital signal from an external Power Delivery controller.

The USB7216 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility and are available as GPIOs for customer specific use.

The USB7216 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range. An internal block diagram of the USB7216 in an upstream Type-B application is shown in Figure 2-1.

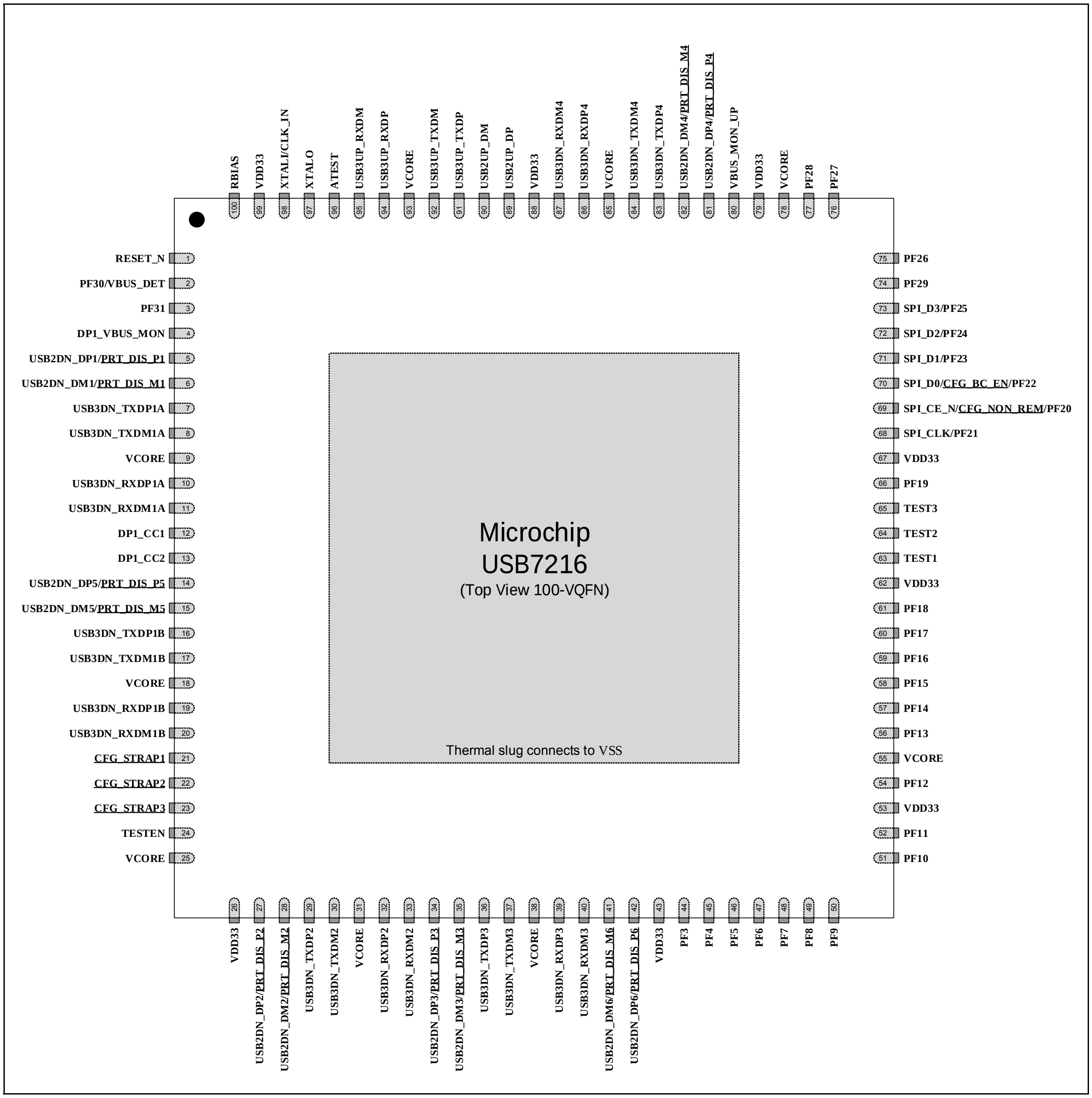
FIGURE 2-1: USB7216 INTERNAL BLOCK DIAGRAM - UPSTREAM TYPE-B APPLICATION



3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

FIGURE 3-1: USB7216 100-VQFN PIN ASSIGNMENTS



Note:	Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

Pin Num	Pin Name	Pin Num	Pin Name
1	RESET_N	51	PF10
2	PF30/VBUS_DET	52	PF11
3	PF31	53	VDD33
4	DP1_VBUS_MON	54	PF12
5	USB2DN_DP1/PRT_DIS_P1	55	VCORE
6	USB2DN_DM1/PRT_DIS_M1	56	PF13
7	USB3DN_TXDP1A	57	PF14
8	USB3DN_TXDM1A	58	PF15
9	VCORE	59	PF16
10	USB3DN_RXDP1A	60	PF17
11	USB3DN_RXDM1A	61	PF18
12	DP1_CC1	62	VDD33
13	DP1_CC2	63	TEST1
14	USB2DN_DP5/PRT_DIS_P5	64	TEST2
15	USB2DN_DM5/PRT_DIS_M5	65	TEST3
16	USB3DN_TXDP1B	66	PF19
17	USB3DN_TXDM1B	67	VDD33
18	VCORE	68	SPI_CLK/PF21
19	USB3DN_RXDP1B	69	SPI_CE_N/CFG_NON_REM/PF20
20	USB3DN_RXDM1B	70	SPI_D0/CFG_BC_EN/PF22
21	CFG_STRAP1	71	SPI_D1/PF23
22	CFG_STRAP2	72	SPI_D2/PF24
23	CFG_STRAP3	73	SPI_D3/PF25
24	TESTEN	74	PF29
25	VCORE	75	PF26
26	VDD33	76	PF27
27	USB2DN_DP2/PRT_DIS_P2	77	PF28
28	USB2DN_DM2/PRT_DIS_M2	78	VCORE
29	USB3DN_TXDP2	79	VDD33
30	USB3DN_TXDM2	80	VBUS_MON_UP
31	VCORE	81	USB2DN_DP4/PRT_DIS_P4
32	USB3DN_RXDP2	82	USB2DN_DM4/PRT_DIS_M4
33	USB3DN_RXDM2	83	USB3DN_TXDP4
34	USB2DN_DP3/PRT_DIS_P3	84	USB3DN_TXDM4
35	USB2DN_DM3/PRT_DIS_M3	85	VCORE
36	USB3DN_TXDP3	86	USB3DN_RXDP4
37	USB3DN_TXDM3	87	USB3DN_RXDM4
38	VCORE	88	VDD33
39	USB3DN_RXDP3	89	USB2UP_DP
40	USB3DN_RXDM3	90	USB2UP_DM
41	USB2DN_DM6/PRT_DIS_M6	91	USB3UP_TXDP
42	USB2DN_DP6/PRT_DIS_P6	92	USB3UP_TXDM
43	VDD33	93	VCORE
44	PF3	94	USB3UP_RXDP
45	PF4	95	USB3UP_RXDM
46	PF5	96	ATEST
47	PF6	97	XTALO
48	PF7	98	XTALI/CLK_IN
49	PF8	99	VDD33
50	PF9	100	RBIAS
Exposed Pad (VSS) must be connected to ground.			

3.2 Pin Descriptions

This section contains descriptions of the various USB7216 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Buffer type definitions are detailed in Section 1.2, Buffer Types.

TABLE 3-1: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 2 Interfaces			
Upstream USB 3.1 Gen 2 TX D+	**USB3UP_TXDP**	I/O-U	Upstream USB 3.1 Gen 2 Transmit Data Plus.
Upstream USB 3.1 Gen 2 TX D-	**USB3UP_TXDM**	I/O-U	Upstream USB 3.1 Gen 2 Transmit Data Minus.
Upstream USB 3.1 Gen 2 RX D+	**USB3UP_RXDP**	I/O-U	Upstream USB 3.1 Gen 2 Receive Data Plus.
Upstream USB 3.1 Gen 2 RX D-	**USB3UP_RXDM**	I/O-U	Upstream USB 3.1 Gen 2 Receive Data Minus.
Downstream Port 1 USB 3.1 Gen 2 TX D+ Orientation A	**USB3DN_TXDP1A**	I/O-U	Downstream USB Type-C® "Orientation A" SuperSpeed+ Transmit Data Plus, port 1.
Downstream Port 1 USB 3.1 Gen 2 TX D- Orientation A	**USB3DN_TXDM1A**	I/O-U	Downstream USB Type-C "Orientation A" SuperSpeed+ Transmit Data Minus, port 1.
Downstream Port 1 USB 3.1 Gen 2 RX D+ Orientation A	**USB3DN_RXDP1A**	I/O-U	Downstream USB Type-C "Orientation A" SuperSpeed+ Receive Data Plus, port 1.
Downstream Port 1 USB 3.1 Gen 2 RX D- Orientation A	**USB3DN_RXDM1A**	I/O-U	Downstream USB Type-C "Orientation A" SuperSpeed+ Receive Data Minus, port 1.
Downstream Port 1 USB 3.1 Gen 2 TX D+ Orientation B	**USB3DN_TXDP1B**	I/O-U	Downstream USB Type-C "Orientation B" SuperSpeed+ Transmit Data Plus, port 1.
Downstream Port 1 USB 3.1 Gen 2 TX D- Orientation B	**USB3DN_TXDM1B**	I/O-U	Downstream USB Type-C "Orientation B" SuperSpeed+ Transmit Data Minus, port 1.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Downstream Port 1 USB 3.1 Gen 2 RX D+ Orientation B	**USB3DN_RXDP1B**	I/O-U	Downstream USB Type-C “Orientation B” SuperSpeed+ Receive Data Plus, port 1.
Downstream Port 1 USB 3.1 Gen 2 RX D- Orientation B	**USB3DN_RXDM1B**	I/O-U	Downstream USB Type-C “Orientation B” SuperSpeed+ Receive Data Minus, port 1.
Downstream Ports 2-4 USB 3.1 Gen 2 TX D+	**USB3DN_TXDP[2:4]**	I/O-U	Downstream SuperSpeed+ Transmit Data Plus, ports 2 through 4.
Downstream Ports 2-4 USB 3.1 Gen 2 TX D-	**USB3DN_TXDM[2:4]**	I/O-U	Downstream SuperSpeed+ Transmit Data Minus, ports 2 through 4.
Downstream Ports 2-4 USB 3.1 Gen 2 RX D+	**USB3DN_RXDP[2:4]**	I/O-U	Downstream SuperSpeed+ Receive Data Plus, ports 2 through 4.
Downstream Ports 2-4 USB 3.1 Gen 2 RX D-	**USB3DN_RXDM[2:4]**	I/O-U	Downstream SuperSpeed+ Receive Data Minus, ports 2 through 4.
USB 2.0 Interfaces			
Upstream USB 2.0 D+	**USB2UP_DP**	I/O-U	Upstream USB 2.0 Data Plus (D+).
Upstream USB 2.0 D-	**USB2UP_DM**	I/O-U	Upstream USB 2.0 Data Minus (D-).
Downstream Ports 1-6 USB 2.0 D+	**USB2DN_DP[1:6]**	I/O-U	Downstream USB 2.0 Ports 1-6 Data Plus (D+).
Downstream Ports 1-6 USB 2.0 D-	**USB2DN_DM[1:6]**	I/O-U	Downstream USB 2.0 Ports 1-6 Data Minus (D-)

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

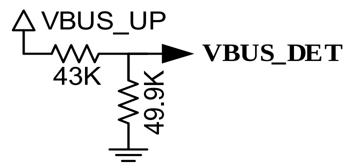
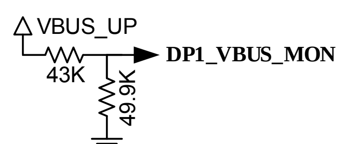
Name	Symbol	Buffer Type	Description
VBUS Detect	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. Externally, VBUS can be as high as 5.25 V, which can be damaging to this pin. The amplitude of VBUS must be reduced by a voltage divider. The recommended voltage divider is shown below.  For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
SPI Interface			
SPI Clock	**SPI_CLK**	I/O-U	SPI clock. If the SPI interface is enabled, this pin must be driven low during reset.
SPI Data 3-0	**SPI_D[3:0]**	I/O-U	SPI Data 3-0. If the SPI interface is enabled, these signals function as Data 3 through 0.
SPI Chip Enable	**SPI_CE_N**	I/O12	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states.
USB Type-C Connector Control			
Downstream Port 1 Type-C Voltage Monitor	**DP1_VBUS_MON**	I/O12	Used to detect Type-C VBUS vSafe5V and vSafe0V states on Port 1. Externally, VBUS can be as high as 5.25 V, which can be damaging to this pin. The amplitude of VBUS must be reduced by a voltage divider. The recommended voltage divider is shown below. 
Downstream Port 1 Type-C CC1	**DP1_CC1**	I/O12	Used for Type-C attach and orientation detection on Port 1. Includes configurable Rp/Ra selection. Connect this pin directly to the CC1 pin of the respective Type-C connector.
Downstream Port 1 Type-C CC2	**DP1_CC2**	I/O12	Used for Type-C attach and orientation detection on Port 1. Includes configurable Rp/Ra selection. Connect this pin directly to the CC2 pin of the respective Type-C connector.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

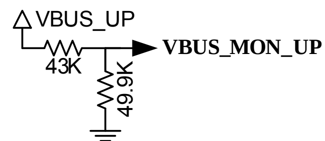
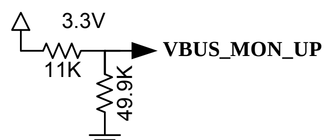
Name	Symbol	Buffer Type	Description
Upstream Type-C Voltage Monitor	**VBUS_MON_UP**	I/O12	Used to detect Type-C VBUS vSafe5V and vSafe0V states on the upstream port. Externally, VBUS can be as high as 5.25 V, which can be damaging to this pin. The amplitude of VBUS must be reduced by a voltage divider. The recommended voltage divider is shown below.  For embedded applications where VBUS_MON_UP will not be connected externally, VBUS_MON_UP must be connected to 2.7V. The recommended voltage divider for using a 3.3V supply is shown below: 
Miscellaneous			
Programmable Function Pins	**PF[31:3]**	I/O12	Programmable function pins.
Test 1	**TEST1**	A	Test 1 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Test 2	**TEST2**	A	Test 2 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Test 3	**TEST3**	A	Test 3 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Reset Input	**RESET_N**	IS	This active low signal is used by the system to reset the device.
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ ±1.0% resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close the device as possible with a dedicated, low impedance connection to the ground plane.
Test	**TESTEN**	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Analog Test	**ATEST**	A	Analog test pin. This signal is used for test purposes and must always be left unconnected.
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input
External 25 MHz Reference Clock Input	**CLK_IN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output
Configuration Straps			
Port 6-1 D+ Disable Configuration Strap	**PRT_DIS_P[6:1]**	I	Port 6-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[6:1]** straps to disable the related port (6-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Port 6-1 D- Disable Configuration Strap	**PRT_DIS_M[6:1]**	I	Port 6-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[6:1]** straps to disable the related port (6-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Non-Removable Ports Configuration Strap. This configuration strap controls the number of reported non-removable ports. See Note 3-1.
Battery Charging Configuration Strap	**CFG_BC_EN**	I/O12	Battery Charging Configuration Strap. This configuration strap controls the number of BC 1.2 enabled downstream ports. See Note 3-1.
Device Mode Configuration Straps 3-1	**CFG_STRAP[3:1]**	I	Device Mode Configuration Straps 3-1. These configuration straps are used to select the device's mode of operation. See Note 3-1.
Power/Ground			
+3.3V I/O Power Supply Input	**VDD33**	P	+3.3 V power and internal regulator input.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Digital Core Power Supply Input	**VCORE**	P	Digital core power supply input.
Ground	**VSS**	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 3-1 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. For additional information, refer to Section 3.3, Configuration Straps and Programmable Functions.

3.3 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following deassertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

> **Note:** The system designer must guarantee that configuration straps meet the timing requirements. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values. Refer to the data sheet.

3.3.1 PORT DISABLE CONFIGURATION (**PRT_DIS_P[6:1]** / **PRT_DIS_M[6:1]**)

The **PRT_DIS_P[6:1]** / **PRT_DIS_M[6:1]** configuration straps are used in conjunction to disable the related port (6-1)

For **PRT_DIS_P*x*** (where *x* is the corresponding port 6-1):

- **0** = Port *x* D+ Enabled
- **1** = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 6-1):

- **0** = Port *x* D- Enabled
- **1** = Port *x* D- Disabled

> **Note:** Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where ***x*** is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.0 port.

3.3.2 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The CFG_NON_REM configuration strap is used to configure the non-removable port settings of the device to one of six settings. These modes are selected by the configuration of an external resistor on the CFG_NON_REM pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-2.

TABLE 3-2: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Ports 1, 2 non-removable
10 kΩ Pull-Up	Ports 1, 2, 3 non-removable
10 Ω Pull-Down	Ports 1, 2, 3, 4 non-removable
10 Ω Pull-Up	Ports 1, 2, 3, 4, 5, 6 non-removable

3.3.3 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The CFG_BC_EN configuration strap is used to configure the battery charging port settings of the device to one of six settings. These modes are selected by the configuration of an external resistor on the CFG_BC_EN pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-3.

TABLE 3-3: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	Battery charging not enable on any port
200 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Port 1
10 kΩ Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2
10 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3
10 Ω Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4
10 Ω Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4, 5, 6

3.3.4 PF[31:3] CONFIGURATION (CFG_STRAP[2:1])

The USB7216 provides 29 programmable function pins (PF[31:3]). These pins can be configured to 2 predefined configuration via the CFG_STRAP[2:1] pins. These configurations are selected via external resistors on the CFG_STRAP[2:1] pins, as detailed in Table 3-4. Resistor values and combinations not detailed in Table 3-4 are reserved and should not be used.

Note: CFG_STRAP3 is not used and must be pulled-down to ground via a 200 kΩ resistor.

TABLE 3-4: CFG_STRAP[2:1] RESISTOR ENCODING

Mode	CFG_STRAP2 Resistor Value	CFG_STRAP1 Resistor Value
Configuration 1	200 kΩ Pull-Down	200 kΩ Pull-Down
Configuration 2	200 kΩ Pull-Down	200 kΩ Pull-Up

A summary of the configuration pin assignments for each of the 2 configurations is provided in Table 3-5. For details on behavior of each programmable function, refer to Table 3-6.

TABLE 3-5: PF[31:3] FUNCTION ASSIGNMENT

Pin	Configuration 1 (SMBus/I^2C)	Configuration 2 (I^2S)
PF3	DP1_VCONN2	DP1_VCONN2
PF4	DP1_VCONN1	DP1_VCONN1
PF5	DP1_DISCHARGE	DP1_DISCHARGE
PF6	GPIO70	GPIO70
PF7	GPIO71	MIC_DET
PF8	GPIO72	GPIO72
PF9	GPIO73	GPIO73
PF10	PRT_CTL2_U3	I2S_SDI
PF11	PRT_CTL3_U3	I2S_MCLK
PF12	PRT_CTL4_U3	PRT_CTL4_U3
PF13	PRT_CTL4	PRT_CTL4
PF14	PRT_CTL3	PRT_CTL3
PF15	PRT_CTL2	PRT_CTL2
PF16	PRT_CTL5	PRT_CTL5
PF17	PRT_CTL1	PRT_CTL1
PF18	ALERT0	ALERT0
PF19	-	I2S_SDO
PF20	SPI_CE_N	SPI_CE_N
PF21	SPI_CLK	SPI_CLK
PF22	SPI_D0	SPI_D0
PF23	SPI_D1	SPI_D1
PF24	SPI_D2	SPI_D2
PF25	SPI_D3	SPI_D3
PF26	SLV_I2C_CLK	I2S_SCK
PF27	SLV_I2C_DATA	PRT_CTL6
PF28	PRT_CTL6	I2S_LRCK
PF29	GPIO93	GPIO93
PF30	MSTR_I2C_CLK	MSTR_I2C_CLK
PF31	MSTR_I2C_DATA	MSTR_I2C_DATA

Note: The default **PF*x*** pin functions can be overridden with additional configuration by modification of the pin mux registers. These changes can be made during the SMBus configuration stage, by programming to OTP memory, or during runtime (after hub has attached and enumerated) by register writes via the SMBus slave interface or USB commands to the internal Hub Feature Controller Device.

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS

Function	Buffer Type	Description
Master SMBus/I²C Interface		
MSTR_I2C_CLK	I/O12	Bridging Master SMBus/I^2C controller clock (SMBus/I^2C controller 1)
MSTR_I2C_DATA	I/O12	Bridging Master SMBus/I^2C controller data (SMBus/I^2C controller 1)
Slave SMBus/I²C Interface		
SLV_I2C_CLK	I/O12	Slave SMBus/I^2C controller clock (SMBus/I^2C controller 2)
SLV_I2C_DATA	I/O12	Slave SMBus/I^2C controller data (SMBus/I^2C controller 2)
SPI Interface		
SPI_CLK	I/O-U	SPI clock. If the SPI interface is enabled, this pin must be driven low during reset.
SPI_D[3:0]	I/O-U	SPI Data 3-0. If the SPI interface is enabled, these signals function as Data 3 through 0.
SPI_CE_N	I/O12	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states.
I²S Interface		
I2S_SDI	I	I^2S Serial Data In
I2S_SDO	O12	I^2S Serial Data Out
I2S_SCK	O12	I^2S Continuous Serial Clock
I2S_LRCK	O12	I^2S Word Select / Left-Right Clock
I2S_MCLK	O12	I^2S Master Clock
MIC_DET	I	I^2S Microphone Plug Detect 0 = No microphone plugged into the audio jack 1 = Microphone plugged into the audio jack
Miscellaneous		
ALERT0	I	Alert 0 Interrupt input for connection to the local companion (UPD360/UPD350) power delivery controller’s IRQ# signal.
DP1_VCONN1	I/O12	Port 1 VCONN1 enable
DP1_VCONN2	I/O12	Port 1 VCONN2 enable
DP1_DISCHARGE	I/O12	Port 1 DISCHARGE enable

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
PRT_CTL6	I/O12 (PU)	Port 6 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 6. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This signal controls both the USB 2.0 and USB 3.1 portions of the port.
PRT_CTL5	I/O12 (PU)	Port 5 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This signal controls both the USB 2.0 and USB 3.1 portions of the port.
PRT_CTL4	I/O12 (PU)	Port 4 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL3	I/O12 (PU)	Port 3 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
PRT_CTL2	I/O12 (PU)	Port 2 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL1	I/O12 (PU)	Port 1 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This signal controls both the USB 2.0 and USB 3.1 portions of the port.
PRT_CTL4_U3	O12	Port 4 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 4 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
PRT_CTL3_U3	O12	Port 3 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 3 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
PRT_CTL2_U3	O12	Port 2 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 3 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
GPIO*x*	I/O12	General Purpose Input/Output (*x* = 70-73, 93)

3.4 Physical and Logical Port Mapping

The USB72xx family of devices are based upon a common architecture, but all have different modifications and/or pin bond outs to achieve the various device configurations. The base chip is composed of a total of 6 USB3 PHYs and 7 USB2 PHYs. These PHYs are physically arranged on the chip in a certain way, which is referred to as the PHYSICAL port mapping.

The actual port numbering is remapped by default in different ways on each device in the family. This changes the way that the ports are numbered from the USB host's perspective. This is referred to as LOGICAL mapping.

The various configuration options available for these devices may, at times, be with respect to PHYSICAL mapping or LOGICAL mapping. Each individual configuration option which has a PHYSICAL or LOGICAL dependency is declared as such within the register description.

The PHYSICAL vs. LOGICAL mapping is described for all port related pins in Table 3-7. A system design in schematics and layout is generally performed using the pinout in Section 3.1, Pin Assignments, which is assigned by the default LOGICAL mapping. Hence, it may be necessary to cross reference the PHYSICAL vs. LOGICAL look up tables when determining the hub configuration.

Note:	The MPLAB Connect tool makes configuration simple; the settings can be selected by the user with respect to the LOGICAL port numbering. The tool handles the necessary linking to the PHYSICAL port settings. Refer to the data sheet for additional information.

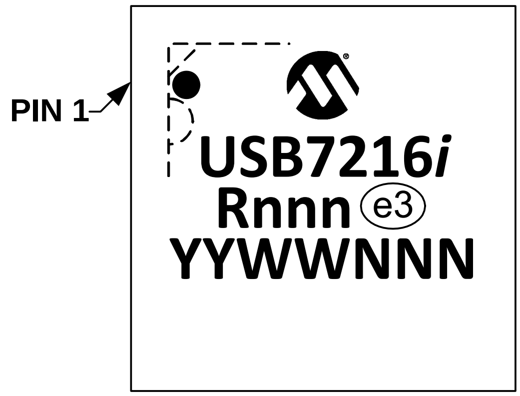
TABLE 3-7: USB7216 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
5	USB2DN_DP1		X							X					
6	USB2DN_DM1		X							X					
7	USB3DN_TXDP1A		X							X					
8	USB3DN_TXDM1A		X							X					
10	USB3DN_RXDP1A		X							X					
11	USB3DN_RXDM1A		X							X					
14	USB2DN_DP5						X				X				
15	USB2DN_DM5						X				X				
16	USB3DN_TXDP1B		X								X				
17	USB3DN_TXDM1B		X								X				
19	USB3DN_RXDP1B		X								X				
20	USB3DN_RXDM1B		X								X				
27	USB2DN_DP2			X								X			
28	USB2DN_DM2			X								X			
29	USB3DN_TXDP2			X								X			
30	USB3DN_TXDM2			X								X			
32	USB3DN_RXDP2			X								X			
33	USB3DN_RXDM2			X								X			
34	USB2DN_DP3				X								X		
35	USB2DN_DM3				X								X		
36	USB3DN_TXDP3				X								X		
37	USB3DN_TXDM3				X								X		
39	USB3DN_RXDP3				X								X		
40	USB3DN_RXDM3				X								X		
41	USB2DN_DM6							X							X
42	USB2DN_DP6							X							X
81	USB2DN_DP4					X								X	
82	USB2DN_DM4					X								X	
83	USB3DN_TXDP4					X								X	
84	USB3DN_TXDM4					X								X	
86	USB3DN_RXDP4					X								X	
87	USB3DN_RXDM4					X								X	
89	USB2UP_DP	X							X						
90	USB2UP_DM	X							X						
91	USB3UP_TXDP	X							X						
92	USB3UP_TXDM	X							X						
94	USB3UP_RXDP	X							X						
95	USB3UP_RXDM	X							X						

4.0 PACKAGE OUTLINE

4.1 Package Marking Information

100-VQFN (12x12 mm)



Legend:	*i*	Temperature range designator (Blank = commercial, *i* = industrial)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

4.2 Package Drawings

Note:	For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 4-1: 100-VQFN PACKAGE (DRAWING)

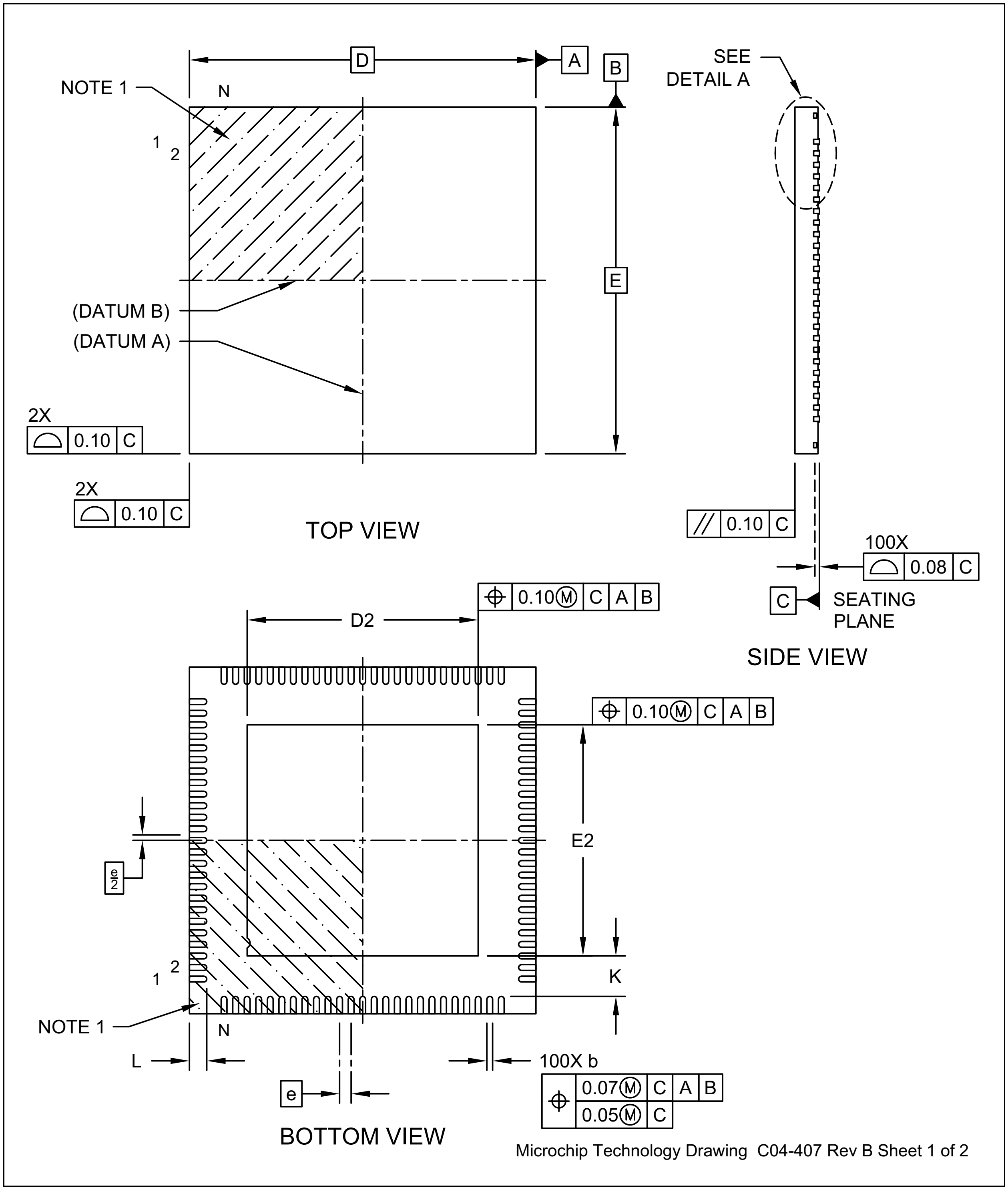
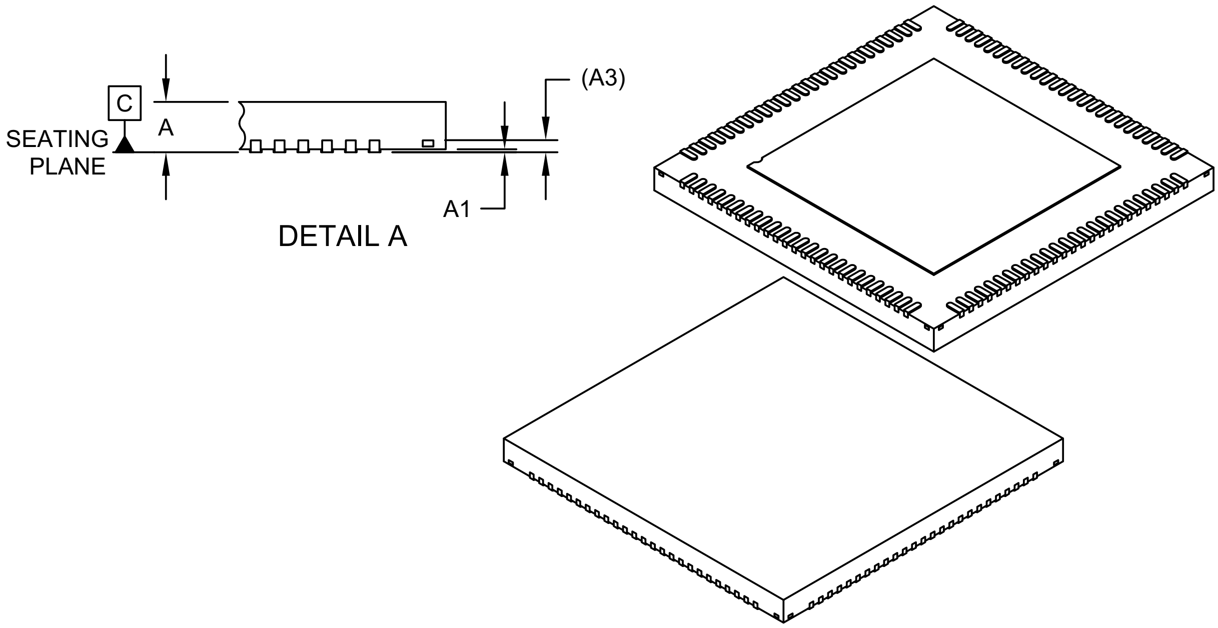


FIGURE 4-2: 100-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		12.00 BSC	
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E		12.00 BSC	
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	1.30	-	-

Notes:

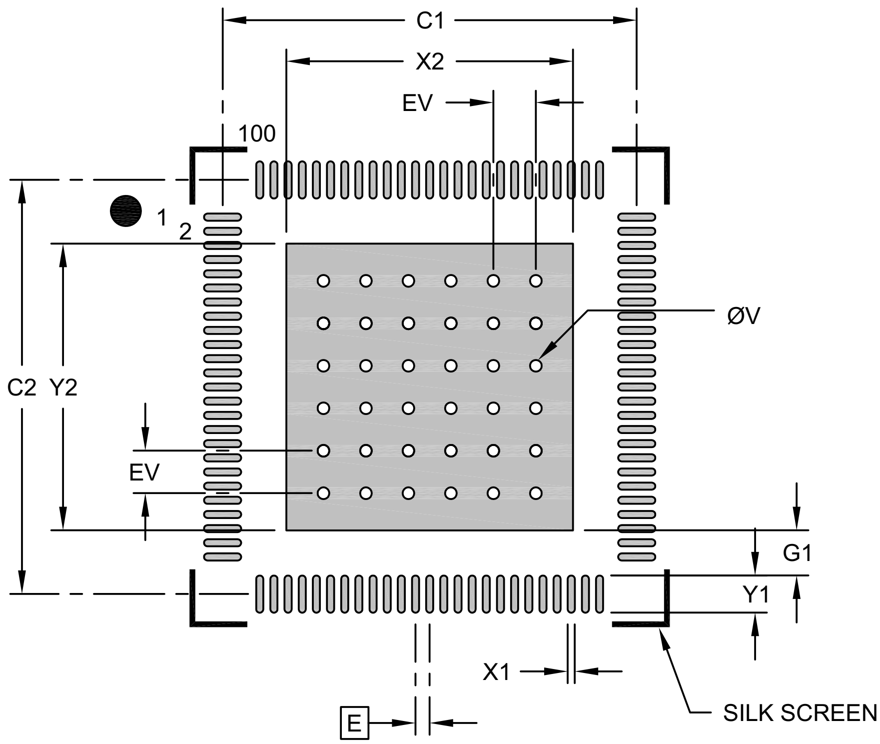
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-407 Rev B Sheet 2 of 2

FIGURE 4-3: 100-VQFN PACKAGE (LAND-PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	X2			8.10
Optional Center Pad Length	Y2			8.10
Contact Pad Spacing	C1		11.70	
Contact Pad Spacing	C2		11.70	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.05
Contact Pad to Center Pad (X100)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2407A

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

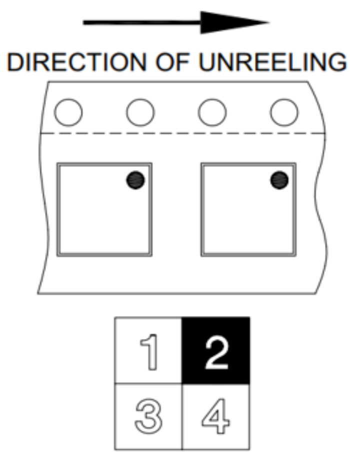
Revision Level & Date	Section/Figure/Entry	Correction
DS00003140A (10-09-19)	All	Initial Release

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	-	[X]	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	USB7216
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel (Note 1)
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)
Package:	KDX = 100-pin VQFN



Examples:

a) USB7216/KDX
Tray, 0°C to +70°C, 100-pin VQFN

b) USB7216T/KDX
Tape & reel, 0°C to +70°C, 100-pin VQFN

c) USB7216-I/KDX
Tray, -40°C to +85°C, 100-pin VQFN

d) USB7216T-I/KDX
Tape & reel, -40°C to +85°C, 100-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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China - Suzhou
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Tel: 86-27-5980-5300

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Tel: 86-29-8833-7252

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