HV582

96-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- 96 High-Voltage Channels
  - Up to 80V Operating Output Voltage
  - 75 mA Peak Output Sink/Source Current
- Six Parallel 16-bit Shift Registers
  - Clockwise and Counter-Clockwise Data Shifting via DIR Pin
- 30 MHz Data Rate

Applications

- Inkjet Printer Driver
- AC Plasma Data Driver
- 3D Printer Driver

Related Devices

- **HV583**: 128-Channel Serial to Parallel Converter with Push-Pull Outputs

Description

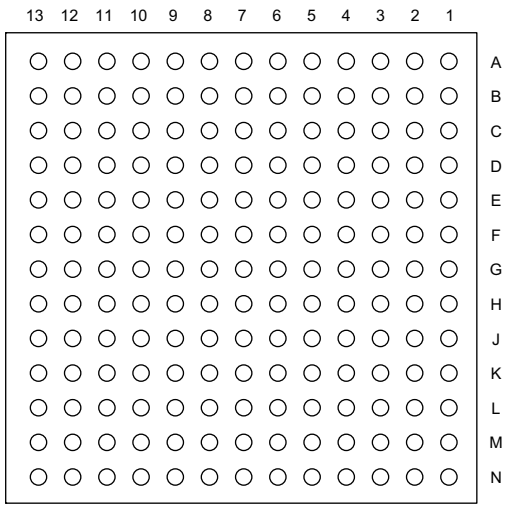
HV582 is a unipolar, 96-channel low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for applications requiring multiple high-voltage outputs with current sinking and sourcing capabilities, such as plasma displays and Inkjet printers.

The device consists of six parallel 16-bit shift registers, a 96-bit latch and 96 high-voltage outputs. The shift registers operate at 30 MHz, allowing 180 MHz data rates due to the parallel arrangement.

HV582 is offered in a 169-ball 10 x 10 x 1.1 mm TFBGA package.

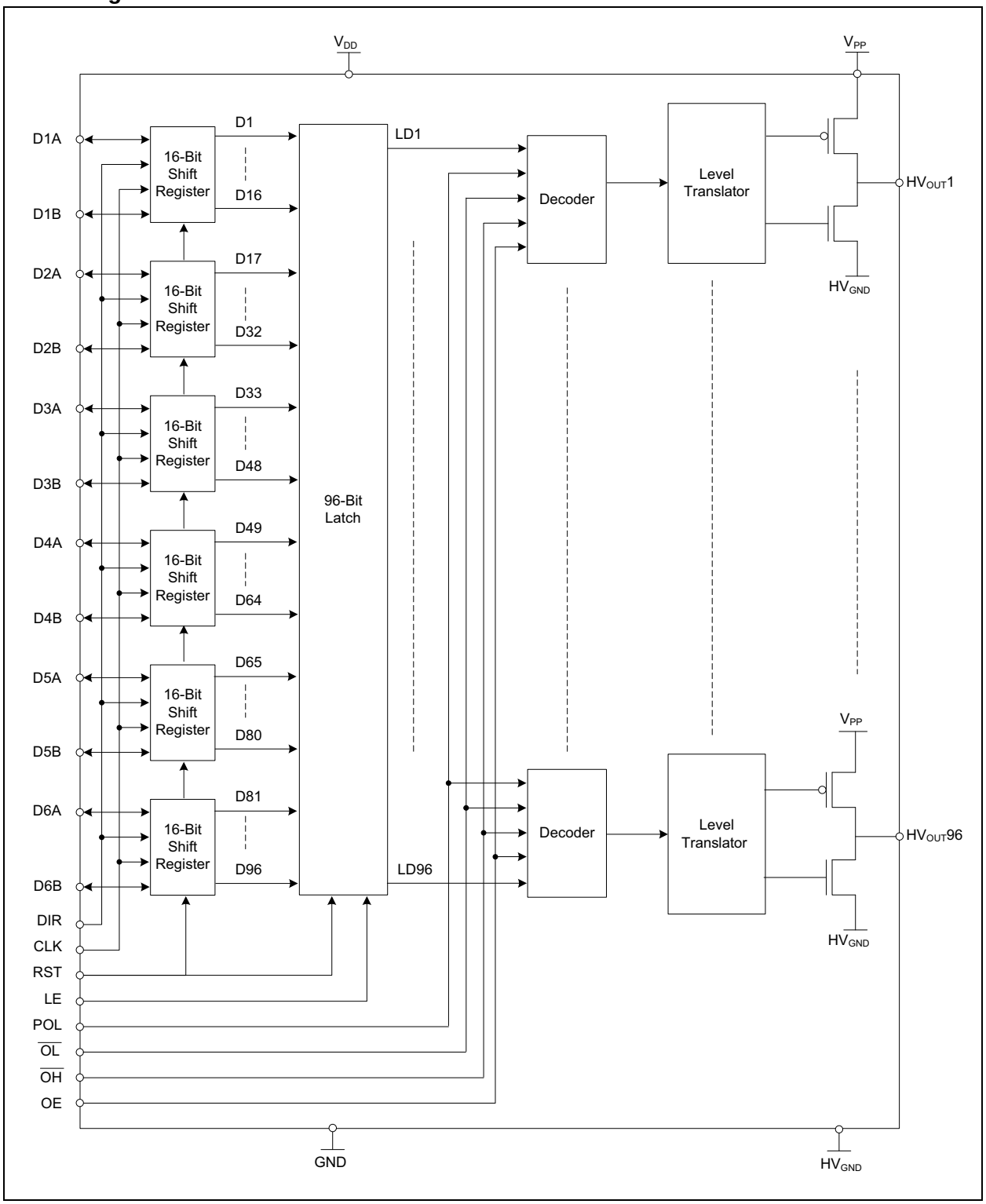
Package Type

HV582
10x10x1.1 mm TFBGA*
Bottom View



* See **Section 2.0, Package Pin Configuration and Function Description**.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating†

Supply Voltage V_{DD} ..... -0.5V to +6.0V

High-Voltage Supply V_{PP} ..... V_{DD} to +85V

Logic Input Voltages ..... -0.5V to V_{DD} + 0.5V

Operating Junction Temperature ..... -40°C to +125°C

Storage Temperature ..... -65°C to +150°C

†Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device is ESD sensitive. Use appropriate ESD precaution.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High-Voltage Supply	V_{PP}	10	—	80	V	
High-Level Input Voltage	V_{IH}	V_{DD} – 0.9	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.9	V	

TABLE 1-1: POWER SEQUENCES

Sequence Type	Steps
Power-Up Sequence	1. Connect Ground. 2. Apply V_{DD}. 3. Set All Inputs (Data, CLK, etc.) to a known state. 4. Apply V_{PP}.
Power-Down Sequence	Repeat the Power-Up sequence in reverse order.

DC ELECTRICAL CHARACTERISTICS

Electrical Specification: Unless otherwise specified, $T_A = T_J$ = +25°C, V_{DD} = 5.0V and V_{PP} = 80V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{PP} Quiescent Supply Current	I_{PPQ}	–	–	100	µA	
V_{DD} Quiescent Supply Current	I_{DDQ}	–	–	100	µA	
V_{DD} Supply Current	I_{DD}	–	–	25	mA	f_{CLK}= 30 MHz, LE = low
High-Level Output Voltage	HV_{OH}	70	75	–	V	I_{OUT} = 75 mA, V_{PP} = 80V
Output P-Channel Body Diode	HV_{OHD}	–	–	83	V	I_{OUT} = -75 mA, V_{PP} = 80V (Note 1)
Low-Level Output Voltage	HV_{OL}	–	5.0	10	V	I_{OUT} = -75 mA
Output N-Channel Body Diode	HV_{OLD}	-3.0	–	–	V	I_{OUT} = 75 mA (Note 1)
Logic Input High Current	I_{IH}	–	–	1.0	µA	$V_{IH} = V_{DD}$
		10	30	50		$V_{IH} = V_{DD}$, RST and POL only

Note 1: Specification is for design guidance only.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specification: Unless otherwise specified, $T_A = T_J = +25°C$, $V_{DD} = 5.0V$ and $V_{PP} = 80V$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Logic Input Low Current	I_{IL}	-1.0	–	–	µA	V_{IL} = -0.3V
Logic Output High	V_{OH}	3.5	–	–	V	I_{OUT} = 4 mA
Logic Output Low	V_{OL}	–	–	1.0		I_{OUT} = -4 mA

Note 1: Specification is for design guidance only.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified $T_A = T_J = +25°C$, $V_{DD} = 5.0V$ and $V_{PP} = 80V$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Data Clock Frequency	f_{CLK}	—	—	30	MHz	
Clock Pulse Width, High and Low	t_{wCLK}	16.6	—	—	ns	Note 1
LE Pulse Width, High and Low	t_{wLE}	16.6	—	—		Note 2
Setup Time, DnA/B to CLK	t_{su1}	5	—	—		Note 1
Setup Time, CLK to LE	t_{su2}	15	—	—		Note 1
Setup Time, LE to $\overline{OL}$,$\overline{OH}$	t_{su3}	25	—	—		Note 1
Hold Time, CLK to DnA/B	t_{h1}	15	—	—		Note 1
Hold Time, LE to CLK	t_{h2}	15	—	—		Note 1
CLK to DnA/B (High-to-Low)	t_{pdHL}	—	—	25		C_L = 170 pF
CLK to DnA/B (Low-to-High)	t_{pdLH}	—	—	25		C_L = 170 pF
LE,$\overline{OL}$,$\overline{OH}$ to $HV_{OUT}n$ (High-to-Low)	t_{pHL}	—	—	300		C_L = 170 pF
LE,$\overline{OL}$,$\overline{OH}$ to $HV_{OUT}n$ (Low-to-High)	t_{pLH}	—	—	300		C_L = 170 pF
OE to $HV_{OUT}n$ (High-to-Low)	t_{pHZL}	—	—	150		C_L = 170 pF
OE to $HV_{OUT}n$ (Low-to-High)	t_{pLZH}	—	—	150		C_L = 170 pF
OE to $HV_{OUT}n$ (High-to-Low)	t_{pHZ}	—	—	300		
OE to $HV_{OUT}n$ (Low-to-High)	t_{pLZ}	—	—	300		
Rise Time $HV_{OUT}n$	t_r	—	—	200		C_L = 170 pF
Fall Time $HV_{OUT}n$	t_f	—	—	200		C_L = 170 pF

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Specification is for design guidance only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature	T_J	-40	—	+125	°C	
Storage Temperature	T_A	-65	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, 169-Ball TFBGA	θ_{JA}	—	27	—	°C/W	

1.1 Logic Characteristics

TABLE 1-2: LOGIC FUNCTION TRUTH TABLE

Function	Inputs								Outputs		
	RST	Data	CLK	LE	OE	POL	$\overline{OL}$	$\overline{OH}$	Shift Reg. 1 2...96	HV Outputs 1 2...96	Data Out
All Low	L	X	X	X	H	X	L	X	* *...*	L L...L	*
All High	L	X	X	X	H	X	H	L	* *...*	H H...H	*
Output High Z	L	X	X	X	L	X	X	X	* *...*	Z Z...Z	*
Invert Mode	L	X	X	L	H	H	H	H	* *...*	* *...*(b)	*
Load S/R	L	H or L	↑	L	H	L	H	H	H or L *...*	* *...*	*
Store Data in Latches	L	X	X	L	H	L	H	H	* *...*	* *...*	*
	L	X	X	L	H	H	H	H	* *...*	* *...* (b)	*
Transparent Mode	L	L	↑	H	H	L	H	H	L * *...*	L * *...*	*
	L	H	↑	H	H	L	H	H	H * *...*	H * *...*	*
Reset	H	X	X	X	H	L	H	H	L * *...*	L * *...*	L

Legend:

D = Data

H = Level High

L = Level Low

X = Don't Care

Z = High Impedance

b = Inversion

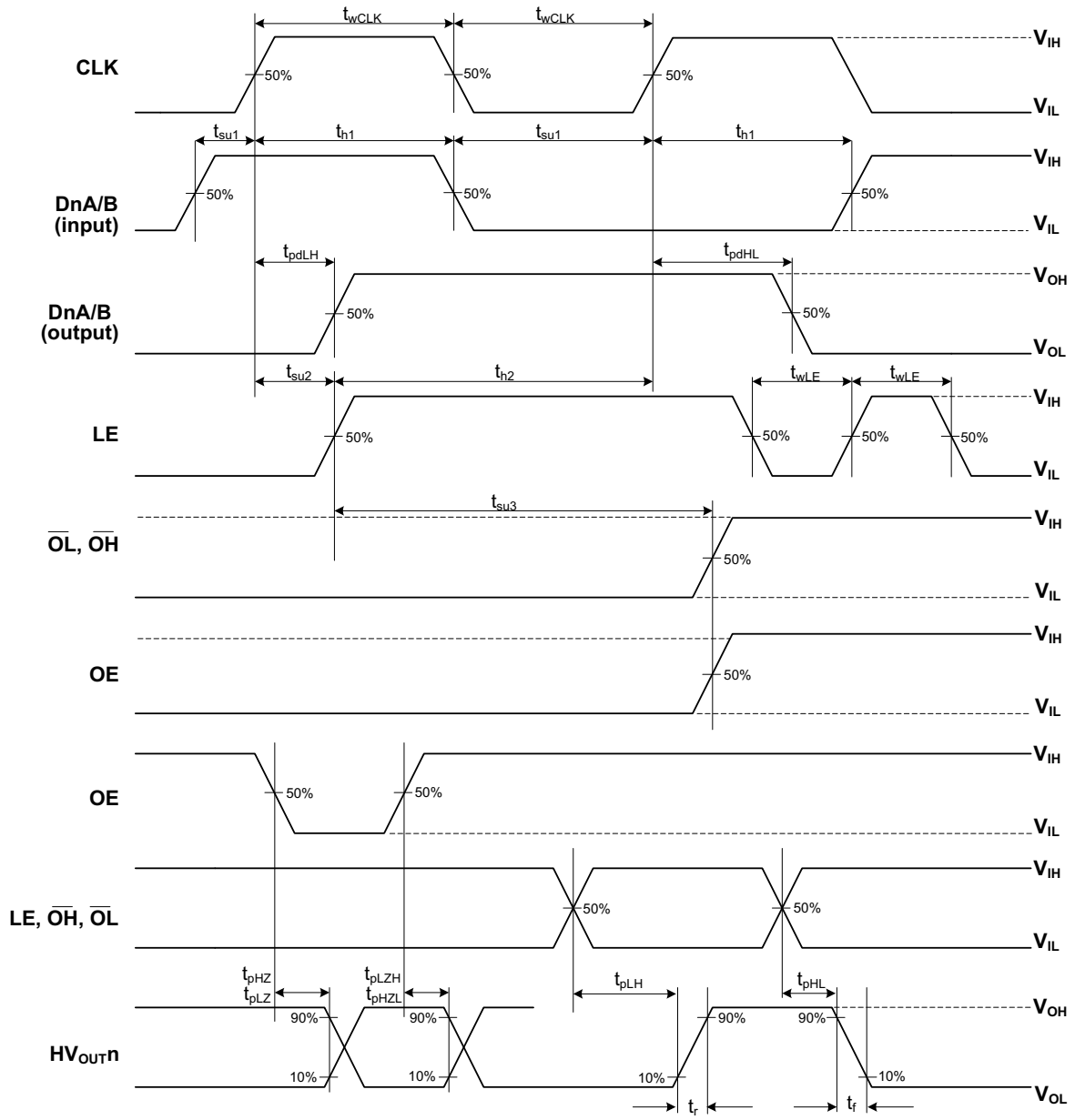
* = Dependent of previous stage's state before the last CLK or last LE high

↑ = Low-to-High Transition

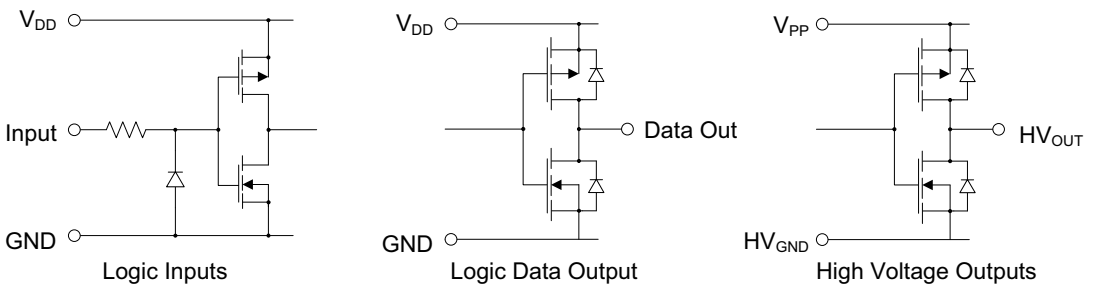
TABLE 1-3: OUTPUT SHIFT OPERATION

Input	Output	DIR	Shift Operation
D1A	D1B	L	D1 to D16
D2A	D2B	L	D17 to D32
D3A	D3B	L	D33 to D48
D4A	D4B	L	D49 to D64
D5A	D5B	L	D65 to D80
D6A	D6B	L	D81 to D96
D1B	D1A	H	D16 to D1
D2B	D2A	H	D32 to D17
D3B	D3A	H	D48 to D33
D4B	D4A	H	D64 to D49
D5B	D5A	H	D80 to D65
D6B	D6A	H	D96 to D81

1.2 Timing Diagram



1.3 Input and Output Equivalent Circuits



2.0 PACKAGE PIN CONFIGURATION AND FUNCTION DESCRIPTION

This section details the pin designation for the 169-Ball TFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	$HV_{OUT}66$	$HV_{OUT}65$	$HV_{OUT}63$	$HV_{OUT}60$	$HV_{OUT}57$	$HV_{OUT}54$	$HV_{OUT}51$	$HV_{OUT}48$	$HV_{OUT}45$	$HV_{OUT}42$	$HV_{OUT}39$	$HV_{OUT}36$	$HV_{OUT}34$
B	$HV_{OUT}67$	$HV_{OUT}64$	$HV_{OUT}62$	$HV_{OUT}59$	$HV_{OUT}56$	$HV_{OUT}53$	$HV_{OUT}50$	$HV_{OUT}47$	$HV_{OUT}44$	$HV_{OUT}41$	$HV_{OUT}38$	$HV_{OUT}35$	$HV_{OUT}33$
C	$HV_{OUT}69$	$HV_{OUT}68$	$HV_{OUT}61$	$HV_{OUT}58$	$HV_{OUT}55$	$HV_{OUT}52$	$HV_{OUT}49$	$HV_{OUT}46$	$HV_{OUT}43$	$HV_{OUT}40$	$HV_{OUT}37$	$HV_{OUT}31$	$HV_{OUT}32$
D	$HV_{OUT}72$	$HV_{OUT}71$	$HV_{OUT}70$	NC	NC	NC	NC	NC	NC	NC	$HV_{OUT}28$	$HV_{OUT}29$	$HV_{OUT}30$
E	$HV_{OUT}75$	$HV_{OUT}74$	$HV_{OUT}73$	NC	V_{PP}	V_{PP}	NC	V_{PP}	V_{PP}	NC	$HV_{OUT}25$	$HV_{OUT}26$	$HV_{OUT}27$
F	$HV_{OUT}78$	$HV_{OUT}77$	$HV_{OUT}76$	NC	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	NC	$HV_{OUT}22$	$HV_{OUT}23$	$HV_{OUT}24$
G	$HV_{OUT}81$	$HV_{OUT}80$	$HV_{OUT}79$	NC	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	NC	$HV_{OUT}19$	$HV_{OUT}20$	$HV_{OUT}21$
H	$HV_{OUT}84$	$HV_{OUT}83$	$HV_{OUT}82$	NC	HV_{GND}	HV_{GND}	HV_{GND}	HV_{GND}	HV_{GND}	NC	$HV_{OUT}16$	$HV_{OUT}17$	$HV_{OUT}18$
J	$HV_{OUT}87$	$HV_{OUT}86$	$HV_{OUT}85$	NC	HV_{GND}	HV_{GND}	HV_{GND}	HV_{GND}	HV_{GND}	NC	$HV_{OUT}13$	$HV_{OUT}14$	$HV_{OUT}15$
K	$HV_{OUT}90$	$HV_{OUT}89$	$HV_{OUT}88$	NC	V_{DD}	GND	V_{DD}	GND	NC	NC	$HV_{OUT}10$	$HV_{OUT}11$	$HV_{OUT}12$
L	$HV_{OUT}92$	$HV_{OUT}91$	NC	D4B	D1B	$\overline{OL}$	RST	D6A	D3A	NC	$HV_{OUT}1$	$HV_{OUT}8$	$HV_{OUT}9$
M	$HV_{OUT}93$	$HV_{OUT}95$	NC	D5B	D2B	OE	DIR	CLK	D4A	D1A	$HV_{OUT}2$	$HV_{OUT}4$	$HV_{OUT}7$
N	$HV_{OUT}94$	$HV_{OUT}96$	NC	D6B	D3B	POL	$\overline{OH}$	LE	D5A	D2A	$HV_{OUT}3$	$HV_{OUT}5$	$HV_{OUT}6$

FIGURE 2-1: *169-Ball TFBGA Package*

TABLE 2-1: PIN ASSIGNMENT

Pin #	Symbol	Pin #	Symbol	Pin #	Symbol
A1	$HV_{OUT}66$	D3	$HV_{OUT}70$	K6, K8	GND
A2	$HV_{OUT}65$	D4, D5, D6, D7, D8, D9, D10, E4, E7, E10, F4, F10, G4, G10, H4, H10, J4, J10, K4, K9, K10, L3, L10, M3, N3	NC	K11	$HV_{OUT}10$
A3	$HV_{OUT}63$	D11	$HV_{OUT}28$	K12	$HV_{OUT}11$
A4	$HV_{OUT}60$	D12	$HV_{OUT}29$	K13	$HV_{OUT}12$
A5	$HV_{OUT}57$	D13	$HV_{OUT}30$	L1	$HV_{OUT}92$
A6	$HV_{OUT}54$	E1	$HV_{OUT}75$	L2	$HV_{OUT}91$
A7	$HV_{OUT}51$	E2	$HV_{OUT}74$	L4	DB4
A8	$HV_{OUT}48$	E3	$HV_{OUT}73$	L5	DB1
A9	$HV_{OUT}45$	E5, E6, E8, E9, F5, F6, F7, F8, F9, G5, G6, G7, G8, G9	V_{PP}	L6	$\overline{OL}$
A10	$HV_{OUT}42$	E11	$HV_{OUT}25$	L7	RST
A11	$HV_{OUT}39$	E12	$HV_{OUT}26$	L8	D6A
A12	$HV_{OUT}36$	E13	$HV_{OUT}27$	L9	D3A
A13	$HV_{OUT}34$	F1	$HV_{OUT}78$	L11	$HV_{OUT}1$
B1	$HV_{OUT}67$	F2	$HV_{OUT}77$	L12	$HV_{OUT}8$
B2	$HV_{OUT}64$	F3	$HV_{OUT}76$	L13	$HV_{OUT}9$
B3	$HV_{OUT}62$	F11	$HV_{OUT}22$	M1	$HV_{OUT}93$
B4	$HV_{OUT}59$	F12	$HV_{OUT}23$	M2	$HV_{OUT}95$
B5	$HV_{OUT}56$	F13	$HV_{OUT}24$	M4	DB5
B6	$HV_{OUT}53$	G1	$HV_{OUT}81$	M5	DB2
B7	$HV_{OUT}50$	G2	$HV_{OUT}80$	M6	OE
B8	$HV_{OUT}47$	G3	$HV_{OUT}79$	M7	DIR
B9	$HV_{OUT}44$	G11	$HV_{OUT}19$	M8	CLK
B10	$HV_{OUT}41$	G12	$HV_{OUT}20$	M9	D4A
B11	$HV_{OUT}38$	G13	$HV_{OUT}21$	M10	D1A
B12	$HV_{OUT}35$	H1	$HV_{OUT}84$	M11	$HV_{OUT}2$
B13	$HV_{OUT}33$	H2	$HV_{OUT}83$	M12	$HV_{OUT}4$
C1	$HV_{OUT}69$	H3	$HV_{OUT}82$	M13	$HV_{OUT}7$
C2	$HV_{OUT}68$	H5, H6, H7, H8, H9, J5, J6, J7, J8, J9	HVGND	N1	$HV_{OUT}94$
C3	$HV_{OUT}61$	H11	$HV_{OUT}16$	N2	$HV_{OUT}96$
C4	$HV_{OUT}58$	H12	$HV_{OUT}17$	N4	DB6
C5	$HV_{OUT}55$	H13	$HV_{OUT}18$	N5	D3B
C6	$HV_{OUT}52$	J1	$HV_{OUT}87$	N6	POL
C7	$HV_{OUT}49$	J2	$HV_{OUT}86$	N7	$\overline{OH}$
C8	$HV_{OUT}46$	J3	$HV_{OUT}85$	N8	LE
C9	$HV_{OUT}43$	J11	$HV_{OUT}13$	N9	D5A
C10	$HV_{OUT}40$	J12	$HV_{OUT}14$	N10	D2A
C11	$HV_{OUT}37$	J13	$HV_{OUT}15$	N11	$HV_{OUT}3$
C12	$HV_{OUT}31$	K1	$HV_{OUT}90$	N12	$HV_{OUT}5$
C13	$HV_{OUT}32$	K2	$HV_{OUT}89$	N13	$HV_{OUT}6$
D1	$HV_{OUT}72$	K3	$HV_{OUT}88$		
D2	$HV_{OUT}71$	K5, K7	V_{DD}		

2.1 High-Voltage Output Pins ($HV_{OUT}1$ to $HV_{OUT}96$)

These are the high-voltage output channels (Push-Pull).

2.2 High-Voltage Power Supply Pins (V_{PP})

High-voltage power supply pins for the output channels ($HV_{OUT}n$).

2.3 High-Voltage Ground Pins (HV_{GND})

High-voltage ground pins provide the reference ground level for the high-voltage output channels.

2.4 Logic Power Supply Pins (V_{DD})

Logic power supply pins for the 16-bit shift registers, 96-bit latch and decoders.

2.5 Data Input/Output Pins (D1B, D2B, D3B, D4B, D5B, D6B)

Data Input/Output pins are configurable as inputs or outputs for the shift registers depending on the state of the Direction pin (DIR).

When DIR is High, pins D1B to D6B are configured as inputs to the data shift registers. When DIR is Low, these pins are configured as outputs of the data shift registers.

2.6 Polarity Pin (POL)

The Polarity pin inverts the current state for all the $HV_{OUT}n$ channels (from High to Low or Low to High) when set High.

2.7 Output Enable Pin (OE)

The Output Enable pin controls the functionality of the high-voltage output channels.

When OE is High, all $HV_{OUT}n$ channels are enabled and form a push-pull configuration to operate according to input data or $\overline{OL}$, $\overline{OH}$ or POL configuration states. When OE is Low, all $HV_{OUT}n$ channels are forced to a high-impedance state, regardless of the data stored in the 96-bit latch or the states of the $\overline{OL}$, $\overline{OH}$ and POL pins.

2.8 Output Low Pin ($\overline{OL}$)

The Output Low pin sets all high-voltage output channels ($HV_{OUT}1$ to $HV_{OUT}96$) to a Low level state (HV_{GND}).

When $\overline{OL}$ is set Low and OE is High, all the $HV_{OUT}n$ channels are forced to a Low-level state (HV_{GND}), regardless of the data stored in the 96-bit latch. See Table 1-2 for more information.

2.9 Output High Pin ($\overline{OH}$)

The Output High pin sets all high-voltage output channels ($HV_{OUT}1$ to $HV_{OUT}96$) to a High-level state (V_{PP}).

When $\overline{OH}$ is Low while OE and $\overline{OL}$ are High, all the $HV_{OUT}n$ channels are forced to a High-level state (V_{PP}), regardless of the data stored in the 96-bit latch. See Table 1-2 for more information.

2.10 Direction Pin (DIR)

The DIR pin controls the direction of the input data flow for the input registers, whether it is clockwise (DnA to DnB) or counter-clockwise (DnB to DnA).

When DIR is set High, data flows from DnB to DnA. When DIR is set Low, data flows from DnA to DnB. See Table 1-3 for more information.

2.11 Logic Ground Pins (GND)

Logic ground pins provide a reference ground level for the low-voltage section of the IC, shift registers, latches and decoders.

2.12 Reset Pin (RST)

The RST pin clears shift registers and the 96-bit latch data content when it is set High. See Table 1-2 for more information.

2.13 Latch Enable Pin (LE)

The Latch Enable pin controls the data transfer from the input shift registers to the 96-bit latch and the $HV_{OUT}n$ channels. See Table 1-2 for more information.

2.14 Clock Input Pin (CLK)

This is the clock input pin for the 16-bit input shift registers.

2.15 Data Input/Output Pins (D1A, D2A, D3A, D4A, D5A, D6A)

The Data Input/Output pins are configurable as inputs or outputs for the shift registers depending on the state of the Direction pin (DIR).

When DIR is Low, pins D1A to D6A are configured as inputs to the data shift registers. When DIR is High, pins D1A to D6A are configured as outputs of the data shift registers.

2.16 No Connection Pins (NC)

NC pins do not have any functionality on the IC. These pins should not be connected.

3.0 FUNCTIONAL DESCRIPTION

The HV582 is a unipolar, 96-channel low-voltage serial to high-voltage parallel converter. The device consists of six parallel 16-bit shift registers, a 96-bit latch and 96 high-voltage outputs.

The six independent shift registers allow data to be updated into the 96-bit latch at six times the speed of a single register (30 MHz), providing a fast update rate for the 96 output channels. The 96-bit latch holds the data for the high-voltage output channels; whether it is a High-level or Low-level state. The flow of the input data can switch direction from clockwise (D1-6A to D1-6B) to counter-clockwise (D1-6B to D1-6A) by controlling the DIR pin. A reset pin (RST) is provided to clear the contents of the latches. All channels can be set at the same time to a high-impedance state (High Z), Low-level state, High-level state, or to alter their polarity through the OE, $\overline{OL}$, $\overline{OH}$ and POL pins, respectively.

The high-output voltages ($HV_{OUT}n$) can operate from 10V to 80V with a maximum current source and sink capability of 75 mA.

3.1 Application Information

HV582 is designed for applications requiring multiple high-voltage outputs with current sinking and sourcing capabilities in the range of ±75 mA. Typical applications where the HV582 is utilized are in plasma displays, Inkjet printer drivers and 3D printer drivers.

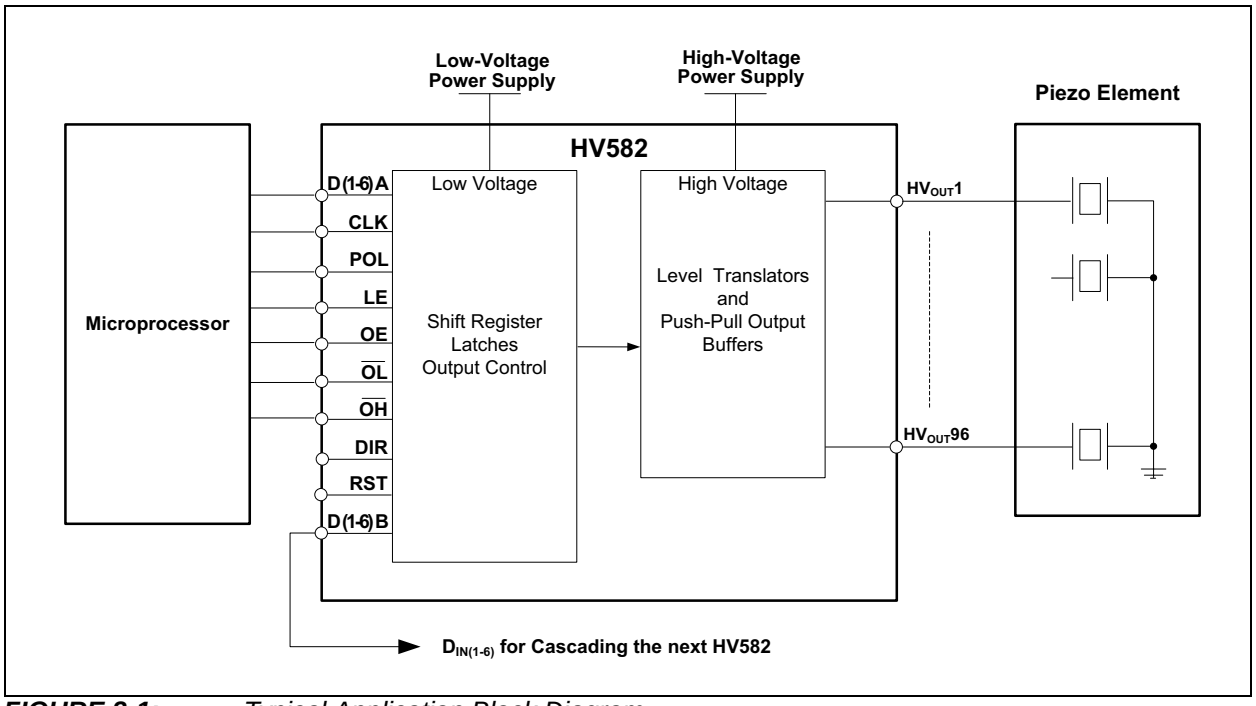
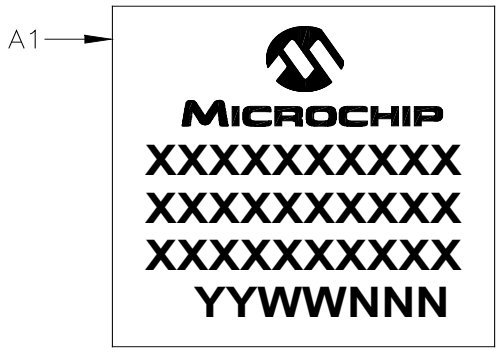


FIGURE 3-1: *Typical Application Block Diagram.*

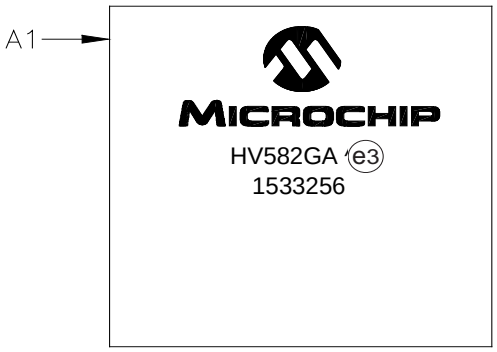
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

169-Ball TFBGA (10 x10 x1.1 mm)



Example

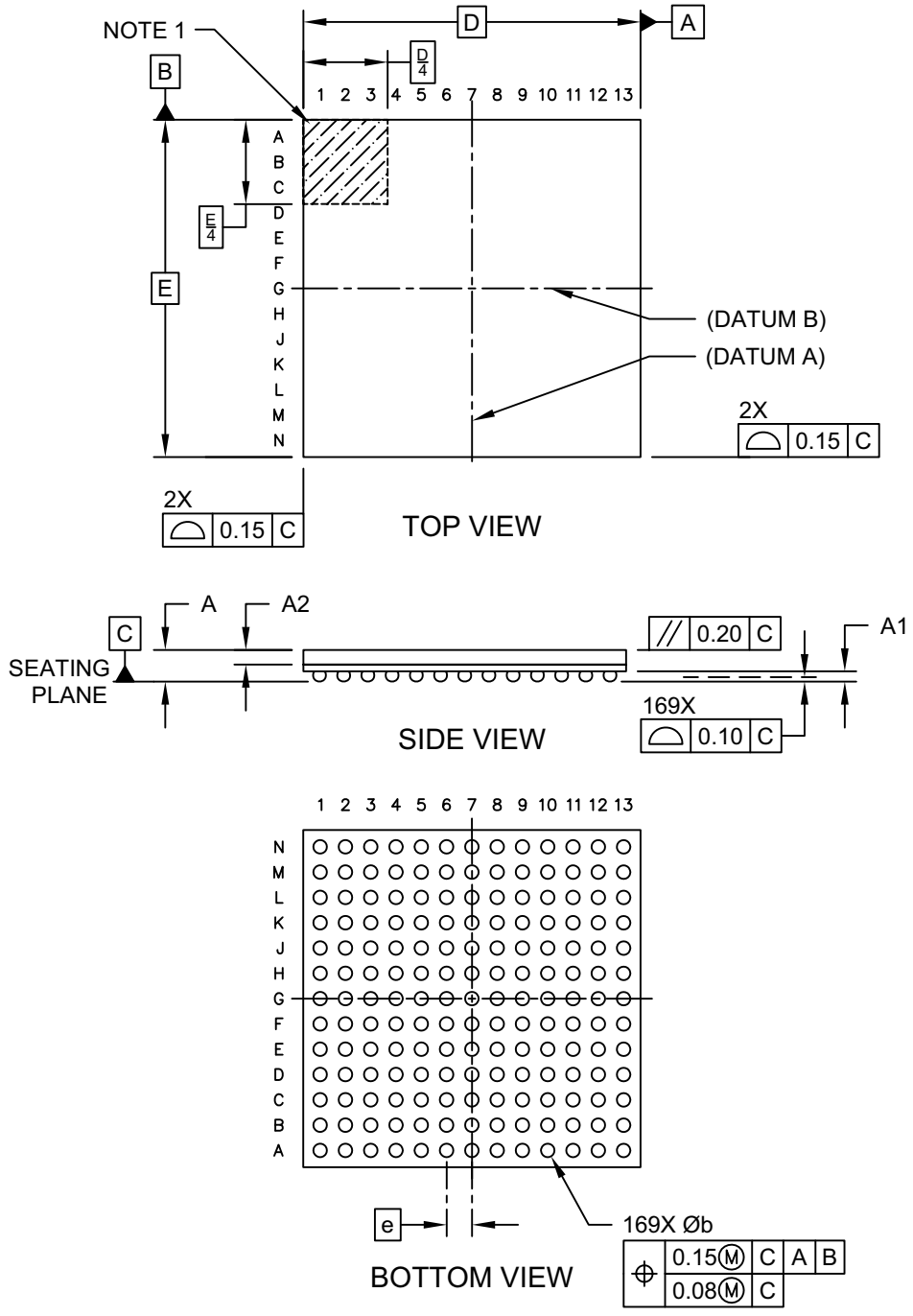


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] (Complies with JEDEC Terminal Assignment recommendations)

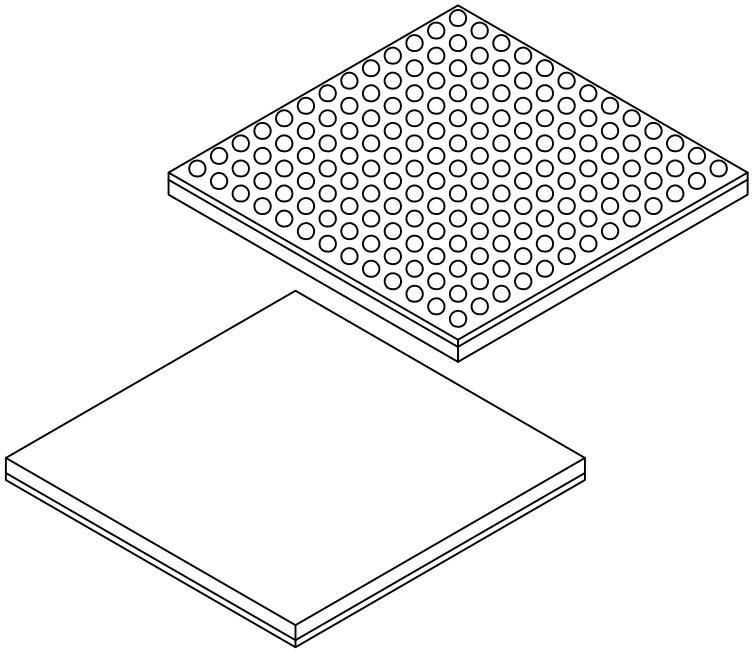
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-377-J Rev C Sheet 1 of 2

169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] (Complies with JEDEC Terminal Assignment recommendations)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		169	
Pitch	e		0.75 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.21	0.32	-
Mold Cap Thickness	A2	0.50	0.45	0.50
Overall Length	D		10.00	
Overall Width	E		10.00	
Ball Diameter	b	0.35	0.40	0.45

Notes:

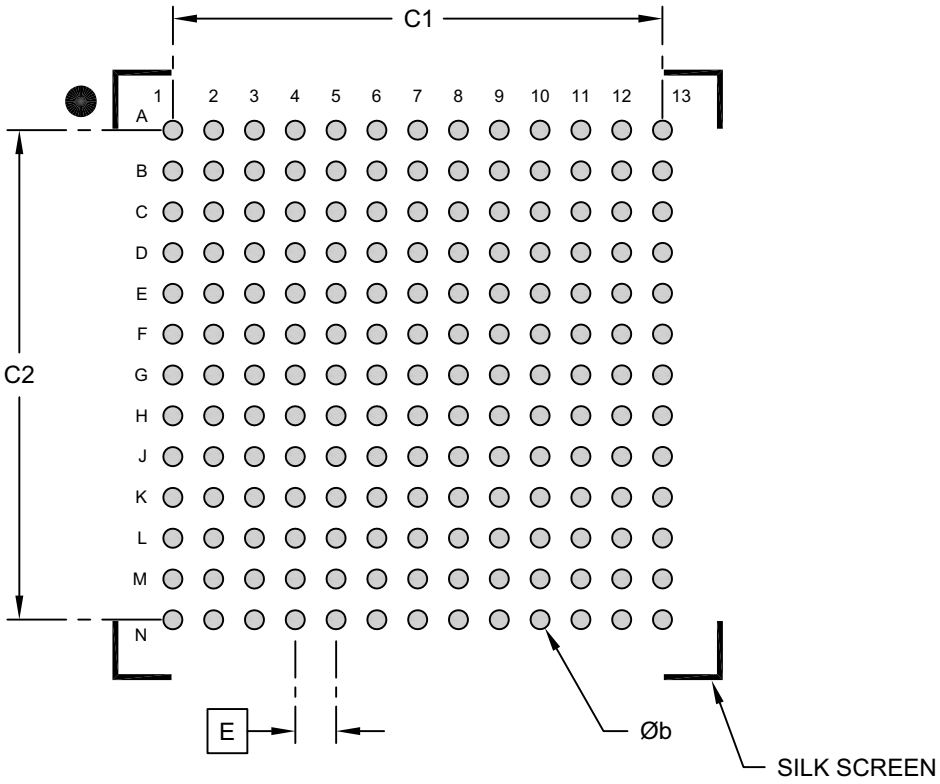
1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-377-J Rev C Sheet 2 of 2

169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] (Complies with JEDEC Terminal Assignment recommendations)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.75 BSC	
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Diameter (X169)	b		0.35	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2377-J Rev C

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX-X
Device	Package

Device:	HV582:		Low-Voltage Serial to High-Voltage Parallel Converter with HV Outputs
Package:	GA-G	=	Thin Fine Pitch Ball Grid Array - 10 x 10 x 1.1 mm Body, 169-lead (TFBGA)

Examples:

a) HV582GA-G: 169-Ball 10x10 TFBGA Package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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