

8-BIT SHIFT REGISTER

SY100S341

FEATURES

- Max. shift frequency of 600MHz
- Max. Clock to Q delay of 1200ps
- IEE min. of -150mA
- Industry standard 100K ECL levels
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75k Ω input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S341 offer eight D-type, edge-triggered flipflops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

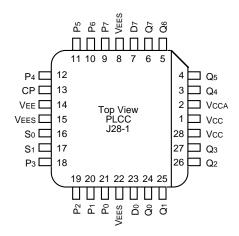
The mode of operation is selected by two Select inputs (S₀, S₁) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have $75k\Omega$ pull-down resistors.

PIN NAMES

Label	Function				
СР	Clock Pulse Input				
S0 — S1	Select Inputs				
D0 — D7	Serial Inputs				
P0 — P7	Parallel Inputs				
Q0 — Q7	Data Outputs				
VEES	VEE Substrate				
VCCA	Vcco for ECL Outputs				

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PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

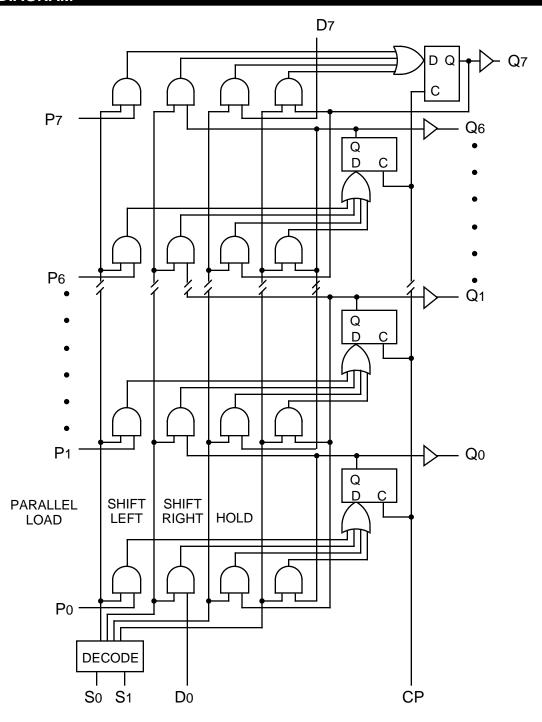
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S341JC	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JCTR ⁽¹⁾	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JZ ⁽²⁾	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S341JZTR ^(1, 2)	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



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TRUTH TABLE

	Inputs				Outputs								
Function	D7	D ₀	S ₁	So	СР	Q7	Q ₆	Q5	Q4	Qз	Q2	Q1	Q ₀
Load Register	Х	Х	L	L	u	P7	P6	P ₅	P4	Рз	P2	P1	P ₀
Shift Left Shift Left	X X	L H	L L	H	u u	Q6 Q6	Q5 Q5	Q4 Q4	Q3 Q3	Q2 Q2	Q1 Q1	Qo Qo	L H
Shift Right Shift Right	L H	X	H	L L	u u	L H	Q7 Q7	Q6 Q6	Q5 Q5	Q4 Q4	Q3 Q3	Q2 Q2	Q1 Q1
Hold Hold Hold	X X X	X X X	H X X	H X X	X H L	No Change							

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

u = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	bol Parameter		Тур.	Max.	Unit	Condition
IIН	Input HIGH Current, All Inputs		_	200	μΑ	VIN = VIH (Max.)
IEE	Power Supply Current	-150	-102	-71	mA	Inputs Open

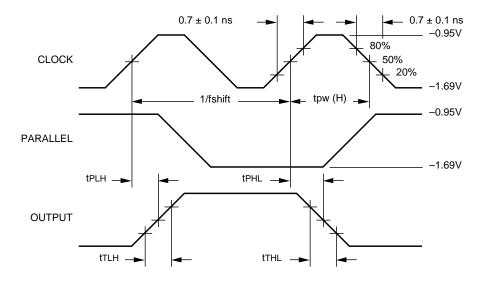
AC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

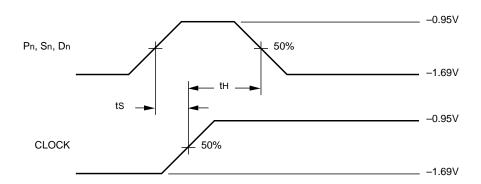
		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
fshift	Shift Frequency	600	_	600	_	600	_	MHz	
tPLH tPHL	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dn, Pn Sn	300 600	_	300 600	_	300 600	_ _	ps	
tH	Hold Time Dn, Pn Sn	300 0	_	300 0	_	300 0	_	ps	
tpw (H)	Pulse Width HIGH, CP	_	600	_	600	_	600	ps	

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TIMING DIAGRAMS



Propagation Delay and Transition Times



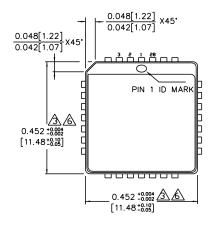
Set-up and Hold Times

Notes:

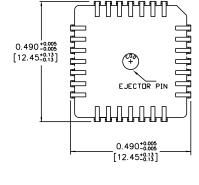
- 1. VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND.
- 2. ts is the minimum time before the transition of the clock that information must be present at the data input.
- 3. th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

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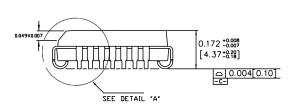
28-PIN PLCC (J28-1)



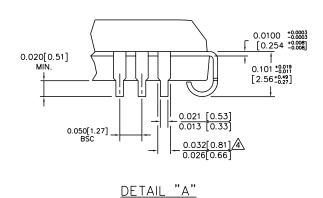
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Rev. A

NOTES:

- DITES:
 DIMENSIONS ARE IN INCHES [MM].
 CONTROLLING DIMENSION: INCHES.
 DIMENSION DOES NOT INCLUDE MOLD FLASH
 OR PROTRUSIONS, EITHER OF WHICH SHALL NOT
 EXCEED 0.008 [0.203].
 LEAD DIMENSION DOES NOT INCLUDE DAMBAR
 PROTRUSION.
 MAXIMUM AND MINIMUM SPECIFICATIONS ARE
 INDICATED AS FOLLOWS: MAX/MIN
 ANCHAGE TOP DIMENSION MAY BE SLIGHTLY
- - PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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