MPM85000

Automotive Power Management Device

Features

- Low-cost, single-chip solution for Automotive Power Management
- Supports low-power *Sleep Mode*; wakeup due to:
  - LIN bus / ECL activity
  - Local event (e.g. ON switch)
  - MOST Network optical/electrical activity
  - *Switch-To-Power* (STP) event
- Power-supply monitoring:
  - Configurable voltage trip points
  - Configurable wakeup from *Sleep Mode* voltage
- Integrated LIN transceiver
  - LIN 2.0 compliant
  - Transmission rates up to 20 kHz
  - MOST *Electrical Control Line* (ECL) compliant
  - Adjustable slew rate for reduced EMI
  - Over-temperature and low-voltage protection
  - Short-circuit protection
  - Optional TXD timeout (MOST ECL compliant)
- Optional I^2C Control Port for configuration/status
- Programmable Precision Reset Generator
- 3.3 V MicroPower Regulator for continuous power requirements (e.g. Rx PHY, EOC/FOR, INIC persistent memory)
- Temperature monitoring with programmable alerts
- User available data storage (while in *Sleep Mode*)
- User available One-Time Programmable (OTP) permanent data storage
- Direct support for MOST INIC power status pins
- 24-pin 4x4 mm^2 QFN package with exposed paddle
- Temperature range: -40 °C to +110 °C

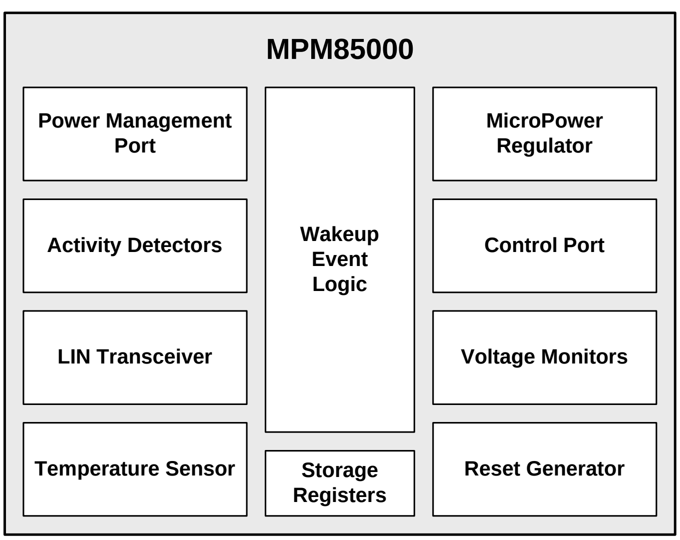
General Description

The MPM85000 is an automotive system power management device intended for integration into an *Electrical Control Unit* (ECU). The MPM85000 includes a very low-power *Sleep Mode*, supporting wakeup transitions to *Active Mode* due to multiple signals. Wakeup event signal detection and qualification includes both glitch protection and power supply validation. Qualified inputs can generate interrupts for an *External Host Controller* (EHC).

The MPM85000 supports all MOST speed grades (MOST25, MOST50, and MOST150). In addition to system power management, other MOST-related features are supported, including: direct connection to power status inputs of MOST *Intelligent Network Interface Controllers* (INICs), MOST50 electrical network (ePHY) activity detection, and ECL support.

In *Active Mode*, the MPM85000 includes a fault-tolerant keep-alive hardware signal (or software bit) that can be used by an external device to keep power enabled until the application is ready to power-down. The MPM85000 also provides continuous monitoring of the application battery voltage and ECU temperature, and can alert the EHC when user-programmed thresholds are crossed.

For robust fault tolerance, stuck wakeup events can be ignored, allowing the MPM85000 to revert to *Sleep Mode*. The MPM85000 detects recovery from stuck conditions and re-enables a signal's ability to wakeup the device.



Ordering Information

Order Number	Package
MPM85000AMT	24-pin QFN (Lead-Free, RoHS Compliant), Tray
MPM85000AMR	24-pin QFN (Lead-Free, RoHS Compliant), Tape and Reel

This table represents valid part numbers at the time of printing and may not represent parts that are currently available. For the latest list of valid ordering numbers for this product, please contact the nearest sales office.

Further Information

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SMSC Europe GmbH
Bannwaldallee 48
D-76185 Karlsruhe
Germany

SMSC
80 Arkay Drive
Hauppauge, New York 11788
USA

Technical Support

Contact information for technical support is available at: http://www.smsc-ais.com/contact.

Legend

Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
msb, lsb	Most significant bit, least significant bit
MSB, LSB	Most significant byte, least significant byte
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Section or Document name.
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don’t care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

TrueAuto™

TrueAuto is SMSC's automotive quality process. It has proven its ability to deliver leading-edge quality and services for IC device products to fulfill the needs of the most demanding automotive customers. TrueAuto is a proven total automotive-grade quality approach. TrueAuto IC device robustness begins with SMSC's design for reliability techniques within the silicon IC itself: automotive-grade robustness and testability are designed into the IC. Once available in silicon, the IC is fully-characterized and qualified over a multitude of operating parameters to prove quality under the harshest conditions. In this, SMSC's TrueAuto approach significantly exceeds the usual automotive reliability standards and customer- specific requirements and goes far beyond the stress tests prescribed by the AEC-Q100 specifications. During the fabrication of TrueAuto products, extensive technologies and processes, such as enhanced monitors are used in order to continuously drive improvements in accordance with SMSC's zero Defects per Million (DPM) goals.

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1 Overview

The MPM85000 is a low-cost, feature-rich *Automotive Power Management Device* (APMD) intended for integration into an *Electrical Control Unit* (ECU). A number of different power architectures exist for automotive ECU systems. In modern automotive infotainment systems, the key-switch position rarely directly controls ECU power, as doing so prohibits advanced network startup and shutdown features (e.g. recalling/saving critical system parameters). Therefore, modern automotive infotainment systems require some type of power management implementation. Although the MPM85000 works well in key-switch managed systems, its feature set is suitable for more advanced power management implementations.

In a networked system with multiple ECUs, continuous battery power is generally supplied to all ECUs, each of which supports a low-power mode of operation in which a majority of the ECU is powered off. In this low-power mode, only the circuitry needed to enable power to the rest of the ECU is active. This power architecture allows the network to power down cleanly, and permits more than one ECU to restore the network to a full-power mode of operation. Power management system architectures are more fully described in the *MOST INIC Hardware Concepts Technical Bulletin [1]*.

To support modern power architectures, the MPM85000 supports two modes of operation: a very low-power *Sleep Mode* and an *Active Mode*. When in *Sleep Mode*, the MPM85000 uses multiple activity detectors to monitor different signals that may indicate the ECU should wakeup from *Sleep Mode*. For robustness, all activity detectors have glitch filters to minimize false wakeup events and the MPM85000 does not exit *Sleep Mode* unless the power supply voltage is within the proper range. Once an activity signal is qualified (and the power supply is valid), the MPM85000 enters *Active Mode* and drives the $\overline{\text{ENABLE}}$ pin low. The $\overline{\text{ENABLE}}$ pin is typically connected to switching-mode power regulators that power the rest of the ECU, as illustrated in Figure 1-1. The MPM85000 also includes a precision reset generator that can be used as an ECU-wide power-on reset (POR) signal.

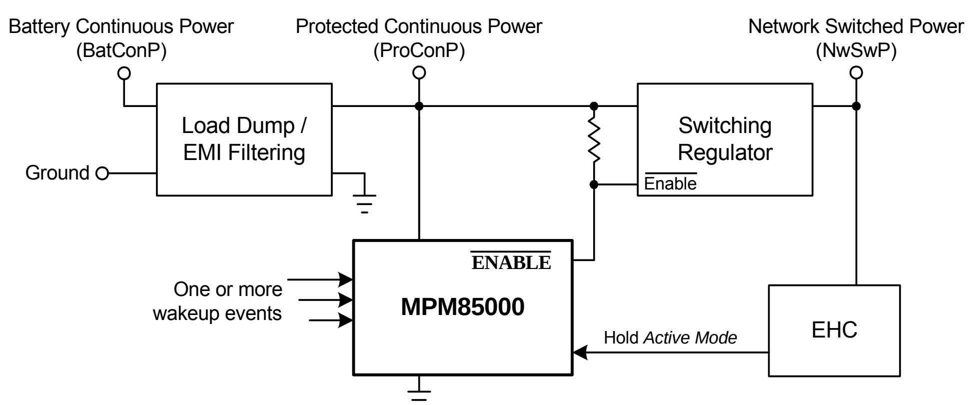


Figure 1-1: Typical ECU Power Arrangement

Once the MPM85000 transitions to *Active Mode*, the ECU is fully powered and the *External Host Controller* (EHC) can keep the MPM85000 in *Active Mode* until the device is ready to be powered down. This MPM85000 “hold” *Active Mode* feature is fault-tolerant and supports either a hardware signal or a register bit. If the MPM85000 transitions to *Active Mode* and the EHC never responds, the MPM85000 returns to *Sleep Mode* on its own to keep from draining the battery. If the EHC is reset due to a fault condition, the MPM85000 delays entering *Sleep Mode* to allow the EHC time to recover from the reset condition.

The MPM85000 can operate without EHC configuration or interaction (defined as stand-alone operation). However, additional features are available when an EHC is connected to the MPM85000 Control Port, including power supply monitoring and status information, system temperature monitoring and status information, the ability to change the voltage monitoring thresholds, and also the ability to adjust the reset active time period.

The MPM85000 meets the power management requirements of the MOST Network *[2]* and includes a number of features specifically designed to support MOST Networks. With respect to wakeup event options, the MPM85000 is designed to wakeup due to MOST optical network activity (from the fiber-optic receiver/optical-electrical converter, FOR/OEC), and also can wakeup due to MOST50 electrical network activity. The integrated LIN transceiver can also wakeup the MPM85000 from *Sleep Mode* as a result of standard LIN communications *[3]*, or activity on a MOST Network Electrical Control Line (ECL) *[4]*. The MPM85000 also supports local wakeup events through the **ON_SW** pin, and can support diagnostic *Switch-To-Power* (STP) event detection, when enabled.

An on-chip 3.3 V MicroPower regulator supplies constant power to ECU circuitry that requires power during *Sleep Mode* (e.g. FOR/OEC, Rx PHY). When used with MOST ROM INIC devices, the MicroPower regulator provides *Sleep Mode* power for their persistent memory requirements.

Utilizing the MPM85000 for ECU power management simplifies design requirements and saves PCB real estate usage, supporting faster development time and lower overall cost. In addition, many fault-tolerant features are available in ECU designs that include the MPM85000 which do not exist in discrete solutions.

1.1 Functional Blocks

The MPM85000 features can be divided into the following functional blocks, as shown in Figure 1-2:

- ***Wakeup Event Logic*** - Provides an output for controlling application regulators (wakeup from *Sleep Mode*) based on configurable parameters and actual conditions detected by other MPM85000 functional blocks. Supports the two MPM85000 operational modes: *Sleep Mode* and *Active Mode*.
- ***Power Management Port*** - Intended for direct connection to a MOST INIC or an EHC.
  - Status outputs report STP events and voltage information from the internal voltage monitor
  - Keep-alive input for a controlled node shutdown (forces the wakeup event logic to hold the power control output active until the application is ready to power down)
- ***Activity Detectors*** - Used to detect and qualify activity on various inputs.
  - LIN Transceiver activity detection / MOST ECL activity detection
  - MOST50 electrical network (ePHY) activity detection
  - MOST25/MOST150 optical network (FOR/EOC, Rx PHY) activity detection
  - Local application wakeup event, such as an external push-button switch (with debouncing)
- ***LIN Transceiver*** - Provides a bi-directional pin for connection to a standard LIN bus *[3]*, with independent transmit and receive signals level-shifted to 3.3 V logic for connection to the EHC. Designed for MOST ECL compliance with many fail-safe features.
- ***Temperature Sensor*** - Detects when programmed temperature thresholds are crossed and can alert the EHC. Simplifies the implementation of MOST Network over-temperature condition management.
- ***MicroPower Regulator*** - Provides a constant 3.3 V output to supply external devices/circuitry that must be continuously powered. Typically used for external circuitry that must remain powered through *Sleep Mode*, such as MOST optical receivers (FOR/OEC) and MOST ROM INIC persistent memory supplies.
- ***Control Port*** - Supports optional I^2C bus *[5]* slave device implementation for communication with the EHC. Provides access to internal control and status registers, with an interrupt output signal to notify the EHC of various application events.

- ***Voltage Monitors*** - Used for power supply (battery) voltage monitoring.
  - Supports configurable wakeup from *Sleep Mode* voltage regions to ensure the battery voltage is high enough for ECU operation
  - Monitors the supply for over- and under-voltage events during *Active Mode*
  - Includes an optional *Switch-To-Power* (STP) pulse detector for legacy MOST Network systems *[6]* that support this feature
- ***Reset Generator*** - Provides a programmable system reset output based on a 3.3 V input voltage that can be used as a system-wide power-on reset (POR) after regulators stabilize. Also monitors for external reset events.
- ***Storage Registers*** - Provides two types of storage registers for general purpose customer use. Each register is 8 bits wide (1 byte of storage).
  - 16 RAM-based registers which maintain their values through *Sleep Mode* (see Section 10.2.13)
  - 56 One-Time-Programmable (OTP) registers which maintain their data through *Sleep Mode* and also through disruptions to continuous battery power (see Section 10.2.14 for more information).

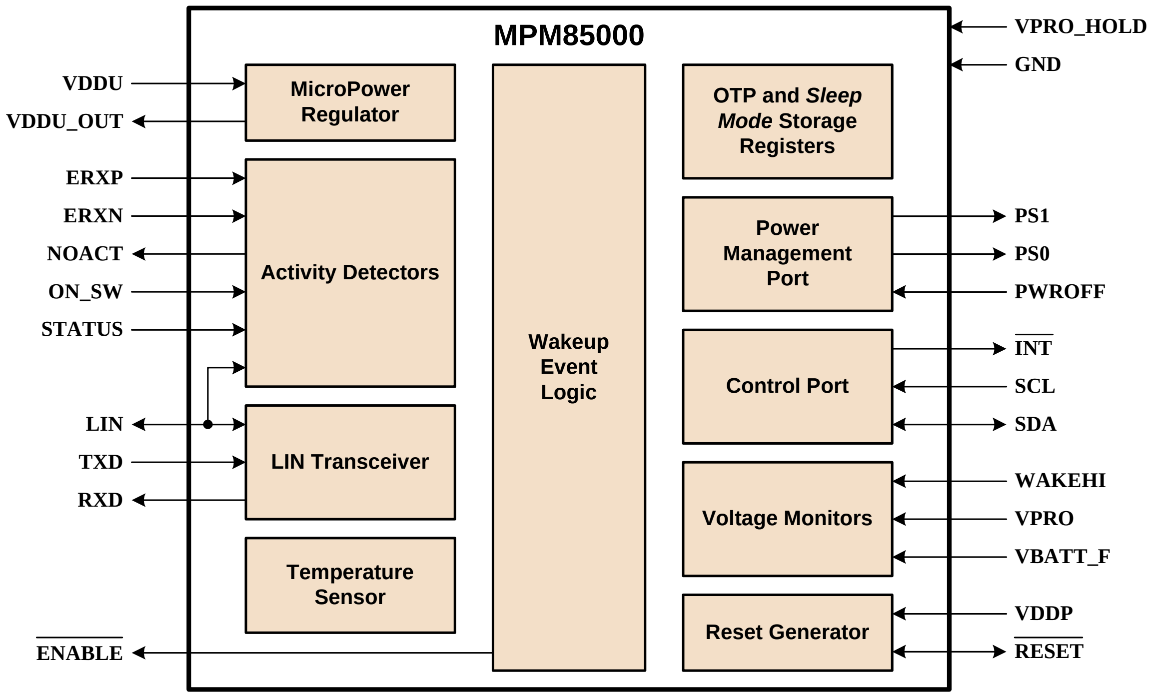


Figure 1-2: Functional Blocks

1.2 ECU Connection Examples

The MPM85000 includes many optional features, not all of which are intended for use in any one design. Figure 1-3 illustrates an ECU block diagram that utilizes the MPM85000 in a stand-alone capacity, without EHC configuration through the Control Port. This block diagram supports wakeup from *Sleep Mode* via the LIN bus. The MPM85000 reset generator provides the power-on reset (POR) for the entire module. Although not shown, the Power Management Port can provide the EHC with power supply monitoring information (using the **PS1**/**PS0** pins), as needed. For ECUs that need to support local wakeup event capabilities during *Sleep Mode*, the MPM85000 MicroPower regulator provides continuous power and either the **STATUS** or **ON_SW** pins signal the local wakeup event. Refer to the *MOST INIC Hardware Concepts Technical Bulletin [1]* for more information regarding local wakeup events.

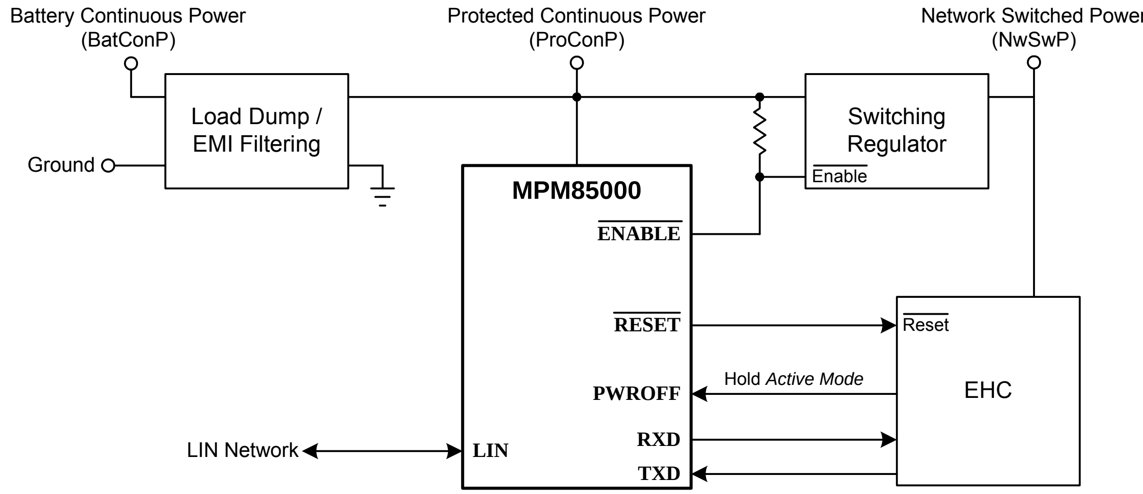


Figure 1-3: LIN Network Stand-Alone Block Diagram

Figure 1-4 on page 10 illustrates a typical MOST optical network ECU block diagram. In this example, the MPM85000 reset generator provides the reset signal to the MOST INIC device while the Power Management Port conveys power states to the INIC. The example also shows two non-local wakeup events: MOST Network activity (FOR activity signal tied to the **STATUS** pin) and the MOST ECL signal (connected to the **LIN** pin). Although the EHC could use the **RXD** and **TXD** pins for MOST ECL, this example assumes the EHC is using register bits (through the Control Port) to manage the **LIN** pin, thereby saving hardware pins. The continuous power required by the FOR is provided by the MPM85000 MicroPower regulator (**VDDU** pin). The **ON_SW** pin remains available for local wakeup events. Since the EHC is connected to the Control Port, it can use the MPM85000 OTP storage registers for end-of-line configuration options and use the RAM-based storage registers for volatile settings which must be restored when returning to *Active Mode*.

Figure 1-5 on page 10 illustrates a typical MOST50 electrical network ECU block diagram supporting ePHY network activity detection and qualification. The MPM85000 MicroPower regulator output is not connected to a network receiver, as the electrical network front-end is passive; however, the **VDDU** pin does supply power to the persistent memory voltage pin of the ROM INIC.

These figures provide general information and are just a few examples of how the MPM85000 can be utilized in both MOST and non-MOST applications to save cost and increase robustness for automotive ECUs. For more detailed MPM85000 usage information, see Chapter 13, *Application Information*.

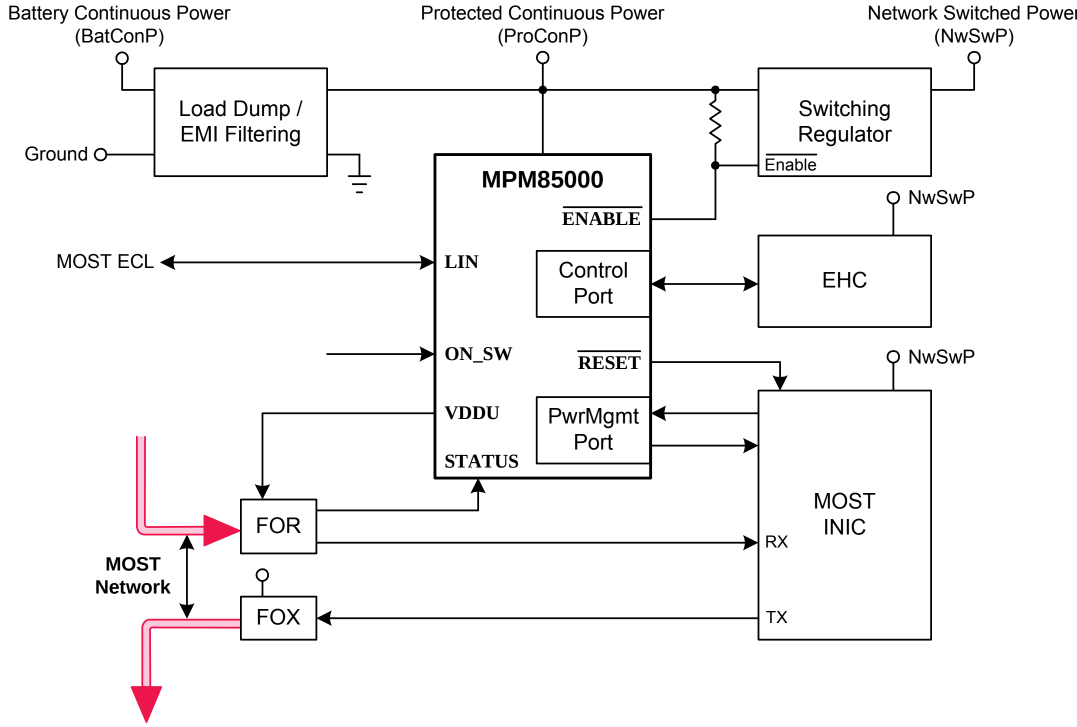


Figure 1-4: MOST Optical Network Block Diagram

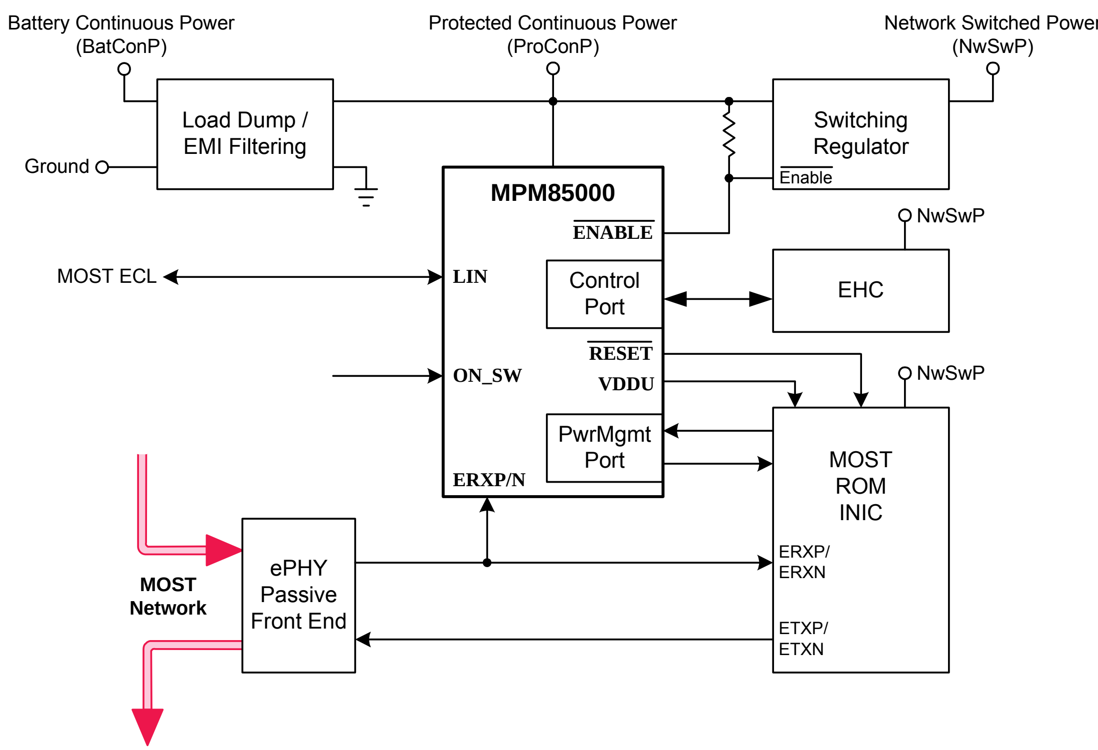


Figure 1-5: MOST50 Electrical Network Block Diagram

2 Pinout

Input pins must not be left floating; therefore, they must be driven, have pull-ups or pull-downs, or be tied directly to one of the appropriate power or ground pins.

Digital pins that can be configured as outputs (e.g. $D_{I/OD}$) are high impedance during initial power-up, except **NOACT**. The “Type” column indicates the pin type, defined in Section 2.3.

2.1 Pinout List

Pin	Name	Type	Logic Block	Description
1	STATUS	D_{IN}	Activity Detector	Local wakeup event input (active low). In optical systems, this pin is typically connected to the Fiber Optic Receiver (FOR) status output, which signals optical network activity. Tie to 3.3 V continuous power (**VDDU**) if unused.
2	VDDU_OUT	A_{OUT}	MicroPower Regulator	Power supply output. This pin provides a 3.3 V continuous power supply, which can be used to power external application circuitry, such as the FOR/OEC and/or INIC persistent memory.
3	VDDU	A_{IN}	MicroPower Regulator	Feedback input. This pin must either be connected directly to **VDDU_OUT** or to the emitter of an external NPN pass transistor when additional current is required by the application.
4	ERXP	A_{IN}	Activity Detector	Positive differential input of ePHY receive circuit. Tie to ground if unused.
5	ERXN	A_{IN}	Activity Detector	Negative differential input of ePHY receive circuit. Tie to ground if unused.
6	NOACT [1]	D_{OUTD}	Activity Detector	ePHY network activity indicator (active low). The MPM85000 drives this pin active when valid ePHY activity exists on **ERXP/ERXN**. Pull-up resistor to the 3.3 V switched supply is required. Tie to ground if unused.
7	GND			Ground
8	VBATT_F [2]	A_{IN}	Voltage Monitor	*Switch-To-Power* (STP) event monitor input. This pin should be connected to the battery voltage (prior to load dump filtering) through a 27 kΩ (1/4 W) series resistor. If STP event detection is not required, tie this pin to ground.
9	VPRO [2]	A_{IN}	Voltage Monitor	Monitored input from the battery supply. This pin also powers the LIN transceiver. This pin should be connected to the protected battery voltage (after the load dump filter) with a 200 Ω (1/2 W) series resistor.
10	VPRO_HOLD			Main power supply input for the MPM85000 12 V core. This pin is typically tied directly to **VPRO**.
11	LIN	$D_{I/OD}$	LIN Transceiver	LIN bus input/output signal, internally pulled high to **VPRO**. This pin may be used as a wakeup event input supporting either LIN bus or MOST ECL. Leave floating if unused.
12	$\overline{\text{ENABLE}}$ [1]	D_{OUTD}	Wakeup Event Logic	Enable control signal (active low) for external voltage regulators. This pin is High-Z in *Sleep Mode* and driven low in *Active Mode*. A pull-up resistor is required; however, the voltage level and circuit configuration depends on the requirements of the external regulator.

1. Pull-up resistor required.
2. Series resistor required.

Table 2-1: Pinout List

Pin	Name	Type	Logic Block	Description
13	VDDP [2]	A_{IN}	Reset Generator	Monitored input from external application voltage regulator. Requires 1 kΩ series resistor to the 3.3 V switched supply. If the reset generator is not used, this pin must remain connected to 3.3 V switched power through the 1 kΩ resistor.
14	RXD [1]	D_{OUTD}	LIN Transceiver	LIN bus output (from LIN bus to EHC). Pull-up resistor to the 3.3 V switched supply is required. Tie to ground if unused.
15	TXD	D_{IN}	LIN Transceiver	LIN bus input (from EHC to LIN bus). A pull-up resistor is recommended to set the initial state during EHC power-up/reset. Tie to the 3.3 V switched supply if unused.
16	WAKEHI	D_{IN}	Voltage Monitor	Power-up configuration input. At initial power-up, the sampled value of this pin sets the default state of the **CR.WAKECV** bit. This pin is used to control the lower boundary of the *Allowed Wakeup Range* (see Section 4.1) for initial power-up. Tie to either 3.3 V continuous power (**VDDU**) or ground.
17	$\overline{\text{RESET}}$ [1]	$D_{I/OD}$	Reset Generator	External device reset output signal (active low). This pin is asserted based on the input voltage at the **VDDP** pin and is also monitored to detect external reset conditions. A pull-up resistor to the 3.3 V switched supply is required. If the reset generator is not used, this pin must still be connected to 3.3 V switched power through a resistor (15-100 kΩ range) while remaining disconnected from the application.
18	PWROFF	D_{IN}	Power Management Port	Power-down control input signal. External devices (EHC or INIC) drive this signal low to keep the MPM85000 in *Active Mode* until they are ready to be powered down. A pull-up resistor to the 3.3 V switched supply is recommended so that external devices release this signal high when reset. Tie to the 3.3 V switched supply if unused.
19	PS0 [1]	D_{OUTD}	Power Management Port	Power status output signal. Together with **PS1**, this pin indicates coded power status to the INIC or the EHC. Pull-up resistor to the 3.3 V switched supply is required. Tie to ground if unused.
20	PS1 [1]	D_{OUTD}	Power Management Port	Power status output signal. Together with **PS0**, this pin indicates coded power status to the INIC or the EHC. Pull-up resistor to the 3.3 V switched supply is required. Tie to ground if unused.
21	$\overline{\text{INT}}$ [1]	D_{OUTD}	Control Port	Interrupt output (active low). The MPM85000 drives this line active to signal various power management interrupt events (defined in Section 10.1) to an external controller. Pull-up resistor to the 3.3 V switched supply is required. Tie to ground if unused.
22	SDA [1]	$D_{I/OD}$	Control Port	Data input/output signal for I^2C communication with an external controller. Pull-up resistor to the 3.3 V switched supply is required. Tie to the 3.3 V switched supply if unused.
23	SCL [1]	D_{IN}	Control Port	Clock input signal for I^2C communication with an external controller. Pull-up resistor to the 3.3 V switched supply is required. Tie to the 3.3 V switched supply if unused.
24	ON_SW	D_{IN}	Activity Detector	Application wakeup event input signal (active low), internally pulled high to **VDDU**. This pin is provided for use as a general-purpose, local application event - either real or simulated. If unused, tie to 3.3 V continuous power (**VDDU**) or leave floating.

1. Pull-up resistor required.
2. Series resistor required.

Table 2-1: Pinout List (Continued)

Pin	Name	Type	Logic Block	Description
TAB	GND			The paddle of the QFN package should be soldered to the ground plane for efficient heat dissipation.

1. Pull-up resistor required.
2. Series resistor required.

Table 2-1: Pinout List (Continued)

2.2 Pinout

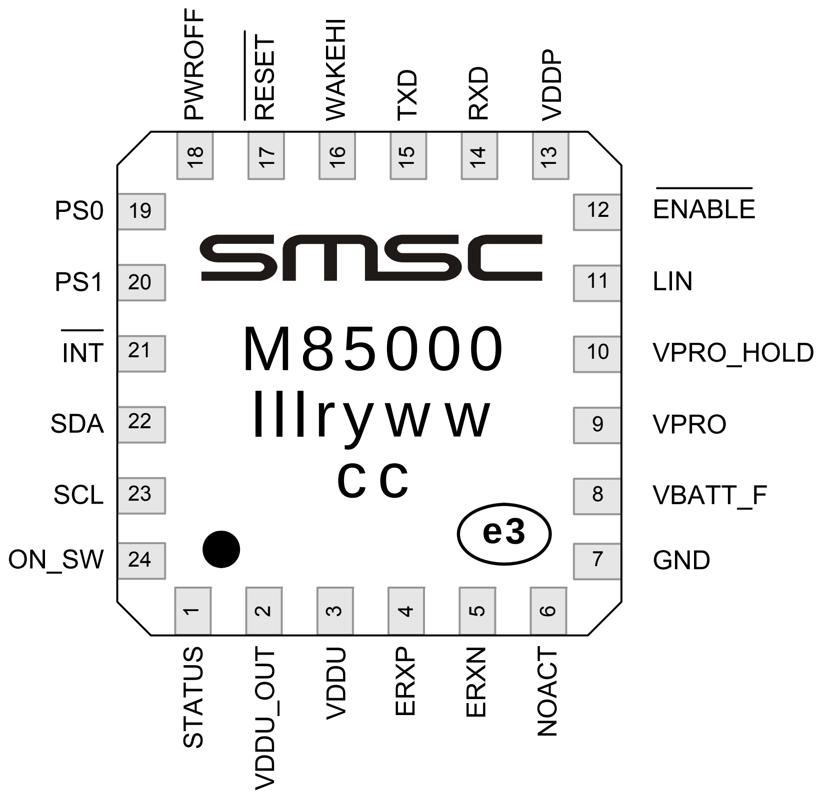


Figure 2-1: Pinout (Topside)

The package designators are:

- lll - Lot Sequence Code
- r - Chip Revision Letter
- y - last digit of Assembly Year
- ww - Assembly Work Week
- cc - Country of Origin Abbreviation (up to 2 characters)
- e3 - Pb Free Symbol

2.3 Equivalent Schematics for Pins

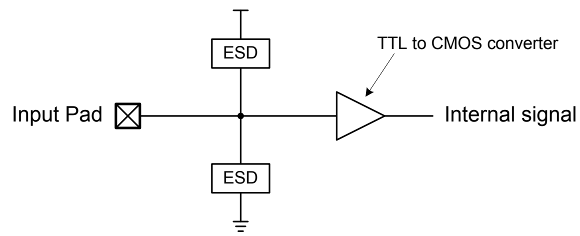


Figure 2-2: Pin-equivalent for Digital Input pin - D_{IN}

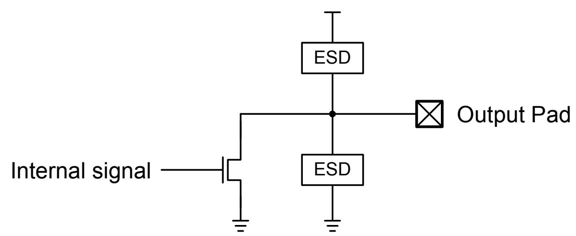


Figure 2-3: Pin-equivalent for Open-Drain Digital Output pin - D_{OUTD}

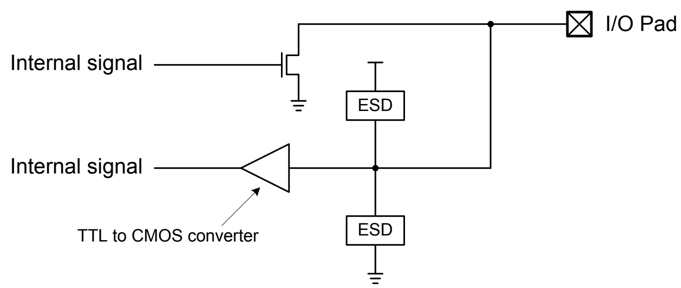


Figure 2-4: Pin-equivalent for Digital Input/Open-Drain Output pin - $D_{I/OD}$

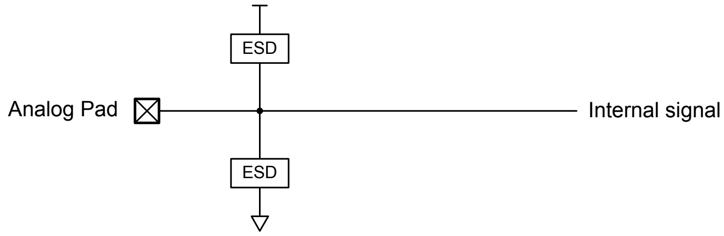


Figure 2-5: Pin-equivalent for Analog Input/Output pin - $A_{I/O}$

3 Operational Modes

The MPM85000 supports two basic modes of operation:

- *Sleep Mode* - minimal circuitry active; waiting for wakeup events (ECU powered down).
- *Active Mode* - all circuits are active (normal ECU operation).

When power is initially applied to the ECU and the **VPRO** supply is above the **WAKEHI** threshold, the MPM85000 begins operating in *Active Mode* and the **$\overline{\text{ENABLE}}$** pin is driven low to enable the external voltage regulator(s). If no qualified activity is detected after the EHC powers up (and the EHC has not made any changes the MPM85000's configuration registers that would prevent power-down), the MPM85000 reverts to *Sleep Mode* and releases the **$\overline{\text{ENABLE}}$** pin by placing it in a high-impedance state.

In *Sleep Mode*, all non-critical circuitry is disabled to minimize power. Only the internal logic required to detect and qualify wakeup events is enabled. The following five events (in addition to initial power being applied) can trigger a transition from *Sleep Mode* to *Active Mode*:

- Valid activity detected on the **LIN** pin (active low). Used for LIN bus *[3]* or MOST ECL *[4]* wakeup and communication.
- Valid activity detected on the **STATUS** pin (active low). Connected to the FOR/OEC in MOST optical systems to permit wakeup from optical network activity. Can be used as a local wakeup event input in other applications.
- Valid network activity detected on the **ERXP**/**ERXN** pins (for MOST50 electrical networks),
- Valid activity detected on the **ON_SW** pin (active low). This pin is intended for general purpose local wakeup events, such as a power-on switch.
- Diagnostic *Switch-To-Power* (STP) event detected and qualified. When this feature is enabled, the MPM85000 detects STP pulses on the battery supply.

In any particular system, not all these wakeup events are used. For example, the **ERXP**/**ERXN** pins are only used in MOST50 electrical network systems to detect and wakeup as the result of electrical network activity. These pins would not be used (tied to ground) in non-MOST or MOST optical systems.

All input activity is qualified with glitch suppression to prevent erroneous wakeup events. Additionally, these wakeup events only trigger a transition to *Active Mode* if the power supply voltage monitor (**VPRO**) is within the *Allowed Wakeup Range* ($V_{WakeupRange}$), which is a requirement of the *MOST Specification [2]*. The $V_{WakeupRange}$ levels are programmable and are only used to qualify a transition from *Sleep Mode* to *Active Mode*. Once in *Active Mode*, $V_{WakeupRange}$ is not considered when transitioning back to *Sleep Mode*.

Figure 3-1 shows a conceptual diagram of the MPM85000 wakeup event logic. For simplicity, the timers for glitch suppression are omitted from each activity input signal.

The *Allowed Wakeup Range* ($V_{WakeupRange}$) always includes the U_{Normal} region and may optionally include the U_{Super} and $U_{Critical}$ regions; however, $V_{WakeupRange}$ never includes the U_{Low} region. The **CR.WAKESV** bit sets the upper bound of $V_{WakeupRange}$ by determining if the MPM85000 is permitted to wakeup in the U_{Super} region while the **CR.WAKECV** bit determines if the MPM85000 is permitted to wakeup in the $U_{Critical}$ region. Furthermore, the initial power-up state of the **CR.WAKECV** bit is determined by the **WAKEHI** configuration pin. The various power supply regions are defined by their respective programmable thresholds: V_{Th_Low}, $V_{Th\_Critical}$, and V_{Th_Super} (see Section 4.1 for more information).

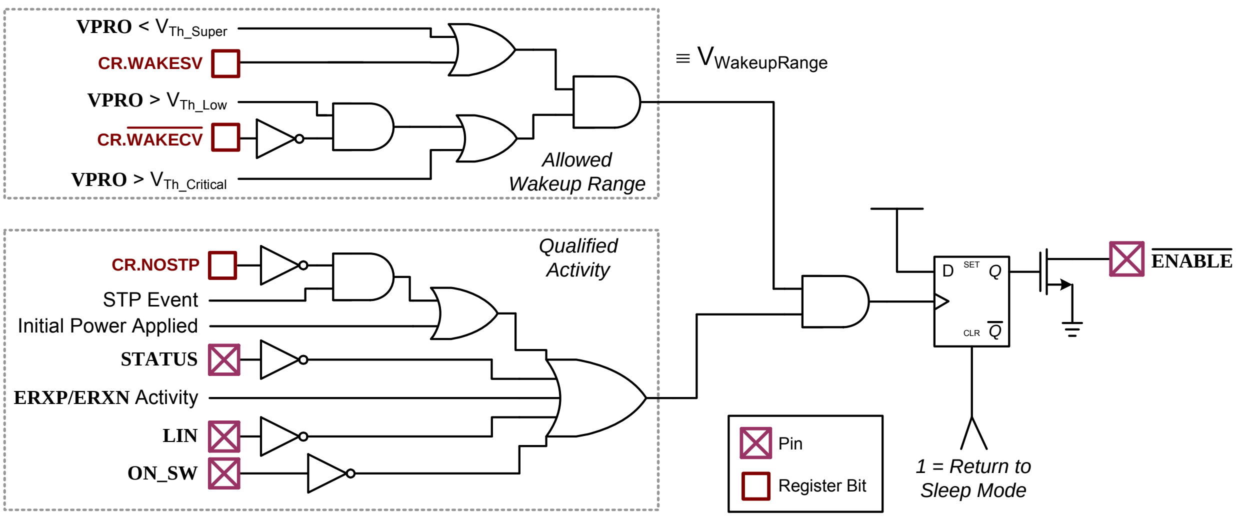


Figure 3-1: Wakeup Event Logic (Conceptual Diagram)

When a wakeup event is qualified and the power supply is in the *Allowed Wakeup Range*, the MPM85000 enters *Active Mode* and drives **ENABLE** low. After entering *Active Mode*, the MPM85000 gives the application time to initialize (t_{WACK}) before considering a transition back to *Sleep Mode*. This timer allows the external device time to drive **PWROFF** low (or set the **OR.HOLD** bit) after powering up. If **PWROFF** is driven low or **OR.HOLD** is set prior to expiration of the t_{WACK} timer, the timer is reset, and the MPM85000 remains in *Active Mode*. The t_{WACK} application initialization timer is more robust than standard LIN transceivers or discrete circuits that latch the wakeup event. The MPM85000 reverts back to *Sleep Mode* if **PWROFF** or **OR.HOLD** are never asserted, and qualified activity is no longer detected. This behavior prevents a failure from keeping the ECU in *Active Mode* and draining the battery.

Figure 3-2 illustrates the MPM85000 logic for reverting to *Sleep Mode*. Four conditions must all be met for the MPM85000 to release the **ENABLE** pin and return to *Sleep Mode*:

- No qualified activity on any of the wakeup event input pins (unless **VPRO** is within the U_{Low} region)
- **PWROFF** input high and the **OR.HOLD** bit cleared for at least t_{POFF_DEL}.
  - The t_{POFF_DEL} delay is disregarded if **VPRO** within U_{Low}.
  - Additionally, a **VDDP** invalid condition (defined in Chapter 7, *Reset Generator and VDDP*) overrides the **PWROFF** pin and **OR.HOLD** bit.
- Minimum time elapsed from a transition on **RESET**.
  - t_{RST_POFF} from falling edge (to detect **RESET** stuck low)
  - t_{WACK} from rising edge (to allow external device, such as INIC/EHC, time to recover)
- Minimum time in *Active Mode* elapsed (t_{WACK} time from **ENABLE** going low)

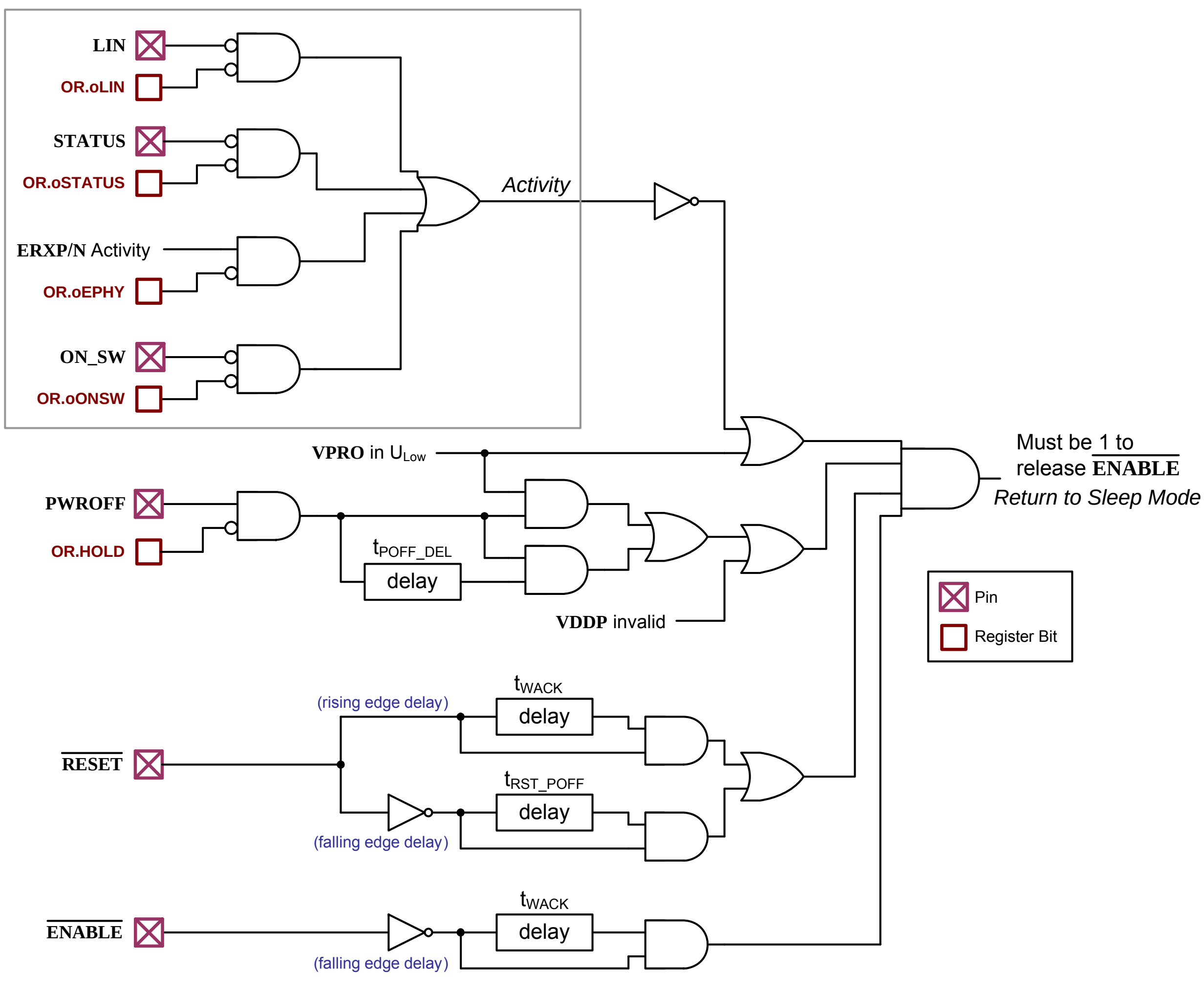
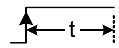
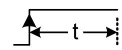
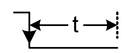
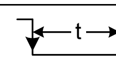


Figure 3-2: Sleep Mode Logic (Conceptual Diagram)

As shown in Figure 3-2 on page 17, **LIN**, **STATUS**, and **ON_SW** pins are active low (logic low level corresponds to activity detected). For robustness, bits in the *Override Register* (OR) (see Section 10.2.7) allow any of these inputs or ePHY activity to be ignored; thereby allowing the MPM85000 to return to *Sleep Mode* in the case of a stuck input condition. If the stuck input is cleared, the corresponding OR bit is automatically cleared to allow the device to wakeup when activity returns on that input.

Table 3-1 lists different scenarios that cause the MPM85000 to enter *Sleep Mode* (power down). For simplicity, Table 3-1 only lists **PWROFF**, but the **OR.HOLD** register bit works similarly. Therefore, the following scenarios assume that **OR.HOLD** is cleared. The "Activity" column references the *Activity* signal shown in Figure 3-2 on page 17, which comes from at least one of the four input pins.

	Sleep Mode Transition Scenarios	Activity	PWROFF	VPRO	$\overline{\text{RESET}}$
1	**PWROFF** released	0	 t > t_{POFF_DEL}	> U_{Low}	1
2	**PWROFF** released; **VPRO** within U_{Low}	don't care		U_{Low}	1
3	All activity ceases (t_{WACK} already expired)		1	> U_{Low}	1
4	t_{WACK} expires	0	1	don't care	 t > t_{WACK}
5	$\overline{\text{RESET}}$ stuck low; external reset	0	1	don't care	 t > t_{RST_POFF}
6	Internal reset (**VDDP** invalid)	0	don't care	don't care	 t > t_{RST_POFF}

Cells containing a transition (edge marked with an arrow) indicate the reason for reverting to *Sleep Mode*.

Table 3-1: Power Down Scenarios

Scenario 1 is the typical case, where all qualified input activity ceases. When no activity has occurred for a period of time ($t_{PwrSwitchOffDelay}$ *[2]* for MOST Network designs), then the external device (INIC/EHC) releases **PWROFF**, and the MPM85000 reverts to *Sleep Mode* after t_{POFF_DEL} expires.

Scenario 2 is similar to Scenario 1, except the **VPRO** supply is in the U_{Low} region. In this case, t_{POFF_DEL} is ignored to allow a faster transition to *Sleep Mode* when the ECU supply is collapsing. Since the ECU supply is collapsing, qualified activity is ignored (consistent with *MOST Specification [2]* requirements).

Scenario 3 would generally be caused by a faulty ECU module, where **PWROFF** was never pulled low and the initial POR t_{WACK} timer expires, but input activity keeps the MPM85000 in *Active Mode*. Therefore, when all qualified activity ceases, the MPM85000 reverts to *Sleep Mode*.

Scenario 4 is similar to 3, except input activity ceases before the t_{WACK} timer expires. The t_{WACK} timer keeps the MPM85000 in *Active Mode*, to give the external device (INIC/EHC) time to initialize and pull **PWROFF** low. In this scenario, **PWROFF** is never pulled low, so the MPM85000 reverts to *Sleep Mode* once t_{WACK} expires (fail-safe feature to save battery power).

Scenario 5 is a robustness feature that allows the MPM85000 to enter *Sleep Mode* if an external device holds $\overline{\text{RESET}}$ low for longer than t_{RST_POFF} (faulty reset is assumed).

Scenario 6 is a result of the **VDDP** voltage dropping to the point where the reset generator asserts $\overline{\text{RESET}}$ (**VDDP** invalid condition). In a typical system **PWROFF** is pulled-up to **VDDP**; therefore, if **VDDP** is invalid, then **PWROFF** becomes invalid and cannot be relied upon. In this scenario, **PWROFF** is ignored and cannot hold the MPM85000 in *Active Mode*.

The following three figures illustrate the power down scenarios defined in Table 3-1 (two scenarios shown per figure). In each figure, qualified activity is represented by just one of the four activity inputs; however, activity on any of the other three inputs would result in the same behavior.

Figure 3-3 illustrates two power cycles that utilize the **STATUS** pin as the wakeup event while the **PWROFF** pin is used by an external device (e.g. INIC/EHC) to keep the MPM85000 in *Active Mode*. When qualified activity ceases (**STATUS** goes high), the external device is notified and should release the **PWROFF** pin when appropriate, which causes the MPM85000 to revert to *Sleep Mode*.

The first power cycle in Figure 3-3 depicts scenario 1 (listed in Table 3-1). After input activity ceases, **PWROFF** is released to revert to *Sleep Mode*. The second power cycle depicts scenario 2, when **VPRO** dips into the U_{Low} region. When the external device is notified about the power dropping, it prepares for power down, then releases **PWROFF**. This causes **ENABLE** to be released regardless of input activity.

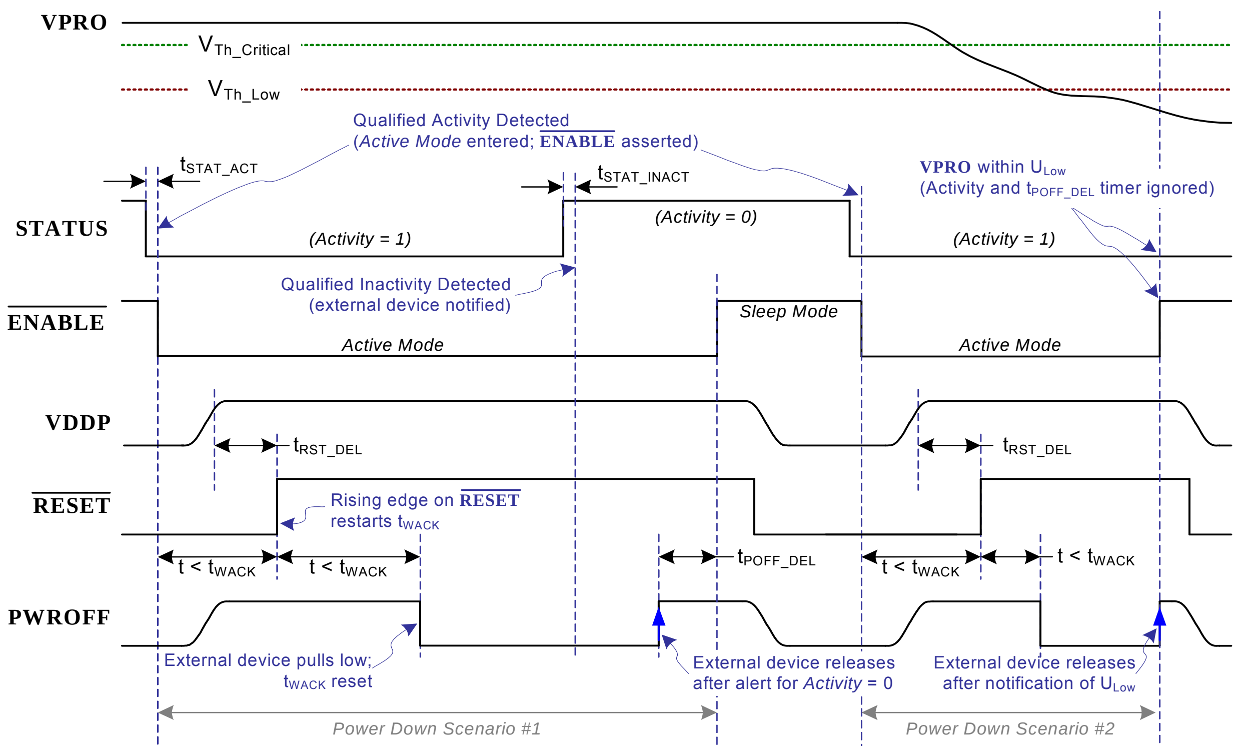


Figure 3-3: Typical Power Cycle (Scenarios 1 and 2)

The first power cycle in Figure 3-4 depicts scenario 3 (listed in Table 3-1). After entering *Active Mode*, **PWROFF** is never driven low and the t_{WACK} timer expires; however, the ePHY input is still active. Once ePHY activity ceases, the MPM85000 reverts to *Sleep Mode*. The second power cycle depicts scenario 4, where the ePHY activity ceases soon after entering *Active Mode*, but the t_{WACK} timer keeps the MPM85000 in *Active Mode*. Since **PWROFF** is never driven low by the external device (fault condition), the MPM85000 reverts to *Sleep Mode* once t_{WACK} expires.

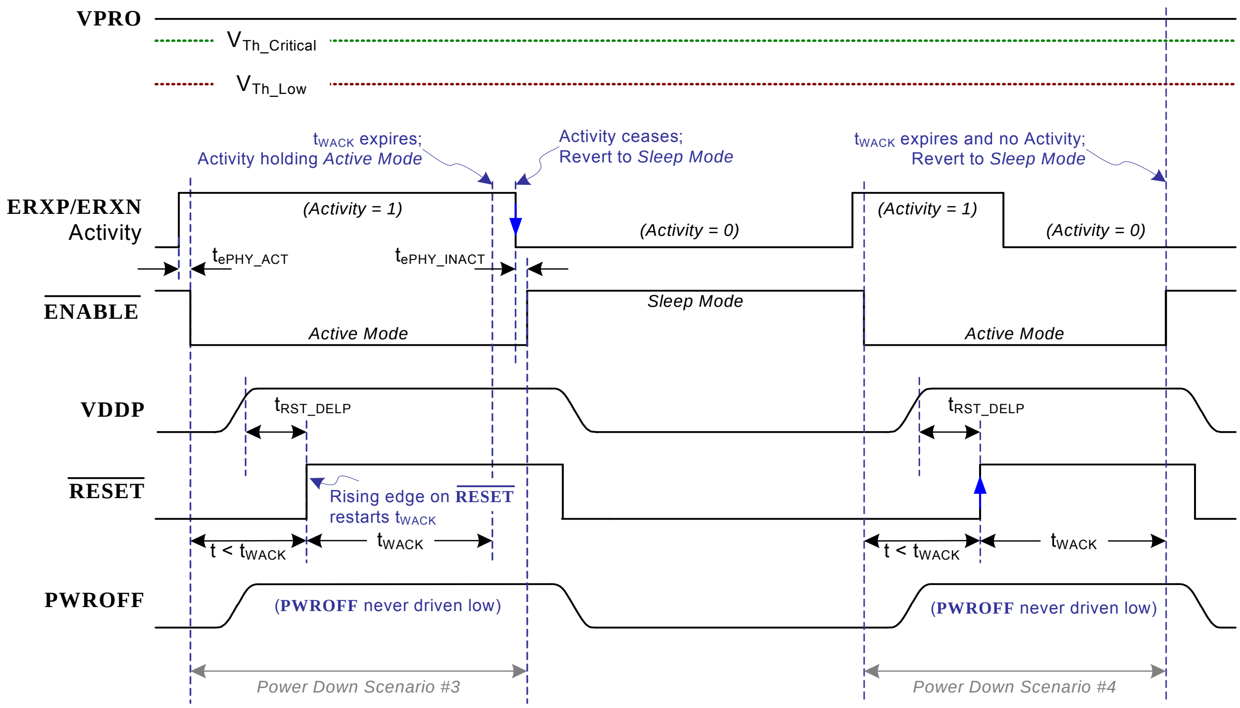


Figure 3-4: Power Down Scenarios 3 and 4

The first power cycle in Figure 3-5 depicts scenario 5 (listed in Table 3-1). After entering *Active Mode*, **LIN** activity ceases (**LIN** goes high), and the **PWROFF** signal is pulled low by the external device (INIC/EHC). At some point later, the **RESET** pin is externally pulled low, which causes the external device to release the **PWROFF** signal. The t_{RST_POFF} timer keeps the MPM85000 in *Active Mode* to allow the INIC/EHC time to recover after the reset. However, in this scenario, **RESET** is faulty (stuck low); therefore, when the t_{RST_POFF} timer expires, the MPM85000 reverts to *Sleep Mode*. The second power cycle depicts scenario 6, where the **VDDP** supply is faulty. In this scenario, **VDDP** collapsing causes the MPM85000 reset generator to drive **RESET** low. Since **VDDP** is invalid, **PWROFF** is ignored, and the MPM85000 reverts to *Sleep Mode* after t_{RST_POFF}.

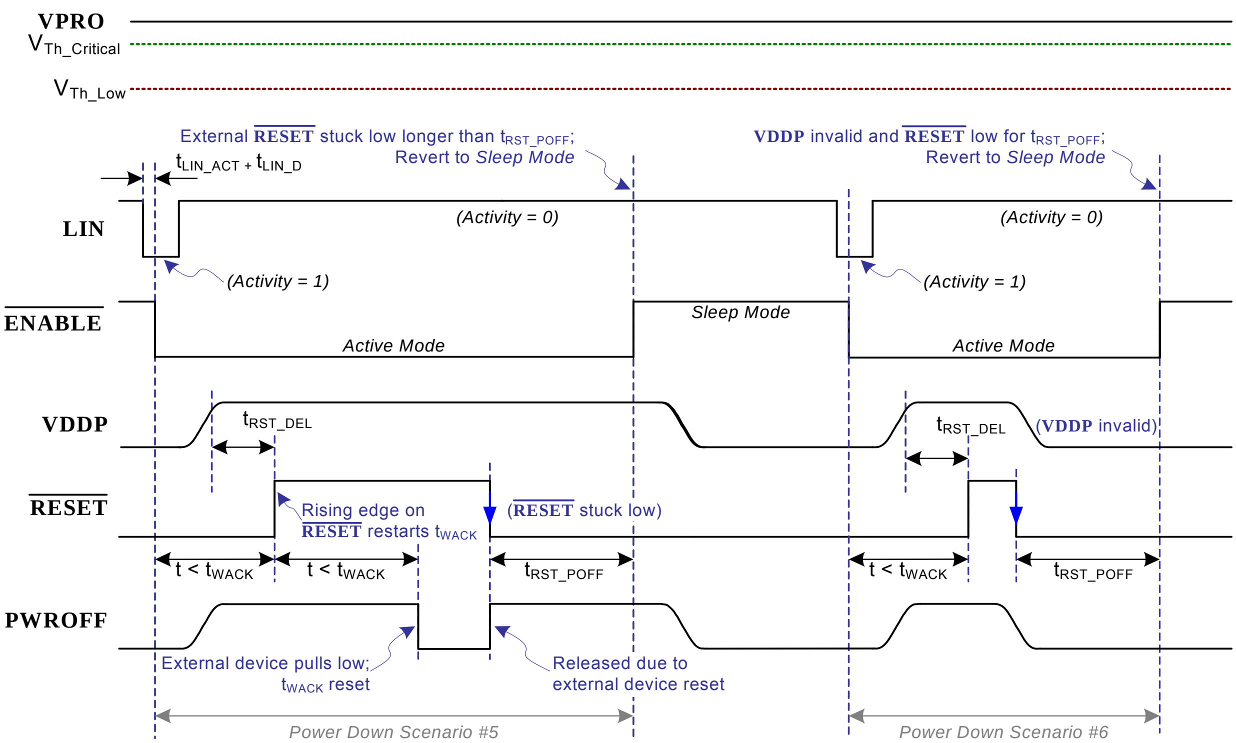


Figure 3-5: Power Down Scenarios 5 and 6

4 Voltage Monitors

The MPM85000 voltage monitors provide high-impedance internal attenuators that are connected to the **VPRO** and **VBATT_F** pins. A large internal impedance is required to minimize current in *Sleep Mode*. Since the attenuator ladders are internal, conformal coating (which is required to maintain accuracy when using a discrete solution) is not needed. Voltages on **VPRO** and **VBATT_F** are divided down to a level that can be compared to programmed voltage thresholds.

4.1 VPRO Pin

The **VPRO** pin should be connected to the protected power supply, after the load dump protection circuitry (see Chapter 13 for typical application connection diagrams). This pin voltage is divided down to obtain the various voltage levels defined in the *MOST Specification [2]*. When in *Sleep Mode*, these regions are used to define the *Allowed Wakeup Range* ($V_{WakeupRange}$), which prevents the MPM85000 from transitioning to *Active Mode* when the power supply voltage is irregular. The $V_{WakeupRange}$ voltage range is programmable through the **WAKEHI** configuration pin as well as the **CR.WAKESV** and **CR.$\overline{\text{WAKECV}}$** register bits.

The following four distinct *VPRO Power Regions* are defined:

- *Normal Power Region* (U_{Normal})
- *Low Power Region* (U_{Low})
- *Critical Power Region* ($U_{Critical}$)
- *Super Power Region* (U_{Super})

Programmed thresholds set the boundaries of the *VPRO Power Regions*, which are shown in Figure 4-1. When in *Active Mode*, these regions are used to alert the INIC/EHC to abnormal power conditions.

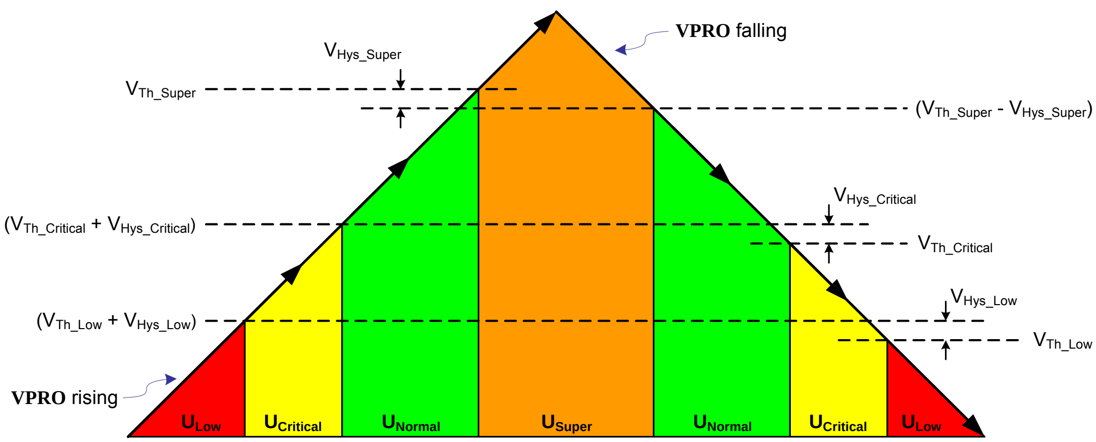


Figure 4-1: VPRO Power Regions

Table 4-1 defines the *Allowed Wakeup Range*, $V_{WakeupRange}$, of the MPM85000.

CR.$\overline{\text{WAKECV}}$*	CR.WAKESV	VPRO Lower Bound	VPRO Upper Bound	Allowed Wakeup Range ($V_{WakeupRange}$)
0	0	**VPRO** ≥ V_{Th_Low}	**VPRO** < V_{Th_Super}	$U_{Critical}$, U_{Normal}
0	1	**VPRO** ≥ V_{Th_Low}	none	$U_{Critical}$, U_{Normal}, U_{Super}
1	0	**VPRO** ≥ $V_{Th\_Critical}$	**VPRO** < V_{Th_Super}	U_{Normal}
1	1	**VPRO** ≥ $V_{Th\_Critical}$	none	U_{Normal}, U_{Super}

* The state of the **WAKEHI** pin at initial power-up sets the default value of the **CR.$\overline{\text{WAKECV}}$** bit.

Table 4-1: Allowed Wakeup Range

Voltage thresholds for **VPRO** (V_{Th_Low}, $V_{Th\_Critical}$, V_{Th_Super}) are set in the *VPRO Comparator Threshold Register* (VCT), which is accessible via the Control Port. Refer to Section 10.2.5 for details on VCT. A fixed hysteresis (V_{Hys_Low}, $V_{HYS\_Critical}$, and V_{Hys_Super}) exists for each threshold.

When the MPM85000 is in *Active Mode*, transitions between *VPRO Power Regions* result in:

- the appropriate bit in the *Status Register* (SR) is changed to indicate the current power region,
- the **PS1** and **PS0** pins are driven to reflect the current power region (to alert INIC/EHC), and
- the **IR.iVOLT** bit is set and, assuming **MR.mVOLT** is not set, the $\overline{\textbf{INT}}$ pin is asserted to alert the EHC.

The U_{Super} region notification is generally used to secure ECU application hardware that is sensitive to high voltage, such as power amplifiers or disk drives.

The $U_{Critical}$ region notification is generally used to secure hardware that cannot operate with at low voltage levels and to secure audio connections in a MOST Network application. Additionally, persistent parameters can be saved at this point before the supply drops further.

The U_{Low} region notification generally indicates the power supply is collapsing and the local device should take the necessary action in anticipation of full loss of power. Bulk capacitance in the load dump circuitry usually prevents small transients into U_{Low} from disrupting the ECU. For MOST Network devices, the *MOST Specification [2]* indicates that the ECU should stop network communications and transition to *Sleep Mode* when the supply drops into the U_{Low} region. The MPM85000 facilitates this feature when **VPRO** drops below V_{Th_Low} by ignoring qualified activity on input signals and overriding the **PWROFF** pin delay timer to allow quick transition into *Sleep Mode* once the external device releases **PWROFF**.

Automotive ECU power supply inputs typically include load dump and filtering circuits which protect the ECU from voltage transients and provide reserve power for short periods of voltage dropout. These components also provide EMI immunity and reduce EMI emissions. The hardware configuration needed is application specific; however, Figure 4-2 illustrates a basic circuit for discussion purposes. The polarized capacitors (C2 and C4) and transient diode (D2) should be specified for low leakage since they contribute to *Sleep Mode* current. The load dump circuitry also causes a voltage drop, $V_{LoadDump}$, between the ECU box edge and the internal protected power (ProConP) net, where the MPM85000 **VPRO** pin monitors the supply voltage.

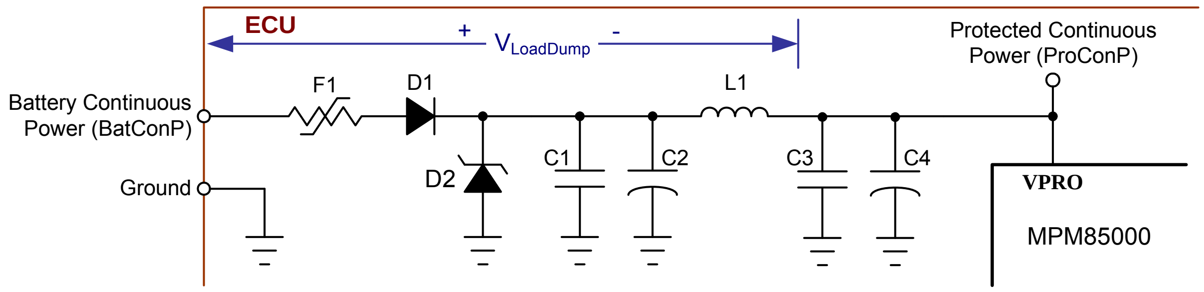


Figure 4-2: Load Dump Voltage Drop

This voltage drop must be taken into account when selecting the **VPRO** comparator thresholds, since the MPM85000 measures the voltage levels at the protected power (ProConP) net, but OEMs specify ECU voltage levels from the outside of the ECU (BatConP).

4.2 STP and VBATT_F Pin

In legacy MOST Network systems (see the *MOST Specification Version 2.5 [6]* for more information) a *Switch-To-Power Detector* is available as a method for initiating ring-break diagnosis (RBD), which can identify and localize a break in a MOST Network for easy repair. A *Switch-To-Power* (STP) event does not occur during normal ECU operation, but rather in a vehicle repair shop or assembly line. The vast majority of newer systems use the *Electrical Control Line Specification [4]* since it provides additional diagnostic capabilities. STP is disabled by default on the MPM85000; the **CR.NOSTP** bit must be cleared to support STP. In addition, the power supply pins must be configured as shown in Section 13.5.

> When STP event detection is not required, the **VBATT_F** pin should be tied directly to ground to reduce power consumption in *Sleep Mode*.

The disruption of battery power for at least the t_{STP} time is referred to as a *Switch-To-Power* (STP) event.

The MPM85000 detects an STP wakeup event when **VBATT_F** drops below the V_{STP_LO} threshold for at least t_{STP} then rises above the V_{STP_HI} threshold. Once an STP event occurs, protected power (**VPRO**) must also be within the $V_{WakeupRange}$ voltage range to wakeup from *Sleep Mode*.

When an STP event is detected, **PS1** and **PS0** are set appropriately (as described in Chapter 9, *Power Management Port*), the **IR.iPOR** bit is set, and **$\overline{\text{INT}}$** is driven low. When set, the **IR.iPOR** register bit indicates either initial power applied to the MPM85000 or that an STP event occurred. In either case, the response (initiating RBD) is the same for MOST INIC devices that are configured to support STP. Table 4-2 illustrates various conditions on **VBATT_F** and how the STP detection logic handles the condition, assuming the **CR.NOSTP** register bit is clear.

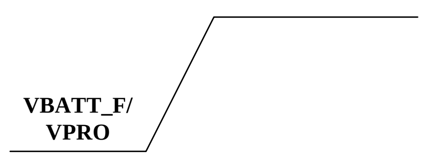
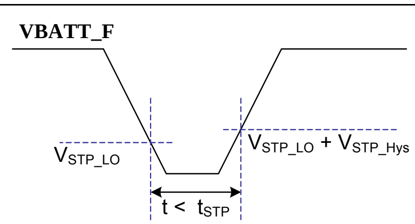
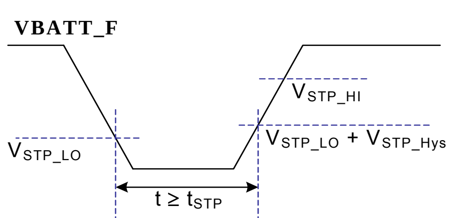
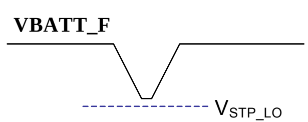
Case	VBATT_F	Condition	STP Event
1		Initial power-up condition: When STP is enabled, this condition is also considered an STP event. In this case, the **VPRO** voltage is compared against $V_{WakeupRange}$.	Yes
2		Engine start condition: In this case, **VBATT_F** drops below V_{STP_LO} for less than t_{STP} before rising above (V_{STP_LO} + V_{STP_Hys}). If the device is in *Sleep Mode*, it does not wake up.	No
3		Valid STP pulse detection: In this case, **VBATT_F** drops below V_{STP_LO} for at least t_{STP} before rising above (V_{STP_LO} + V_{STP_Hys}). The actual STP event does not occur until **VBATT_F** exceeds the V_{STP_HI} threshold. Then the **VPRO** voltage must be within the $V_{WakeupRange}$ voltage range to cause a wakeup event.	Yes
4		Normal operating condition: In this case, **VBATT_F** remains above V_{STP_LO} so the t_{STP} timer is never started. If the device is in *Sleep Mode*, it does not wake up.	No

Table 4-2: STP Event Detection

Figure 4-3 illustrates STP activity and interaction with the application. Note that **WAKEHI** = **VDDU**, thereby prohibiting the MPM85000 from waking up when **VPRO** is in the $U_{Critical}$ region.

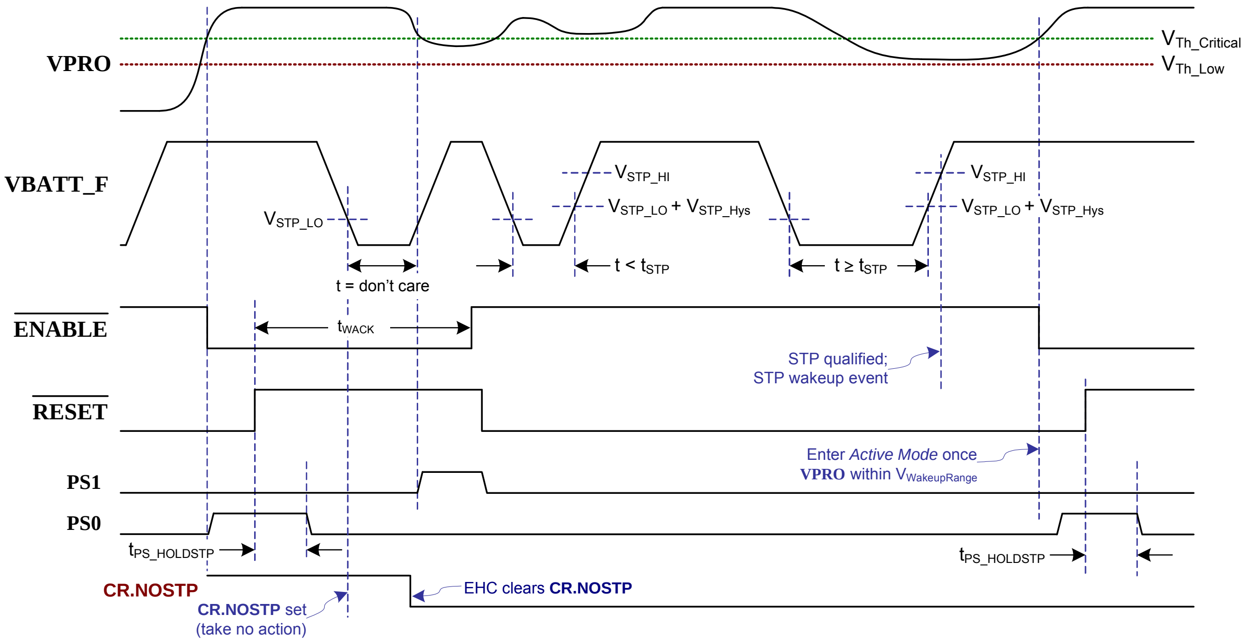


Figure 4-3: STP Activity and Interaction

5 Activity Detectors

The MPM85000 contains four inputs with activity detection and qualification circuits that are capable of waking the MPM85000 from *Sleep Mode*, as well as keeping the MPM85000 in *Active Mode*. The four inputs that support activity detection are:

- **LIN** - Supports standard LIN bus *[3]* connections and is also MOST ECL *[4]* compliant. When used, activity on this pin wakes up the MPM85000 from *Sleep Mode* whenever a qualified LIN or ECL wakeup pulse is detected.
- **STATUS** - In MOST optical systems, the **STATUS** pin is connected to the OEC/FOR activity indicator output, which is driven active (low) whenever optical activity is present. This functionality allows MPM85000 wakeup events based on optical MOST Network activity. In non-MOST or non-optical MOST systems, **STATUS** can be used as a general purpose local wakeup event.
- **ERXP**/**ERXN** - In MOST50 electrical systems, these pins are connected to the electrical network receive circuitry to provide network activity wakeup event signalling. This is equivalent to the functionality that the **STATUS** pin provides for optical MOST systems. For other applications (e.g. non-MOST or optical MOST systems) these pins are typically unused and should be tied directly to ground.
- **ON_SW** - Provides local wakeup event support, such as a momentary push-button switch. Other uses are as an on-board wakeup signal for a telematics system which needs to wakeup the MPM85000 from *Sleep Mode* when a call comes in, or a door open switch which needs to wakeup the ECU to respond to the event.

In addition to monitoring activity on these pins, all the activity detection circuits implement qualification procedures to validate both activity and inactivity over a set period of time. This provides robust fault tolerance and glitch protection by effectively ignoring spurious events on these input pins.

5.1 LIN Pin Activity Detection

In addition to operating as a standard *Local Interconnect Network (LIN) Transceiver [3]* (refer to Chapter 6, *LIN Transceiver*), the MPM85000 **LIN** pin is also compliant to the *MOST Electrical Control Line (ECL) Specification [4]*. In simple, low-cost implementations, the **LIN** pin can serve as the only source of non-local wakeup events. In advanced systems, LIN or ECL communication can be specified as a redundant wakeup event mechanism to MOST Network activity, as it provides simultaneous wakeup to all ECUs and can also provide a communications bus for diagnostics. When used for MOST ECL signalling, software register bits can replace the hardware **TXD**/**RXD** pins, while the **LIN** pin activity detector is used to generate interrupts to the EHC whenever the **LIN** pin changes state (eliminates the need for software polling). If the **LIN** pin is not needed for a particular design, it can be left floating since it contains an internal pull-up resistor to **VPRO**.

When a falling edge is detected on **LIN**, the MPM85000 turns on an internal timer to qualify the activity. If **LIN** remains low for t_{LIN_ACT}, then the activity is considered valid, the **IR.iLIN** bit in the *Interrupt Register* (IR) is set, and the $\overline{\textbf{INT}}$ pin is driven low (assumes the **MR.mLIN** mask bit is clear). If the MPM85000 is in *Sleep Mode* when the **LIN** activity is qualified as valid, and if the **VPRO** power supply is valid (within the $V_{WakeupRange}$ voltage range), then the MPM85000 transitions to *Active Mode*. If the **LIN** pin causes the MPM85000 to exit *Sleep Mode*, then the **IWE.wLIN** bit in the *Initial Wakeup Event Register* (IWE) is set. This register indicates the reason the MPM85000 entered *Active Mode*; refer to Section 10.2.12 for more information.

Once in *Active Mode*, both edges on **LIN** are qualified for noise rejection. Therefore, once **LIN** activity is qualified (logic low level, also defined as dominant) with t_{LIN_ACT}, then **LIN** inactivity (logic high level, also defined as recessive) is qualified with the t_{LIN_INACT} timer. The **LSR.LIN** bit in the *Line Status Register* (LSR) indicates the current qualified state of the **LIN** pin. The **LSR.LIN** bit is set when **LIN** is qualified low or active, and cleared when **LIN** is qualified high or inactive. Each transition of the **LSR.LIN** bit (each qualified edge of the **LIN** pin) causes the **IR.iLIN** bit in the *Interrupt Register* (IR) to be set, which in turn causes the $\overline{\textbf{INT}}$ pin to be driven low (assumes **MR.mLIN** clear). The IR bits are cleared (interrupt cleared) when the register is read. If the **LIN** pin is used for standard high-speed LIN communication (EHC using the **RXD/TXD** pins), then the **MR.mLIN** mask bit should be set so LIN communication does not cause excessive EHC interrupts.

Figure 5-1 depicts the *Active Mode* **LIN** pin detection logic, without the fail-safe features (see Figure 6-1 on page 33 for the complete **LIN** pin logic diagram). The **LC.RXD** bit is a software version of the **RXD** pin that differs from **LSR.LIN** in polarity. Also, the **LC.RXD** register bit represents the actual pin value (i.e. it is not qualified with timers). The **LC.TXD** bit is a software version of the **TXD** pin.

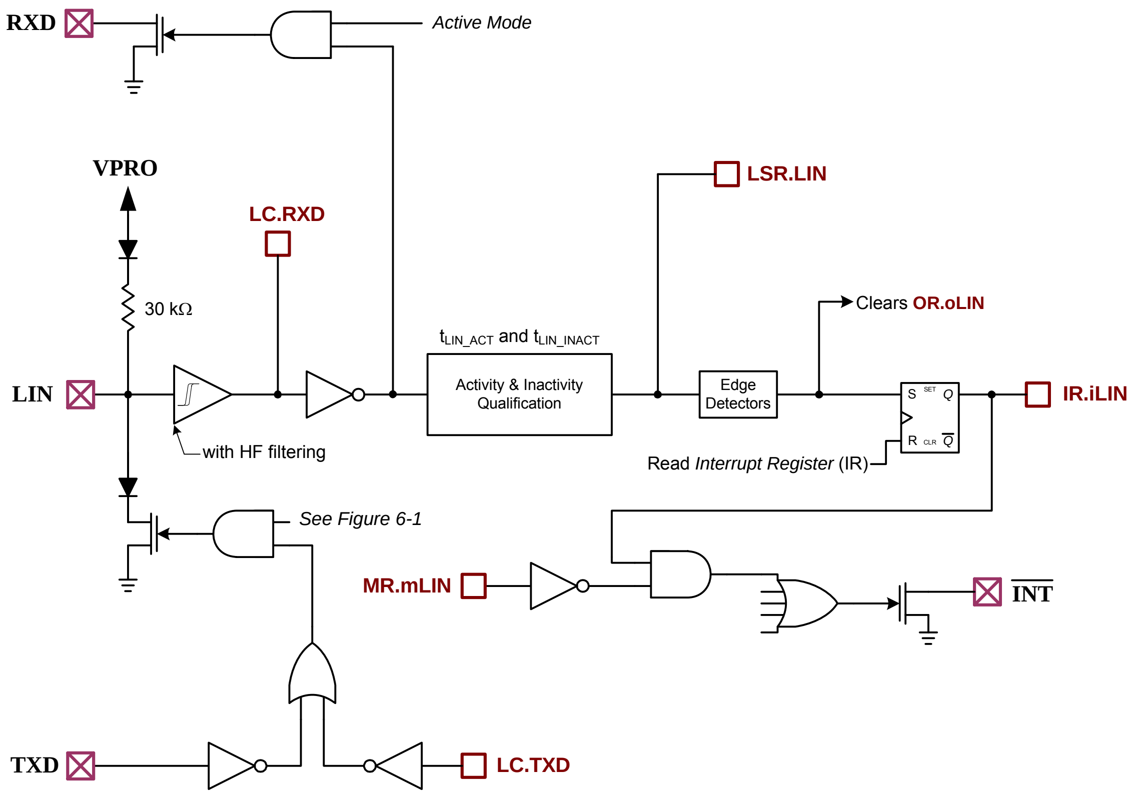


Figure 5-1: LIN Pin Detector Logic

If the **LIN** pin override bit (**OR.oLIN** in the *Override Register* (OR)) was previously set to ignore a stuck **LIN** pin, then any transition from qualified activity to qualified inactivity, or vice versa (i.e. any change of **LSR.LIN**), clears the **OR.oLIN** bit. In a normal operating environment, qualified **LIN** activity (**LIN** pin low, or dominant) keeps the MPM85000 in *Active Mode*. If the EHC determines that the **LIN** pin is stuck low for any reason (e.g. short to ground), then the EHC can set **OR.oLIN** which allows the MPM85000 to revert to *Sleep Mode* when the EHC chooses. If, while in *Sleep Mode*, the **LIN** pin gets unstuck, then any transitions automatically clear **OR.oLIN** thereby allowing the MPM85000 to wakeup again from **LIN** activity. Figure 5-2 below illustrates the **LIN** activity qualification process.

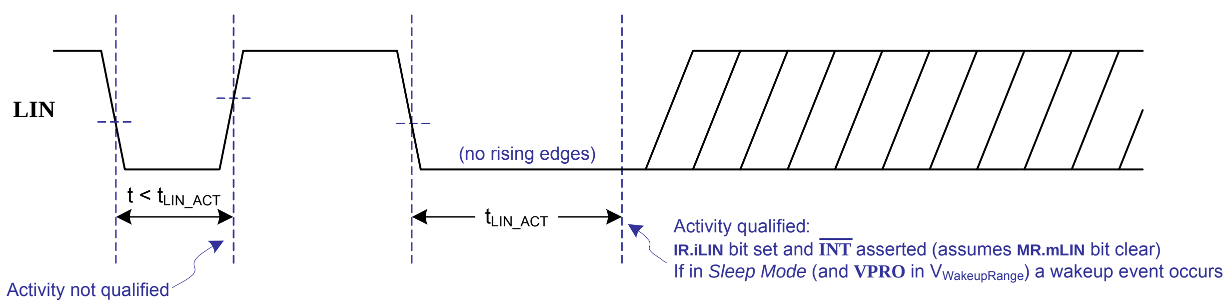


Figure 5-2: LIN Activity Qualification

5.2 STATUS Pin Activity Detection

In MOST optical systems, the MPM85000 **STATUS** pin is connected to the OEC/FOR network activity indicator output, which is driven active (low) when optical activity is present. The OEC/FOR is powered from the MPM85000 MicroPower regulator (**VDDU** pin) continuous power supply and typically implements its own low-power (sleep mode) mode of operation to meet OEM power requirements. The OEC/FOR wakes up from its sleep mode when optical activity exists and drives its activity indicator output pin active (logic low level). This, in turn, wakes up the MPM85000 from *Sleep Mode* (provided **VPRO** is within the $V_{WakeupRange}$ voltage range). In non-MOST or non-optical MOST systems, the **STATUS** input can be used to detect a general purpose local wakeup event (see the *MOST INIC Hardware Concepts Technical Bulletin [1]* for examples of local wakeup events). If the **STATUS** input pin is not needed in a particular design, it should be tied to **VDDU**.

When a falling edge is detected on **STATUS**, the MPM85000 turns on an internal timer to qualify the activity. If **STATUS** remains low for t_{STAT_ACT}, then the activity is considered valid, the **IR.iSTATUS** bit in the *Interrupt Register* (IR) is set, and the $\overline{\textbf{INT}}$ pin is driven low (assumes the **MR.mSTATUS** mask bit is clear). If the MPM85000 is in *Sleep Mode* when the **STATUS** activity is qualified as valid, and if the **VPRO** power supply is valid (within $V_{WakeupRange}$), then the MPM85000 transitions to *Active Mode*. If the **STATUS** pin causes the MPM85000 to exit *Sleep Mode*, then the **IWE.wSTATUS** bit in the *Initial Wakeup Event Register* (IWE) is set.

Once in *Active Mode*, both edges on **STATUS** are qualified for noise rejection. Therefore, once **STATUS** activity is qualified (logic low level) with t_{STAT_ACT}, then **STATUS** inactivity (logic high level) is qualified with the t_{STAT_INACT} timer. The **LSR.STATUS** bit in the *Line Status Register* (LSR) indicates the current qualified state of the **STATUS** pin. The **LSR.STATUS** bit is set when **STATUS** is qualified low or active, and cleared when **STATUS** is qualified high or inactive. Each transition of the **LSR.STATUS** bit (each qualified edge on the **STATUS** pin) causes the **IR.iSTATUS** bit to be set, which in turn causes the $\overline{\textbf{INT}}$ pin to be driven low (assumes **MR.mSTATUS** clear). The IR bits are cleared (interrupt cleared) when the register is read. Figure 5-3 depicts the **STATUS** pin logic.

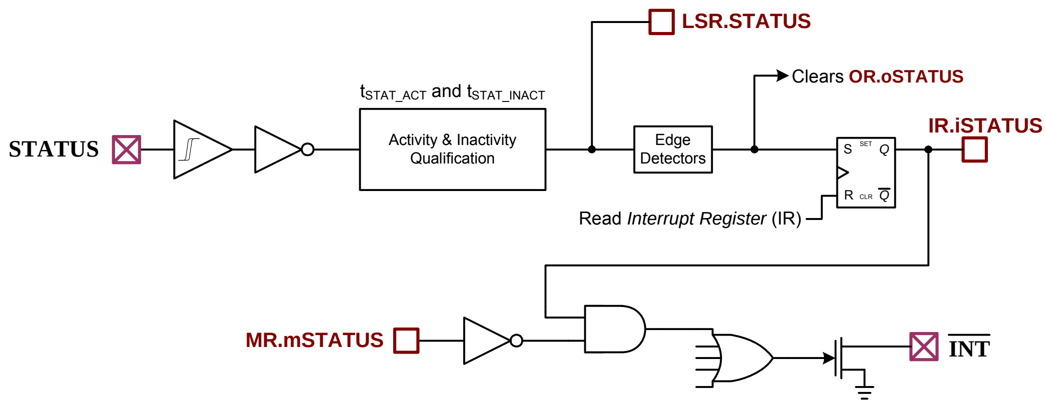


Figure 5-3: STATUS Pin Detector Logic

If the **STATUS** pin override bit (**OR.oSTATUS** bit in the *Override Register* (OR)) was previously set to ignore a stuck **STATUS** pin, then any transition from qualified activity to qualified inactivity, or vice versa (i.e. any change of **LSR.STATUS**), clears the **OR.oSTATUS** bit. In a normal operating environment, qualified **STATUS** activity (**STATUS** pin low) keeps the MPM85000 in *Active Mode*. If the EHC determines that the **STATUS** pin is stuck low for any reason, then the EHC can set **OR.oSTATUS** which allows the MPM85000 to revert to *Sleep Mode* when the EHC chooses. If, while in *Sleep Mode*, the **STATUS** pin gets unstuck, then any transitions automatically clear **OR.oSTATUS** thereby allowing the MPM85000 to wakeup again from **STATUS** activity.

5.3 ePHY Activity Detection

In MOST50 electrical systems, the physical layer front-end circuitry is passive and does not include activity detection logic (unlike MOST optical systems, in which the FOR/OEC checks for network activity). For these electrical network systems, the MPM85000 contains an internal ePHY network activity detector. The MPM85000 **ERXP/ERXN** pins should connect to the network at MOST50 specification point four (also known as SP4E; see the *MOST Specification of Electrical Physical Layer [7]* for more information) to allow wakeup events based on ePHY network activity. For systems that do not require electrical network activity detection, the **ERXP/ERXN** pins should both be tied directly to ground. Additionally, the ePHY activity detector should be powered down (by setting the **CR.PDEPHY** bit in the *Configuration Register* (CR)) to minimize *Sleep Mode* current.

When activity is detected on the **ERXP/ERXN** pins the internal ePHY activity detector evaluates the signal for both amplitude and transitions. If the activity meets the requirements, the MPM85000 turns on an internal timer to qualify the activity over time. If the signal is continuously active for t_{ePHY_ACT}, then the activity is considered valid, the **IR.iEPHY** bit in the *Interrupt Register* (IR) is set, and the $\overline{\textbf{INT}}$ pin is driven low (assumes the **MR.mEPHY** mask bit is clear). In addition, **NOACT** pin is driven low for the duration of qualified ePHY activity and can be used by the EHC or other external circuitry, if desired. If the MPM85000 is in *Sleep Mode* when ePHY activity is qualified as valid, and if the **VPRO** power supply is valid (within the $V_{WakeupRange}$ voltage range), then the MPM85000 transitions to *Active Mode*. If ePHY activity causes the MPM85000 to exit *Sleep Mode*, then the **IWE.wEPHY** bit in the *Initial Wakeup Event Register* (IWE) is set.

Once in *Active Mode*, both ePHY activity and inactivity are qualified for noise rejection. Therefore, once ePHY activity is qualified for t_{ePHY_ACT}, then ePHY inactivity is qualified with the t_{ePHY_INACT} timer. The **LSR.EPHY** bit in the *Line Status Register* (LSR) indicates the current qualified state of the ePHY activity detector inputs (**ERXP/ERXN**), where **LSR.EPHY** set indicates that the ePHY signal is qualified as active, and **LSR.EPHY** clear indicates the ePHY signal is qualified as inactive. Each transition of the **LSR.EPHY** bit causes the **IR.iEPHY** bit to be set, which in turn causes the $\overline{\textbf{INT}}$ pin to be driven low (assumes **MR.mEPHY** clear). The IR bits are cleared (interrupt cleared) when the register is read. Figure 5-4 depicts the ePHY activity detector logic.

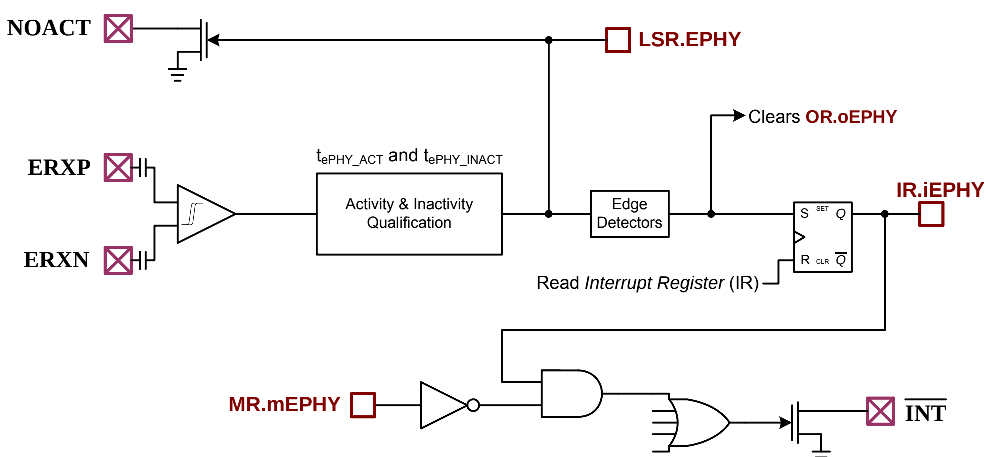


Figure 5-4: ePHY Detector Logic

If the ePHY detector override bit (**OR.oEPHY** in the *Override Register* (OR)) was previously set to ignore a stuck ePHY condition, then any transition from qualified activity to qualified inactivity, or vice versa (i.e. any change of **LSR.EPHY**), clears **OR.oEPHY.** In a normal operating environment, qualified ePHY activity keeps the MPM85000 in *Active Mode*. If the EHC determines that the ePHY activity detector should be ignored, then the EHC can set **OR.oEPHY** which allows the MPM85000 to revert to *Sleep Mode* when the EHC chooses. If, while in *Sleep Mode*, the ePHY detector changes state, the transitions automatically clear **OR.oEPHY** thereby allowing the MPM85000 to wakeup again from ePHY activity.

5.4 ON_SW Pin Activity Detection

In the majority of vehicle networks, a single ECU is responsible for waking the network under normal circumstances. When this ECU wakes up the other ECUs it does so via LIN/ECL or network activity, which are defined as network wakeup events. The ECU responsible for waking the rest of the network requires its own signal to wake it up from *Sleep Mode*. This signal is defined as a local wakeup event since it does not originate from the network. Refer to the *MOST INIC Hardware Concepts Technical Bulletin [1]* for more information on the concepts of local and network wakeup events. Additionally, some network architectures require more than one node to be capable of waking the network. These nodes also require some type of local event to wakeup from *Sleep Mode*.

The MPM85000 **ON_SW** pin provides a means of detecting and qualifying these local wakeup event signals. The local event could be a simple momentary push-button switch (input debouncing is handled by the MPM85000). An alternate local event could be a telematics unit indicating a call is coming in, for which the ECU must wakeup to respond to the call. Once the ECU is in *Active Mode*, the EHC can qualify the local event to determine whether the rest of the network should be started or not. If the **ON_SW** pin is not needed in a particular design, it can be left floating since it contains an internal pull-up resistor to **VDDU**.

When a falling edge is detected on **ON_SW**, the MPM85000 turns on an internal timer to qualify the activity. If **ON_SW** remains low for t_{ON_ACT}, then activity is considered valid, the **IR.iONSW** bit in the *Interrupt Register* (IR) is set, and the $\overline{\textbf{INT}}$ pin is driven low (assumes **MR.mONSW** mask bit is clear). If the MPM85000 is in *Sleep Mode* when the **ON_SW** activity is qualified as valid, and if the **VPRO** power supply is valid (within the $V_{WakeupRange}$ voltage range), then the MPM85000 transitions to *Active Mode*. If the **ON_SW** pin causes the MPM85000 to exit *Sleep Mode*, then the **IWE.wONSW** bit in the *Initial Wakeup Event Register* (IWE) is set.

Once in *Active Mode*, both edges of **ON_SW** are qualified for noise rejection. Therefore, once **ON_SW** activity is qualified (logic low level) with t_{ON_ACT}, then **ON_SW** inactivity (logic high level) is qualified with the t_{ON_INACT} timer. The **LSR.ONSW** bit in the *Line Status Register* (LSR) contains indicates the current qualified state of the **ON_SW** pin. The **LSR.ONSW** bit is set when **ON_SW** is qualified low or active, and clear when **ON_SW** is qualified high or inactive. Each transition of the **LSR.ONSW** bit (each qualified edge of the **ON_SW** pin) causes the **IR.iONSW** bit to be set, which in turn causes the $\overline{\textbf{INT}}$ pin to be driven low (assumes **MR.mONSW** clear). The IR bits are cleared (interrupt cleared) when the register is read. Figure 5-5 depicts the **ON_SW** pin logic.

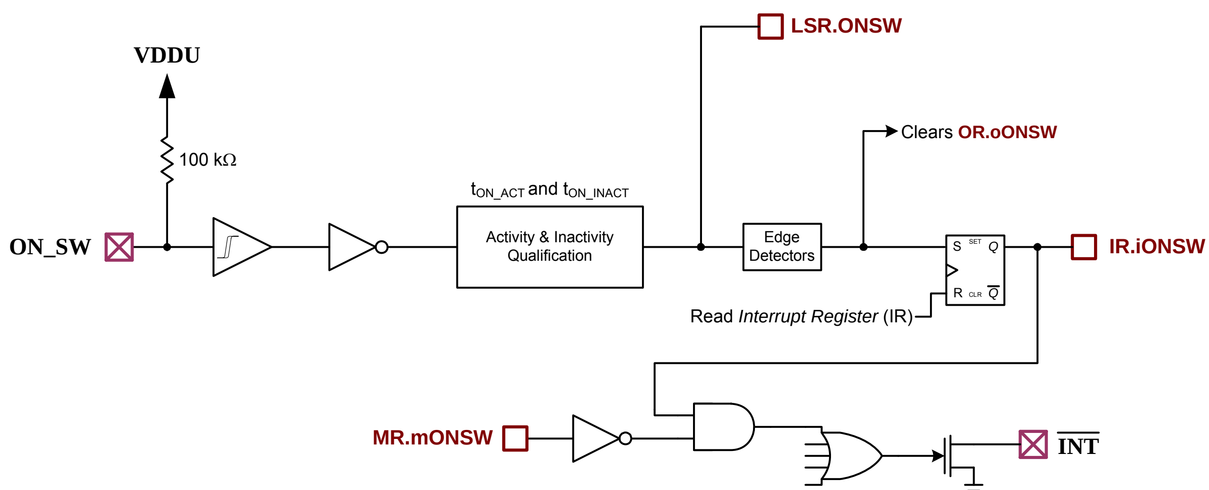


Figure 5-5: ON_SW Pin Detector Logic

If the **ON_SW** pin override bit (**OR.oONSW** in the *Override Register* (OR)) was previously set to ignore a stuck **ON_SW** pin, then any transition from qualified activity to qualified inactivity, or vice versa (i.e. any change of **LSR.ONSW**), clears **OR.oONSW**. In a normal operating environment, qualified **ON_SW** activity (**ON_SW** low) keeps the MPM85000 in *Active Mode*. If the EHC determines that the **ON_SW** pin is stuck low for any reason, then the EHC can set **OR.oONSW** which allows the MPM85000 to revert to *Sleep Mode* when the EHC chooses. If, while in *Sleep Mode*, the **ON_SW** pin gets unstuck, then any transitions automatically clear **OR.oONSW** thereby allowing the MPM85000 to wakeup again from **ON_SW** activity.

Figure 5-6 illustrates the **ON_SW** qualification process. Since the MPM85000 qualifies all wakeup events with a valid power supply voltage, this figure assumes **VPRO** is in the $V_{WakeupRange}$ voltage range.

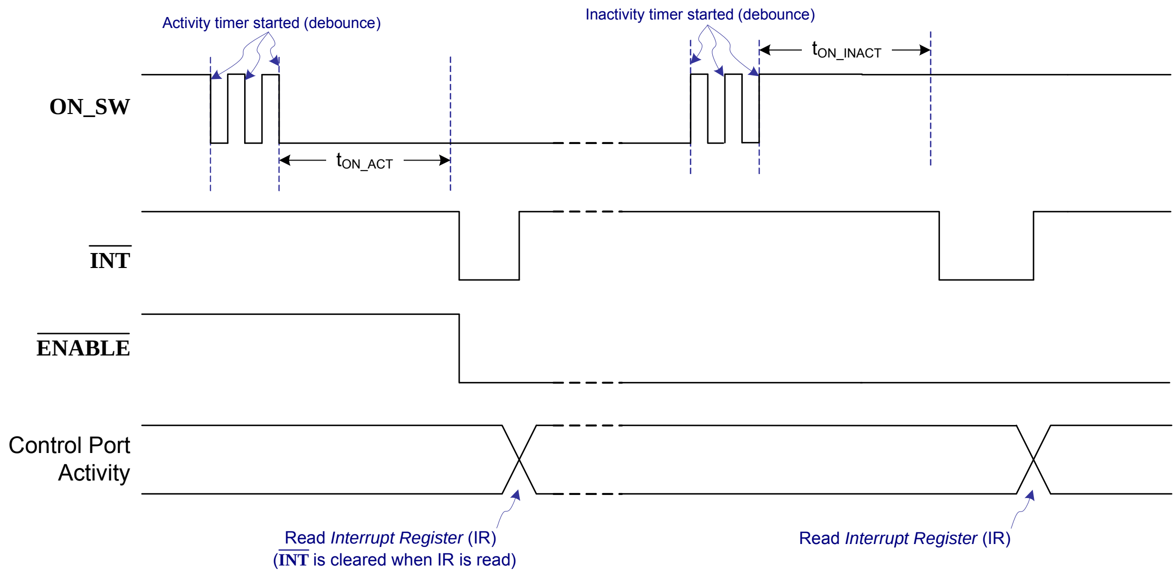


Figure 5-6: ON_SW Qualification Timing

6 LIN Transceiver

The MPM85000 contains an integrated LIN transceiver, powered from the **VPRO** pin, which supports standard *Local Interconnect Network* (LIN) *[3]* communication. Additionally, the LIN transceiver contains custom features which make it compliant to the *MOST Electrical Control Line Specification [4]*. The LIN transceiver interface consists of the **LIN**, **TXD** and **RXD** pins. When the LIN transceiver is operational (only when the MPM85000 is in *Active Mode*), bidirectional data is exchanged on the **LIN** pin. The **LIN** pin logic states are the car battery supply voltage and ground. Battery voltage is the recessive state (logic 0; idle condition), and ground is the dominant state (logic 1; driven/active condition).

The bidirectional data on **LIN** is level-shifted (to a 3.3 V logic level) and split into the unidirectional **RXD** and **TXD** signals. The **RXD** pin always outputs the **LIN** pin logical state, and is typically connected to an EHC's UART/LIN receiver pin. Likewise, the EHC's UART/LIN transmitter pin is typically connected to the **TXD** pin. When the **TXD** pin is high, the **LIN** pin is in the recessive state (i.e. not driven, high-impedance). Conversely, when **TXD** is low, the **LIN** pin is in the dominant state (i.e. driven low).

Both the **RXD** and **TXD** pins should have pull-up resistors to keep the pins in an idle state when not driven. If the MPM85000 is in *Sleep Mode*, a logic low level on the **LIN** pin can trigger a transition to *Active Mode*. This low level is glitch-protected and must be continuously present for at least t_{LIN_ACT} for the MPM85000 to exit *Sleep Mode*. If the LIN transceiver causes the MPM85000 to exit *Sleep Mode*, then the **IWE.wLIN** bit in the *Initial Wakeup Event Register* (IWE) is set. This register indicates the reason the MPM85000 entered *Active Mode*; refer to Section 10.2.12 for more information.

The *LIN Control Register* (LC) provides control and status information on the LIN transceiver. When using ECL communication, and also when communicating on the LIN bus at lower speeds, the LC bits can be used in lieu of the **RXD** and **TXD** hardware pins, thereby freeing EHC pins for other uses. The **LC.RXD** bit tracks the **LIN** pin logic levels and functions identically to the **RXD** pin. The **LC.TXD** bit can drive the **LIN** pin low, and is logically or'ed with the **TXD** pin. Since the MPM85000 contains edge detectors on all activity input pins, interrupts can be generated whenever the **LIN** pin changes state; thereby eliminating the need for polling by the EHC. For detailed LC bit descriptions, see Section 10.2.6.

The LIN transmitter supports a configurable slew rate using the **LC.SLEW[1:0]** register bits. Depending on the application, the slew rate can be changed to provide the most appropriate trade-off between data rate and EMI. Refer to Section 10.2.6 for more information on the available slew rate control options.

An added MPM85000 fail-safe feature included in the LIN transceiver is the ability to handle the case where the **LIN** pin is stuck low. The MPM85000 includes an override feature on all activity inputs. For the LIN transceiver, if the EHC determines that the **LIN** pin is stuck low, it can set the **OR.oLIN** bit in the *Override Register* (OR), which allows the MPM85000 to revert to *Sleep Mode* even though **LIN** is in the dominant state. If, while in *Sleep Mode*, the **LIN** pin gets unstuck, the **OR.oLIN** bit is automatically cleared, thereby allowing the MPM85000 to wakeup again from **LIN** activity.

Figure 6-1 shows a simplified internal logic diagram of the **LIN** transceiver. When the MPM85000 is in *Active Mode*, the **VPRO** pull-up current (i.e. current when the **LIN** pin is driven low, or dominant) is based on the R_{SLAVE} resistor. During *Sleep Mode*, the R_{SLAVE} increases thereby reducing the pull-up current during the dominant state.

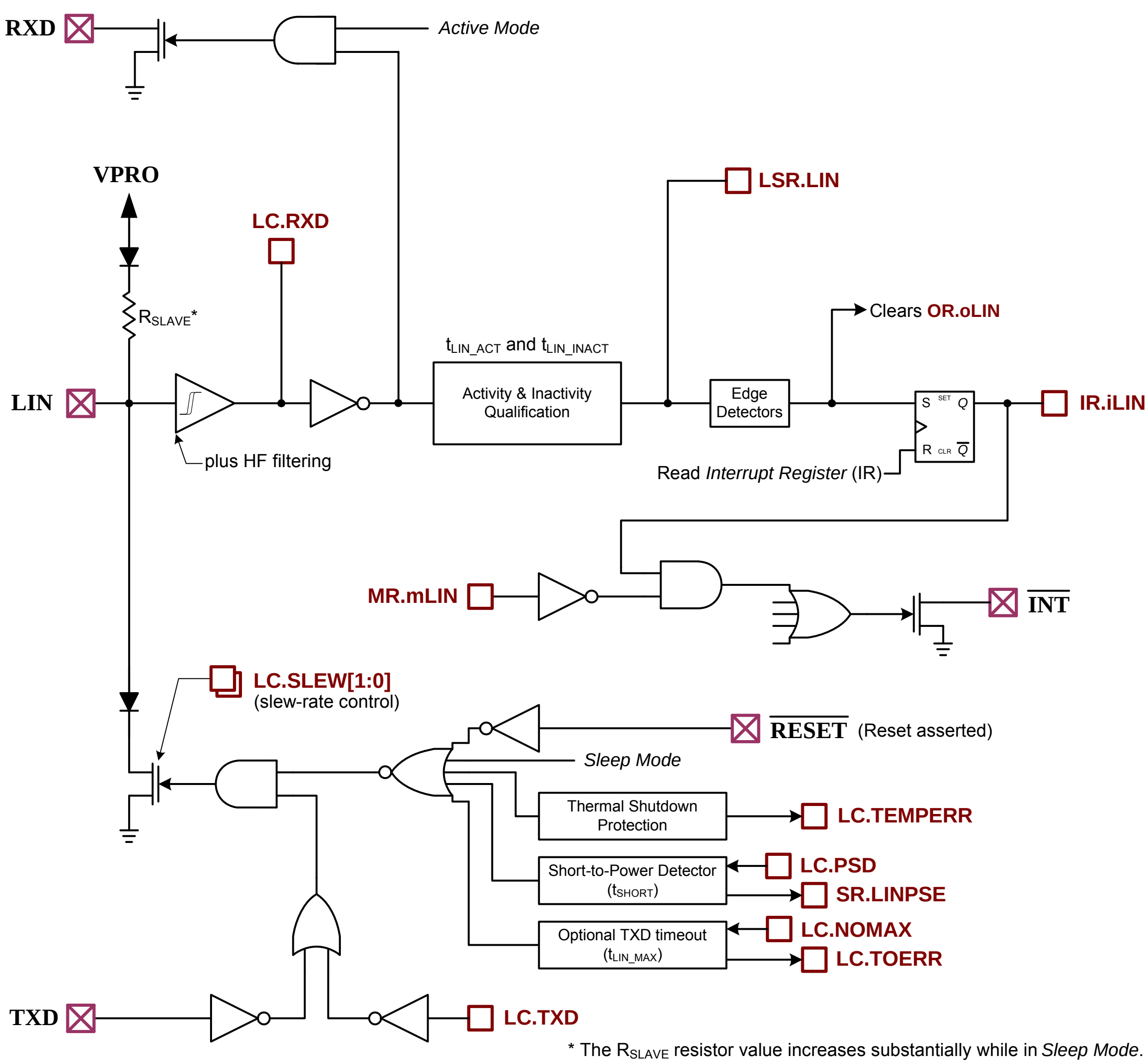


Figure 6-1: LIN Pin Logic Diagram

When in *Sleep Mode*, the **RXD** pin is high-impedance and the LIN driver is disabled. For added robustness while in *Active Mode*, any of the following conditions disable the LIN driver:

- **LIN** pin short-to-power fault condition (see Section 6.1),
- **TXD** pin (and equivalent **LC.TXD** register bit) timeout condition (see Section 6.2),
- LIN driver thermal shutdown condition (see Section 6.3), or
- **RESET** pin asserted (see Chapter 7, *Reset Generator and VDDP*).

Refer to Section 5.1 for more information on **LIN** pin activity detection and qualification.

Figure 6-2 shows the LIN transceiver waking the MPM85000 from *Sleep Mode*. Since the MPM85000 qualifies all wakeup events with a valid power supply voltage, this figure assumes **VPRO** is within the $V_{WakeupRange}$ voltage range.

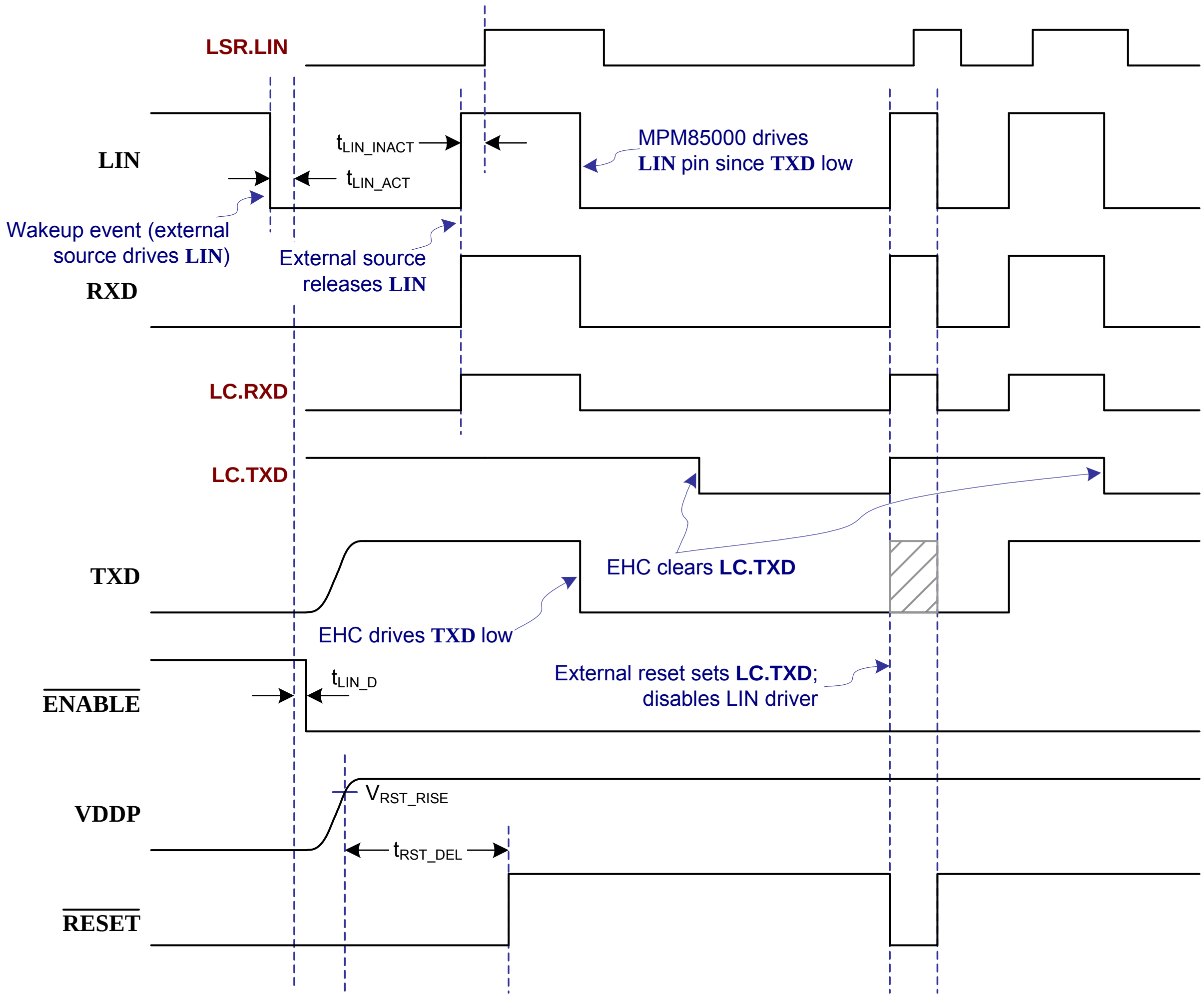


Figure 6-2: LIN Transceiver Wakeup Event

6.1 Short-To-Power Detector

Under the error condition where the **LIN** pin is shorted to the battery supply, the MPM85000 LIN driver will not be able to pull the **LIN** pin to ground. The MPM85000 includes three methods to protect the driver in this scenario:

- The LIN driver is current limited (I_{BUS_LIM}),
- The MPM85000 includes thermal shutdown protection (see Section 6.3), and
- The LIN transceiver includes a short-to-power detector which detects the LIN driver trying to drive low, while the **LIN** pin stuck high for an extended period of time.

When using the LIN transceiver for LIN bus communication, the first two scenarios listed above protect the LIN driver. The third scenario is applicable when the LIN transceiver is used for MOST ECL communication and is described in this section.

To support stand-alone operation, the short-to-power detection logic only applies to the **LC.TXD** register bit by default; however, setting the **LC.PSD** bit includes the **TXD** hardware pin during short-to-power fault detection.

When the MPM85000 tries to drive **LIN** low (due to **LC.TXD** being cleared, or by the EHC driving **TXD** low while **LC.PSD** is set) and the **LIN** pin stays high for longer than t_{SHORT}, the detection circuitry disables the LIN driver, sets the **SR.LINPSE** bit (see Section 10.2.2), and sets the **LC.TXD** bit (recessive state). When this occurs, an interrupt is generated ($\overline{\textbf{INT}}$ asserted low) to alert the EHC to the error condition. The EHC can clear the interrupt condition by reading the *Status Register* (SR); however, to re-enable the LIN driver and to be able to clear the **LC.TXD** bit, the EHC must first clear the **SR.LINPSE** bit. An example of the short-to-power detection functionality is shown in Figure 6-3.

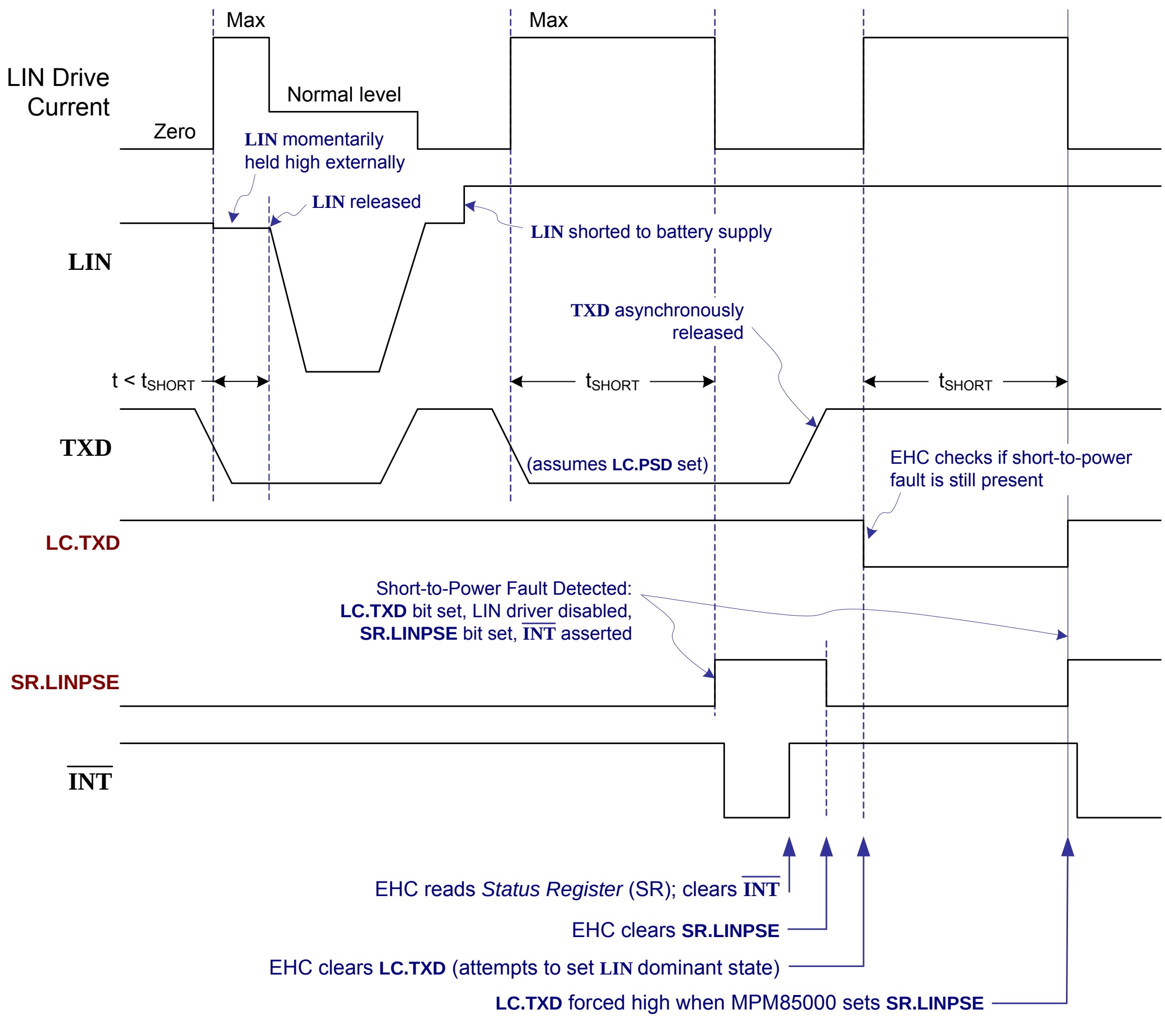


Figure 6-3: LIN Short-To-Power Example

6.2 Optional Timeout Condition

In the fault condition where the EHC either leaves the **TXD** pin stuck low, or it has cleared the **LC.TXD** bit and then never sets it again (to indicate the recessive state), the **LIN** pin would be stuck low and no other ECUs would be able to communicate on the LIN bus. The MPM85000 includes a fail-safe transmitter time-out that disables the LIN driver thereby releasing the **LIN** pin under this fault condition. Releasing the LIN bus allows LIN or ECL communication between the other connected ECUs. If the MPM85000 drives **LIN** low for longer than t_{LIN_MAX} (as a result of either the **LC.TXD** register bit or the **TXD** hardware pin), the **LC.TOERR** bit is set and the LIN driver is disabled to allow **LIN** to be driven by external sources. The driver remains disabled as long as **LC.TXD** remains clear or **TXD** remains low. When both the **LC.TXD** bit is set and the **TXD** pin is high, the transmitter is automatically re-enabled, and the timeout timer is re-initialized. To support MOST ECL communications, the t_{LIN_MAX} timeout is longer than the maximum ECL pulse width.

For systems that must support longer times for the **LIN** dominant state, this timeout feature can be disabled by setting the **LC.NOMAX** bit.

6.3 Thermal Shutdown Condition

Under the fault condition where the **LIN** pin is shorted to power and the EHC is trying to drive standard LIN communications through the **TXD** pin, then the timeouts mentioned previously will not trigger due to the faster speed of LIN. The EHC should be able to recognize this condition since the **RXD** pin will be constantly high while the **TXD** pin is sending out data (during normal operation **RXD** should at least track all **TXD** low levels). However, if the EHC fails to recognize this condition, then the LIN driver current-limiting protection structures could excessively heat up the MPM85000 over time. As an added fail-safe feature, the MPM85000 includes thermal shutdown protection, wherein if the internal temperature reaches $T_{Shutdown}$, then the LIN driver is disabled to prevent excessive power dissipation, and the **LC.TEMPERR** bit is set. The LIN driver remains disabled until the internal temperature drops below $T_{Recover}$, at which point the LIN driver is automatically enabled again (and the **LC.TEMPERR** bit is cleared).

7 Reset Generator and VDDP

The MPM85000 has an integrated, precision reset generator that can be used as an ECU-wide power-on reset (POR) signal. This reset generator monitors the **VDDP** pin input voltage, which should be connected to the switched power supply of the MOST INIC and/or the EHC. When initial power is applied, the $\overline{\textbf{RESET}}$ pin is driven low by the MPM85000 until the **VDDP** pin voltage crosses above the rising trip point (V_{RST_RISE}). Once this threshold is crossed, the MPM85000 releases the $\overline{\textbf{RESET}}$ pin after a fixed delay (either t_{RST_DEL} or t_{RST_DELP}; see next paragraph for more information). Any subsequent voltage drops of the **VDDP** supply below the falling trip point (V_{RST_FALL}) cause the MPM85000 to assert the $\overline{\textbf{RESET}}$ pin low because the **VDDP** supply is in an improper range (also referred to as a **VDDP** invalid condition). At any time, the current state of the $\overline{\textbf{RESET}}$ pin is available through the Control Port by reading the value of **LSR.RESET** bit in the *Line Status Register* (LSR) (see Section 10.2.3).

The delay until $\overline{\textbf{RESET}}$ rises differs depending on how the MPM85000 woke up from *Sleep Mode*. If the MPM85000 transitioned to *Active Mode* based on ePHY network activity then t_{RST_DELP} applies, otherwise t_{RST_DEL} applies. Each delay is configurable through the Control Port, where the t_{RST_DEL} ranges from 1 ms to 45 ms using the **RD.DELAY[2:0]** bits in the *Reset Delay Register* (RD) (see Section 10.2.4), and the t_{RST_DELP} delay ranges from 1 ms to 10 ms using the **CR.EDELAY[2:0]** bits in the *Configuration Register* (CR) (see Section 10.2.8).

The $\overline{\textbf{RESET}}$ pin typically has an external pull-up resistor and can be wire-or'ed with other devices or application circuitry that drive the line low. When the MPM85000 is not driving the $\overline{\textbf{RESET}}$ signal low itself, the reset generator monitors the state of the pin and detects when other devices externally pull $\overline{\textbf{RESET}}$ low. Refer to Section 11.8 for $\overline{\textbf{RESET}}$ timing diagrams for both the internally and externally driven scenarios. Regardless of how $\overline{\textbf{RESET}}$ is driven low (e.g. by the MPM85000 or externally), when a logic low level is detected, the following fail-safe actions are taken by the MPM85000:

- the **LC.TXD** register bit is set for as long as $\overline{\textbf{RESET}}$ remains low,
- the **OR.HOLD** register bit is cleared for as long as $\overline{\textbf{RESET}}$ remains low,
- The **LIN** pin driver is disabled for as long as $\overline{\textbf{RESET}}$ remains low, and
- The t_{RST_POFF} timer is started (which forces the MPM85000 to stay in *Active Mode* temporarily).

For robustness, extra timers are built in to keep the MPM85000 in *Active Mode* during reset conditions and to allow time for the **PWROFF** pin to be pulled low (or for the **OR.HOLD** bit to be set) once $\overline{\textbf{RESET}}$ is deasserted. Keeping the ECU in *Active Mode* allows for quicker recovery from fault conditions and keeps from disrupting network communication between other nodes.

When $\overline{\textbf{RESET}}$ is asserted, the t_{RST_POFF} timer is started and holds the MPM85000 in *Active Mode*. If the t_{RST_POFF} timer expires, then $\overline{\textbf{RESET}}$ is assumed stuck low (shorted low or invalid voltage) and the MPM85000 is no longer forced to stay in *Active Mode*; although other application events (e.g. qualified activity) can still force *Active Mode*.

When $\overline{\textbf{RESET}}$ goes high (deasserted), the t_{WACK} timer is re-started and forces *Active Mode* to allow time for application initialization, which typically includes pulling the **PWROFF** pin low (or setting the **OR.HOLD** bit). When either of these two conditions occur, the t_{WACK} timer is reset. If neither condition occurs before the t_{WACK} timer expires, then the external device managing *Active Mode* is assumed to be faulty and the MPM85000 is no longer forced to stay in *Active Mode*.

Another robustness feature added to the MPM85000, is the t_{POFF_DEL} timer, which holds the MPM85000 in *Active Mode* for a short period of time after **PWROFF** is released or the **OR.HOLD** bit is cleared. This timer permits recovery from momentary fault conditions and allows recovery time after an external device reset not visible on the $\overline{\textbf{RESET}}$ pin, such as a watchdog timer internal to the EHC or the MOST INIC device.

Lastly, if the **VDDP** pin indicates an invalid power supply voltage (and the MPM85000 asserts $\overline{\textbf{RESET}}$), then the **PWROFF** input is ignored (not allowed to force *Active Mode*). In a typical system, **PWROFF** is pulled-up to the **VDDP** pin voltage; therefore if **VDDP** is invalid, then **PWROFF** becomes invalid and cannot be relied on. This feature stops a faulty **VDDP** supply from keeping the MPM85000 from going to *Sleep Mode*.

8 Temperature Sensor

The MPM85000 includes a precision temperature sensor which can be configured to alert the EHC when programmable temperature thresholds are crossed. Automotive ECUs should be designed to handle all temperature extremes; however, some types of application circuitry (e.g. power amplifiers) may malfunction or experience permanent damage when exposed to temperatures above their operating limits. Using the MPM85000's internal temperature sensor in combination with EHC software routines for under- or over-temperature management eliminates the need for dedicated temperature monitoring circuitry, thereby reducing overall system cost and complexity.

The following three MPM85000 registers define the temperature thresholds (see Section 10.2.11):

- *Temperature Limit High Register* (TLIMHI)
- *Temperature Limit Low Register* (TLIMLO)
- *Temperature High Hysteresis Register* (THHYS)

Two additional registers store the temperature (in °C) measured by the MPM85000 (see Section 10.2.10):

- *Temperature High Register* (TEMPHI)
- *Temperature Low Register* (TEMPLO)

The temperature is measured periodically (the exact interval is defined by t_{CONV}; see Section 11.6) with the result stored separately as integer and fractional components. The integer component is stored in TEMPHI, and the fractional component is stored in TEMPLO.

MPM85000 internal circuitry associated with the temperature sensor compares the actual measured temperature to the programmed thresholds and automatically sets the **SR.iTEMP** bit when a temperature threshold is crossed. This action also causes the $\overline{\text{INT}}$ pin to be asserted low (assuming the **MR.mTEMP** bit is clear), which eliminates the need for EHC polling. The programmable thresholds include:

- High temperature threshold - when the temperature rises above TLIMHI
- High temperature recovery threshold - after rises above TLIMHI, when the temperature then falls below (TLIMHI - THHYS)
- Low temperature threshold - when the temperature falls below TLIMLO
- Low temperature recovery threshold - after falling below TLIMLO, when the temperature then rises above the TLIMLO value.

When the MPM85000 transitions to *Active Mode*, or when the limit registers are written, only the high and low temperature thresholds are checked. Once the temperature crosses a particular threshold, only then is the corresponding recovery threshold checked. For each limit register, only one temperature threshold direction is checked at any particular time. Therefore, when transitioning to *Active Mode*, the limit register values must be checked against the current temperature to make sure the proper temperature interrupts occur. In other words, if the MPM85000 transitions to *Active Mode* and the current temperature is already above the high threshold (or, conversely, if the current temperature is already below the low threshold), a temperature interrupt is not generated when the temperature eventually drops below the high recovery threshold (or, conversely, when the temperature eventually rises above the low recovery threshold).

The registers provided for setting thresholds and monitoring temperature are accessible via the Control Port.

8.1 MOST Implementation

The *MOST Specification [2]* defines how an ECU should respond to over-temperature events. This section provides application information on using the MPM85000 temperature sensor to implement the MOST over-temperature requirements; however, the over-temperature event handling procedures are also useful in non-MOST systems.

Temperature management functionality described in this section requires specific EHC behavior in response to MPM85000 generated interrupt events. Refer to Table 8-2 for more information.

The MOST Network temperature alert and recovery levels are listed below in Table 8-1.

Symbol	Name	Description
MOST Temperature Alert Levels:		
ϑ_{AppOff}	Individual Application shutdown	ECUs turn off the application circuitry while still leaving the network interface operational.
$\vartheta_{Shutdown}$	Temperature shutdown (request)	ECU sends request to the network PowerMaster to shutdown the network due to a temperature problem.
$\vartheta_{Critical}$	Critical emergency shutdown	If this temperature is reached, the EHC immediately shuts down all application circuitry, including the network interface.
MOST Temperature Recovery Levels:		
ϑ_{NetOn}	Network Operational	Once an ECU reaches $\vartheta_{Shutdown}$ or above (where the network is turned off), ϑ_{NetOn} is where the network should be restarted.
ϑ_{AppOn}	Individual Application restart	ECUs have cooled enough to turn the application circuitry back on.

Table 8-1: MOST Temperature Levels

Figure 8-1 illustrates the MOST temperature levels in the system and the over-temperature requirements of the application.

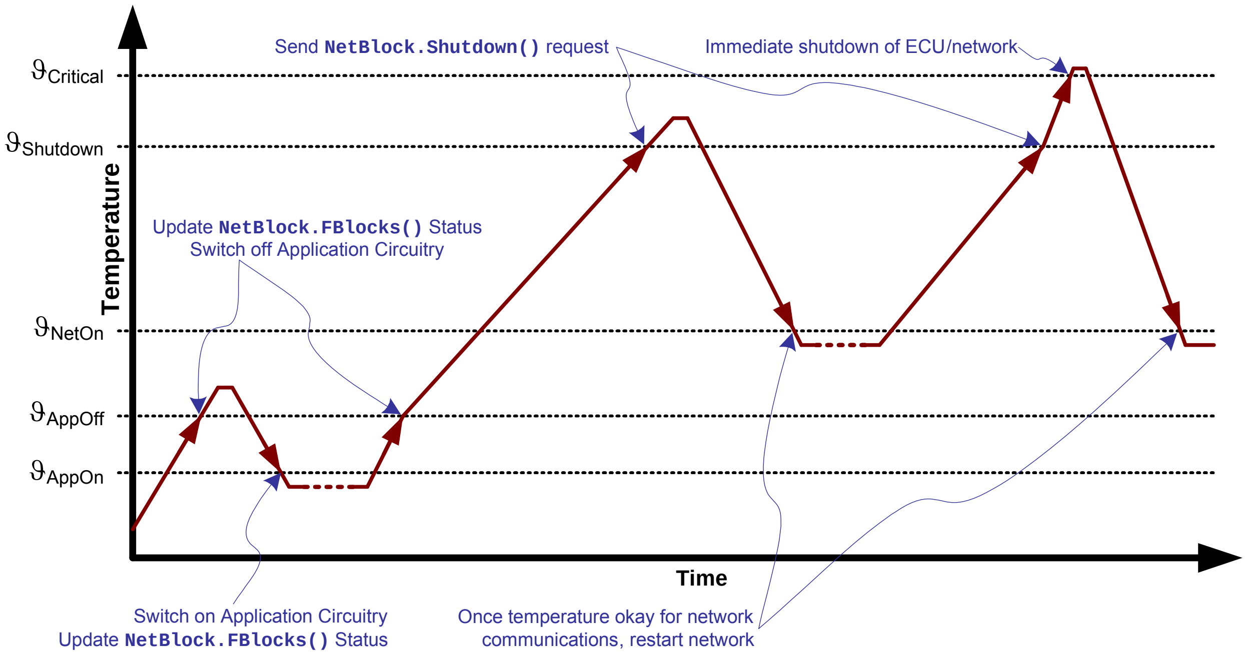


Figure 8-1: MOST Temperature Levels

The MPM85000 can be used to implement the MOST over-temperature requirements (shown above) by utilizing the interrupts generated (when specific thresholds are crossed) to alert the EHC, as shown in Table 8-2.

Cause of EHC Interrupt *	EHC Action	New Thresholds *	
		TLIMHI	**TLIMLO**
Temperature rises above ϑ_{AppOff}	- Set new thresholds in TLIMHI and TLIMLO - Update `NetBlock.FBlocks()` status - Switch off application circuitry	$\vartheta_{Shutdown}$	ϑ_{AppOn}
Temperature drops below ϑ_{AppOn}	- Set new threshold in TLIMHI - Set TLIMLO to a low value (threshold to be ignored) - Update `NetBlock.FBlocks()` status - Switch on application circuitry	ϑ_{AppOff}	-40
Temperature rises above $\vartheta_{Shutdown}$	- Set new thresholds in TLIMHI and TLIMLO - Send `NetBlock.Shutdown()` request	$\vartheta_{Critical}$	ϑ_{NetOn}
Temperature rises above $\vartheta_{Critical}$	- Immediate shutdown of ECU/network (TLIMHI and TLIMLO remain in their present state)	$\vartheta_{Critical}$	ϑ_{NetOn}
Temperature drops below ϑ_{NetOn}	- Set new thresholds in TLIMHI and TLIMLO - Once temperature okay for network communications, restart the network.	$\vartheta_{Shutdown}$	ϑ_{AppOn}

* This example assumes the initial register settings are TLIMHI = ϑ_{AppOff} and TLIMLO = -40 (low value - threshold to be ignored).

Table 8-2: MOST Over-Temperature Implementation Example

9 Power Management Port

The MPM85000 Power Management Port consists of three external interface pins: **PS1**, **PS0**, and **PWROFF**, which can be connected to a MOST INIC device or to an EHC configured for stand-alone operation. The **PS1** and **PS0** pins are open-drain outputs (external pull-up resistors required) that convey the status of the internal power management logic. Specifically, these pins are used to alert an external device (e.g. INIC/EHC) of transitions between the *VPRO Power Regions* (U_{Normal}, $U_{Critical}$, U_{Super}, U_{Low} - defined in Section 4.1). The **PS1** and **PS0** pins are also used to indicate initial MPM85000 power-up and *Switch-To-Power* (STP) events (when enabled).

The power management states conveyed by **PS1** and **PS0** are defined in Table 9-1 (where U_{Low} is highest priority and U_{Normal} is lowest priority). When the MPM85000 is in *Sleep Mode* the **PS1** and **PS0** pins are in a high impedance state.

PS1	PS0	State	Description	Priority
1	1	U_{Low}	**VPRO** operating in the *Low Power Region* (U_{Low})	1
0	1	POR/STP	Indicates initial power applied or an STP event *	2
1	0	$U_{Critical}$	**VPRO** operating in the *Critical Power Region* ($U_{Critical}$)	3
		U_{Super}	**VPRO** operating in the *Super Power Region* (U_{Super})	
0	0	U_{Normal}	**VPRO** operating in the *Normal Power Region* (U_{Normal})	4

* When **CR.NOSTP** is set (default), **PS[1:0]** = 01 only indicates initial power applied to the MPM85000. STP events are not conveyed on the **PS1**/**PS0** pins unless **CR.NOSTP** is clear.

Table 9-1: Power Management States

The initial power-up and STP events are conveyed on the **PS1**/**PS0** pins for $t_{PS\_HOLDSTP}$ after the rising edge of $\overline{\mathbf{RESET}}$, unless the higher priority U_{Low} event is detected. After that time, the **PS1**/**PS0** pins convey the current *VPRO Power Region*. If the **PS1**/**PS0** pins are connected to a MOST INIC and STP is not supported, the `INIC.RBDOptions(Options)` parameter should be configured to ignore STP events. Refer to the respective INIC documentation *[9, 10]* for more information regarding MOST INIC device operation.

The external device connected to **PS1**/**PS0** (e.g. INIC/EHC) responds to the state of these pins using the **PWROFF** pin, where a logic low level holds the MPM85000 in *Active Mode* and a logic high level indicates the external device is ready to be powered down. The MPM85000 powers down the application by releasing the $\overline{\mathbf{ENABLE}}$ pin, which is typically connected to the enable input of the ECU's external power regulator.

To keep the MPM85000 in *Active Mode* during short releases of the **PWROFF** pin (e.g. glitches, or a reset of the controlling device), the MPM85000 starts an internal timer (t_{POFF_DEL}) when a rising edge is detected on **PWROFF**. Once the t_{POFF_DEL} timer expires, the MPM85000 is no longer forced to stay in *Active Mode*. If no qualified activity exists (see Chapter 5, *Activity Detectors*), the MPM85000 transitions to *Sleep Mode*. This scenario assumes that the **OR.HOLD** register bit is cleared, which operates identically to the **PWROFF** pin.

If **PWROFF** transitions low prior to the internal timer reaching t_{POFF_DEL}, the timer is reset, the $\overline{\mathbf{ENABLE}}$ pin remains low, and the MPM85000 stays in *Active Mode*. This behavior allows the external device time to recover from a momentary reset condition (such as an internal watchdog reset) without causing a system power-down.

To handle the case of a quickly collapsing power supply, if a rising edge is detected on **PWROFF** while **VPRO** is in the U_{Low} region (**PS[1:0]** = 11), the MPM85000 immediately releases $\overline{\mathbf{ENABLE}}$ and enters *Sleep Mode* without the t_{POFF_DEL} delay and regardless of any existing qualified activity.

Figure 9-1 illustrates an example of **PWROFF** pin operation.

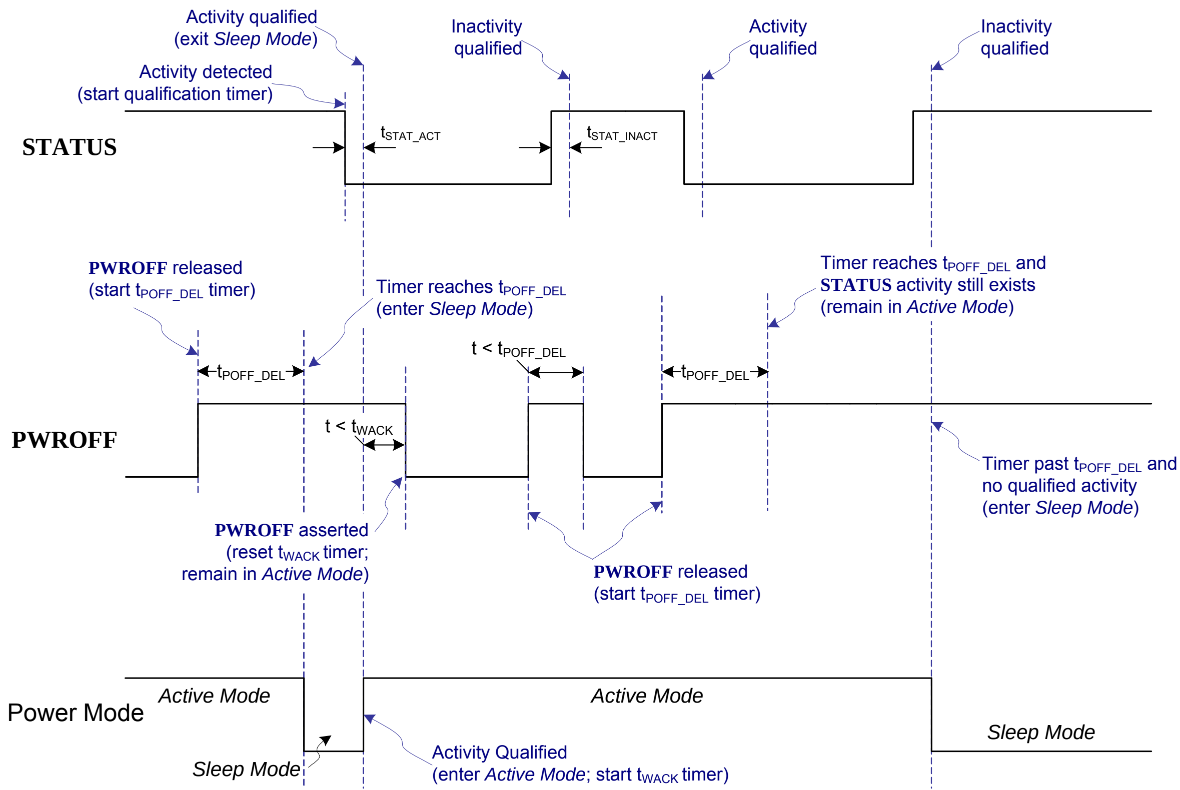


Figure 9-1: PWROFF Pin Operation

The **PWROFF** pin is gated by the **OR.HOLD** register bit (defined in Section 10.2.7); therefore, if **OR.HOLD** is set, the MPM85000 is prevented from releasing **$\overline{\text{ENABLE}}$** and entering *Sleep Mode*.

The **PWROFF** pin is ignored when the **VDDP** voltage is below the V_{RST_RISE} threshold (since **PWROFF** typically has a pull-up resistor tied to **VDDP**). In this situation, the MPM85000 enters *Sleep Mode* as soon as all qualified activity ceases to exist (**VDDP** invalid condition clears the **OR.HOLD** bit).

10 Control Port

The Control Port is an optional two-wire serial communication port that supports communication between the MPM85000 (bus slave) and an EHC (bus master). Through this interface, the EHC can access all MPM85000 control, status, and data registers (defined in Section 10.2). This communication interface is I^2C-compatible and supports the write byte, block write, read byte, and block read protocols. Data on the Control Port is received MSB-first.

The first byte of a Control Port access is the MPM85000 bus address plus the read/write (R/$\overline{W}$) bit. The R/$\overline{W}$ bit determines whether the EHC is reading or writing from the Control Port. The MPM85000 device address on the bus is 10h for MPM85000 write access and 11h for MPM85000 read access.

The **SCL** pin clocks data in and out; **SDA** is the bi-directional data pin. Communication on the bus is controlled by Start and Stop conditions. A Start condition is defined as a high to low transition on **SDA**, while **SCL** is high. A Stop condition is defined as a low to high transition on **SDA**, while the **SCL** is high. The MPM85000 acknowledges all data bytes received by pulling **SDA** low after the eighth bit of each byte is transmitted. This applies to both the write byte and block write protocols.

Figure 10-1 illustrates the MPM85000 in an I^2C environment. For information on the I^2C protocol, refer to the *I2C-Bus Specification [5]*.

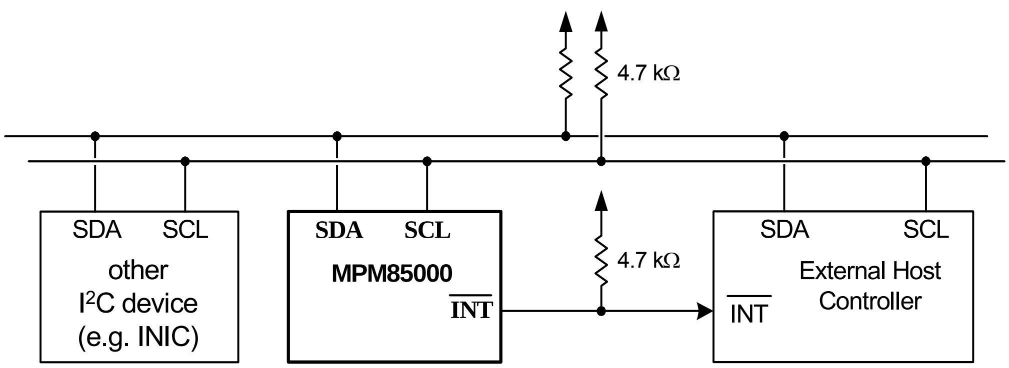


Figure 10-1: Control Port Pin Connections

The **$\overline{INT}$** pin is driven low to alert the EHC of various power management interrupt events (defined in Section 10.1). **$\overline{INT}$** is an open-drain, active low output that can be wire-or'ed with the interrupt outputs of other devices into the EHC's interrupt input.

When writing data to the MPM85000, a pre-defined set of bytes must be sent to select the device, and then indicate the location in the device (i.e. register) to access. The beginning of transmission is marked by a Start condition. The first byte specifies the device address, as well as whether the operation is a read or a write. The MPM85000 address (0001 000b) occupies the upper seven bits of the first byte; the R/$\overline{W}$ bit is the LSB. When the Control Port receives an address byte of 10h (MPM85000 address and R/$\overline{W}$ bit clear), it acknowledges reception of the byte through an acknowledge bit and the rest of the data is written into the Control Port. The second byte transmitted by the external system is the memory address pointer (MAP) which indicates the register location to be written to (or read from) first.

The third byte is actual data which is written to the location within the MPM85000 pointed to by the MAP. The MAP value, internally stored by the MPM85000, is automatically incremented after writing a data byte. Therefore, successive bytes are written to increasing register addresses, supporting efficient transfer of a continuous block of data. Data can be continually written until a Stop condition occurs. If the MAP reaches FFh it wraps back to 00h on the next increment.

Figure 10-2 illustrates the bus transmission write sequence. The characters "S" and "P" represent the Start and Stop conditions for messages.

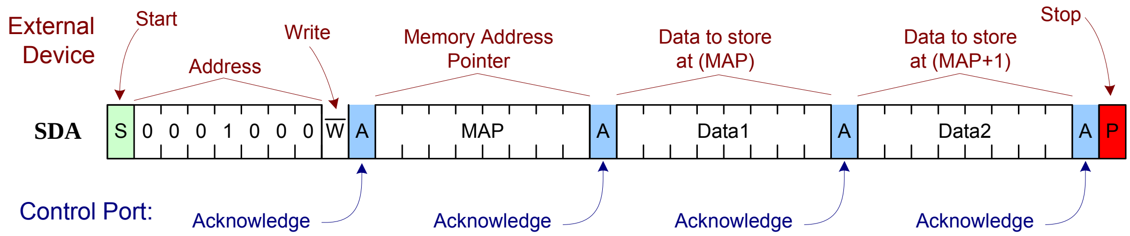


Figure 10-2: Control Port Write Sequence

In contrast to the write access, the read access generally consists of two parts. First, the target address (Memory Address Pointer, or MAP) must be sent to the device using a separate transmission cycle (delineated by Start conditions). Then the data can be read from the MAP address.

The beginning of transmission is marked by a Start condition. The first byte specifies the device address, as well as whether the operation is a read or a write. The MPM85000 address (0001 000b) occupies the upper seven bits of the first byte; the R/$\overline{\text{W}}$ bit is the LSB. To write the MAP, the LSB is cleared in the first byte. The second byte contains the target address (MAP). This first transmission can be ended by an optional Stop condition (not shown).

The second access is initiated with a (Repeated) Start condition, followed by the address byte, which must specify a read operation (LSB set to 1). The MPM85000 then transmits byte after byte (MAP auto-incremented) until a Stop condition occurs. If the MAP reaches FFh it wraps back to 00h on the next increment.

Figure 10-3 illustrates the bus transmission read sequence. The characters "S", "Sr", and "P" represent the Start, Repeated Start, and Stop conditions, respectively.

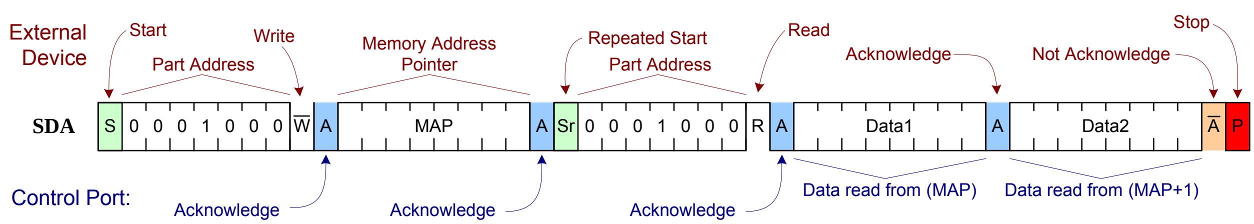


Figure 10-3: Control Port Read Sequence

10.1 Interrupt Events

The MPM85000 detects various operating conditions that may require EHC intervention (assuming the device is not being used in a stand-alone configuration). When such a condition is detected, a status register is updated and the MPM85000 generates an interrupt (**INT** pin driven low) to alert the EHC.

Most interrupt events can be masked via the *Mask Register* (MR), described in Section 10.2. Masking a particular interrupt does not prevent the condition from being logged in the corresponding status register (except in the case of disabling STP events with the **CR.NOSTP** bit); however, masking prevents the **INT** pin from being asserted. Interrupt masking has no affect on the **PS1** and **PS0** pins. Additionally, when valid activity is qualified on an input signal and the interrupt is masked, the **ENABLE** pin is still asserted if the device is in *Sleep Mode* (normal behavior). In other words, masking an interrupt does not prevent a wakeup event (transition to *Active Mode*) from occurring.

When the EHC services an MPM85000 interrupt, the *Interrupt Register* (IR) and the *Status Register* (SR) must both be read (regardless of mask bit settings) to guarantee that the interrupt condition is cleared (**INT** pin deasserted).

The various MPM85000 interrupt events (defined as conditions that can cause the MPM85000 to generate an interrupt) are listed in Table 10-1.

Interrupt Event	Wakeup Event	Status Bit(s) Set	Mask Setting
Activity Detection:			
LIN/ECL Activity Detected on **LIN** pin	Yes	IR.iLIN	MR.mLIN
LIN/ECL Inactivity Detected on **LIN** pin (after qualified LIN/ECL activity)	No	IR.iLIN	MR.mLIN
Activity Detected on **STATUS** pin	Yes	IR.iSTATUS	MR.mSTATUS
Inactivity Detected on **STATUS** pin (after qualified **STATUS** activity)	No	IR.iSTATUS	MR.mSTATUS
ePHY Activity Detected	Yes	IR.iEPHY	MR.mEPHY
ePHY Inactivity Detected (after qualified ePHY activity)	No	IR.iEPHY	MR.mEPHY
Activity Detected on **ON_SW** pin	Yes	IR.iONSW	MR.mONSW
Inactivity Detected on **ON_SW** pin (after qualified **ON_SW** activity)	No	IR.iONSW	MR.mONSW
Switch-To-Power (STP) Pulse Detected	Yes	IR.iPOR	CR.NOSTP*
LIN Transceiver Short-to-Power Error Detected	No	SR.LINPSE	-
Temperature Limits:			
Internal temperature exceeds high limit	No	SR.iTEMP	MR.mTEMP
Internal temperature drops below low limit	No	SR.iTEMP	MR.mTEMP
Internal temperature drops below high limit minus hysteresis after exceeding high limit	No	SR.iTEMP	MR.mTEMP
Internal temperature exceeds low limit after dropping below low limit	No	SR.iTEMP	MR.mTEMP

* This bit prevents the event from actually being detected, rather than only masking the resulting interrupt.

Table 10-1: Interrupt Events

Interrupt Event	Wakeup Event	Status Bit(s) Set	Mask Setting
Voltage Limits:			
VPRO exceeds V_{Th_Super}	No	IR.iVOLT + SR.SV	MR.mVOLT
VPRO drops below V_{Th_Super} - Hysteresis	No	IR.iVOLT + (SR.SV clear)	MR.mVOLT
VPRO drops below $V_{Th\_Critical}$	No	IR.iVOLT + SR.CV	MR.mVOLT
VPRO exceeds $V_{Th\_Critical}$ + Hysteresis	No	IR.iVOLT + (SR.CV clear)	MR.mVOLT
VPRO drops below V_{Th_Low}	No	IR.iVOLT + SR.LV	MR.mVOLT
VPRO exceeds V_{Th_Low} + Hysteresis	No	IR.iVOLT + (SR.LV clear)	MR.mVOLT

* This bit prevents the event from actually being detected, rather than only masking the resulting interrupt.

Table 10-1: Interrupt Events (Continued)

10.2 Registers

Control, status, and data registers of the MPM85000 are described in this chapter. All registers are accessible via the Control Port. The hexadecimal number above each register table indicates the Control Port MAP address, followed by the register mnemonic, and full register name. A read- or write-only register is indicated as such above the register table. If bits in the register have different access restrictions, the individual register bits in the table indicate so. If no indication is given at the register or bit level, then all bits are read and writable. All registers retain their values through *Sleep Mode*, unless noted otherwise.

10.2.1 Interrupt Register (IR)

The *Interrupt Register* (IR) is a read-only register that conveys the status of various operating conditions that may require EHC intervention. A set IR bit triggers an **INT** pin assertion if the corresponding bit in the *Mask Register* (MR) is clear.

00h IR* Interrupt Register (read-only)

Bit	Label	Description	Default
7, 6	rsvd	Reserved	00
5	iEPHY	ePHY network activity interrupt	0
4	iONSW	**ON_SW** pin interrupt	0
3	iLIN	**LIN** pin interrupt	0
2	iPOR	Initial power-on interrupt (also indicates STP events, when enabled)	0
1	iSTATUS	**STATUS** pin interrupt	0
0	iVOLT	**VPRO** voltage change interrupt	0

* This register is cleared after being read and when entering *Sleep Mode*.

Table 10-2: Interrupt Register (IR)

iEPHY ePHY network activity interrupt. When set, indicates a change between qualified activity and qualified inactivity on the **ERXP**/**ERXN** pins (used in MOST50 electrical systems). If the **MR.mEPHY** bit is clear, then the **INT** pin is driven low when **iEPHY** is set. If the **ERXP**/**ERXN** pins are used, this bit is set on initial power-up (in addition to the **iPOR** bit).

iONSW **ON_SW** pin interrupt. When set, indicates a valid state change was qualified on the **ON_SW** activity input pin. Rising and falling edges are qualified for glitch protection. If the **MR.mONSW** bit is clear, then the **INT** pin is driven low when **iONSW** is set.

iLIN **LIN** pin interrupt. When set, indicates a valid state change was qualified on the **LIN** pin. Rising and falling edges are qualified for glitch protection. If the **MR.mLIN** bit is clear, then the **INT** pin is driven low when **iLIN** is set. When using the **LIN** pin for actual LIN bus communication (rather than for wakeup event signalling), the **MR.mLIN** bit should be set to block interrupts from overloading the EHC. When the **LIN** pin is used for MOST ECL communication, then **LIN** pin interrupts can be used for EHC software timers, in lieu of using the hardware **RXD** pin.

iPOR Initial power-on interrupt (additionally serves as the STP event interrupt, when enabled). When set, indicates either initial power applied to the MPM85000 or that an STP event was detected. To support STP events, the **CR.NOSTP** bit must be cleared. This interrupt event cannot be masked (i.e. **INT** is always driven low when this bit is set).

iSTATUS **STATUS** pin interrupt. When set, indicates a valid state change was qualified on the **STATUS** pin. Rising and falling edges are qualified for glitch protection. If the **MR.mSTATUS** bit is clear, then the **INT** pin is driven low when **iSTATUS** is set.

iVOLT **VPRO** voltage interrupt. When set, indicates a valid state change (between the *VPRO Power Regions*) was qualified on the **VPRO** pin. The actual state is indicated through the **SR.SV**, **SR.CV**, or **SR.LV** bits. If the **MR.mVOLT** bit is clear, then the **INT** pin is driven low when **iVOLT** is set.

10.2.2 Status Register (SR)

The *Status Register* (SR) contains **VPRO** pin voltage indicator bits (**SV**, **CV**, and **LV**), which are used by the EHC to determine the current *VPRO Power Region.* The U_{Normal} region (refer to Figure 4-1 on page 22) is indicated when all three bits are clear. SR also contains the temperature sensor interrupt indicator as well as the LIN driver short circuit indicator.

01h SR Status Register

Bit	Label	Description	Default
7	rsvd	Reserved	0
6	LINPSE	**LIN** power short error	0
5	rsvd	Reserved	0
4	iTEMP	Temperature interrupt (read-only)	0
3	rsvd	Reserved	0
2	SV	Super-voltage indicator (read-only)	0
1	CV	Critical-voltage indicator (read-only)	0
0	LV	Low-voltage indicator (read-only)	0

Table 10-3: Status Register (SR)

LINPSE — **LIN** pin short-to-power error. When set, indicates the **LIN** pin did not go low within t_{SHORT} of being driven low via the **LC.TXD** bit (or possibly via the **TXD** pin when **LC.PSD** bit is set). This error implies that the **LIN** pin is shorted to power. When this bit is set, the LIN transceiver is disabled and the $\overline{\text{INT}}$ pin is asserted to alert the EHC that an error occurred. This bit must be cleared (written to zero) in order to re-enable the LIN transceiver.

iTEMP — Temperature sensor interrupt (read-only). When set, indicates that the device temperature crossed one of the programmed thresholds (see Chapter 8, *Temperature Sensor* for more information). If the **MR.mTEMP** bit is clear, then the $\overline{\text{INT}}$ pin is driven low when **iTEMP** is set. This bit is cleared with an SR read.

SV — Super-voltage indicator (read-only). When set, indicates that **VPRO** is in the *Super Power Region* (U_{Super}), as set by the **VCT.SVTH[1:0]** threshold.

CV — Critical-voltage indicator (read-only). When set, indicates that **VPRO** is lower than the $V_{Th\_Critical}$ voltage, as set by the **VCT.CVTH[1:0]** threshold. If **CV** is set and **LV** is clear, then **VPRO** is in the *Critical Power Region* ($U_{Critical}$).

LV — Low-voltage indicator (read-only). When set, indicates that **VPRO** is in the *Low Power Region* (U_{Low}), as set by the **VCT.LVTH[1:0]** threshold.

10.2.3 Line Status Register (LSR)

The *Line Status Register* (LSR) indicates the current status of various MPM85000 pins. All pins except $\overline{\text{RESET}}$ have qualification timers for glitch protection; therefore, the LSR bits only change state when the pin has been qualified for valid activity (bit set) and valid inactivity (bit clear).

02h LSR Line Status Register (read-only)

Bit	Label	Description	Default
7, 6	rsvd	Reserved	00
5	RESET	$\overline{\text{RESET}}$ assertion indicator	0
4	EPHY	ePHY network activity indicator	0
3	ONSW	**ON_SW** activity indicator	0
2	LIN	**LIN** activity indicator	0
1	STATUS	**STATUS** activity indicator	0
0	rsvd	Reserved	0

Table 10-4: Line Status Register (LSR)

RESET — $\overline{\text{RESET}}$ assertion indicator. Set when the $\overline{\text{RESET}}$ pin is low, either due to the internal reset generator or due to an external reset event. This bit is useful for EHCs that are not connected to the $\overline{\text{RESET}}$ pin output. This bit is cleared when the $\overline{\text{RESET}}$ pin is high.

EPHY — ePHY activity indicator. Indicates the state of the ePHY network activity detector (on the **ERXP/ERXN** pins). This bit is set when ePHY activity exists for t_{EPHY_ACT} and cleared when ePHY inactivity exists for t_{EPHY_INACT}.

ONSW — **ON_SW** pin activity indicator. Indicates the state of the **ON_SW** pin activity detector. This bit is set when the **ON_SW** pin is low for t_{ON_ACT} and cleared when the **ON_SW** pin is high for t_{ON_INACT}.

LIN — **LIN** pin activity indicator. Indicates the state of the **LIN** pin activity detector. This bit is set when the **LIN** pin is low for t_{LIN_ACT} and cleared when the **LIN** pin is high for t_{LIN_INACT}.

STATUS — **STATUS** pin activity indicator. Indicates the state of the **STATUS** pin activity detector. This bit is set when the **STATUS** pin is low for t_{STAT_ACT} and cleared when the **STATUS** pin is high for t_{STAT_INACT}.

10.2.4 Reset Delay Register (RD)

03h RD Reset Delay Register

Bit	Label	Description	Default
7…3	rsvd	Reserved	00000
2…0	DELAY[2:0]	Reset generator delay (for non-ePHY network activity wakeup events)	111

Table 10-5: Reset Delay Register (RD)

DELAY[2:0] Reset generator delay (t_{RST_DEL}) for non-ePHY network activity wakeup events. The MPM85000 $\overline{\textbf{RESET}}$ pin is driven low when the **VDDP** voltage is below V_{RST_FALL}. Once **VDDP** rises above V_{RST_RISE}, $\overline{\textbf{RESET}}$ remains low for an additional period of time (defined by these bits) before going high.

000 - 1.2 ms
001 - 2 ms
010 - 4 ms
011 - 8 ms
100 - 12 ms
101 - 20 ms
110 - 30 ms
111 - 45 ms (default)

DELAY[2:0] assumes the MPM85000 did not wakeup due to ePHY network activity (**IWE.wEPHY** clear). If the MPM85000 transitioned to *Active Mode* because of ePHY activity, a different delay (t_{RST_DELP} - set by the **CR.EDELAY[2:0]** bits) is used.

10.2.5 VPRO Comparator Threshold Register (VCT)

The *VPRO Comparator Threshold Register* (VCT) defines the trip points (thresholds) for the *VPRO Power Regions*, as illustrated in Figure 4-1 on page 22. These trip points alert the EHC to device power supply variations. These thresholds are applicable at the MPM85000 **VPRO** pin; therefore, they do not include voltage drop due to load-dump filtering. When specifying ECU thresholds, the load-dump filtering voltage drop ($V_{LoadDump}$ - see Figure 4-2 on page 23) should be taken into account when setting these thresholds.

04h VCT VPRO Comparator Threshold Register

Bit	Label	Description	Default
7, 6	rsvd	Reserved	00
5, 4	SVTH[1:0]	Super-voltage threshold	10
3, 2	CVTH[1:0]	Critical-voltage threshold (and also V_{STP_HI} threshold)	01
1, 0	LVTH[1:0]	Low-voltage threshold	01

Table 10-6: VPRO Comparator Threshold Register (VCT)

SVTH[1:0] Super-voltage threshold. Determines the **VPRO** rising-edge threshold V_{Th_Super}.
11 - 16.0 V
10 - 15.5 V (default)
01 - 15.0 V
00 - 14.5 V

CVTH[1:0] Critical-voltage threshold (and also V_{STP_HI} threshold). Determines the **VPRO** falling-edge threshold $V_{Th\_Critical}$ and also the **VBATT_F** rising-edge threshold used during STP event detection. Refer to Section 4.2 for more information on STP events.

CVTH[1:0]	$V_{Th\_Critical}$	V_{STP_HI}
11	9.5 V	7.5 V
10	9.0 V	7.0 V
01	8.5 V (default)	6.5 V (default)
00	8.0 V	6.0 V

Table 10-7: Critical-Voltage Threshold and STP Threshold Settings

LVTH[1:0] Low-voltage threshold. Determines the **VPRO** falling-edge threshold V_{Th_Low}.
11 - 7.0 V
10 - 6.5 V
01 - 6.0 V (default)
00 - 5.5 V

10.2.6 LIN Control Register (LC)

05h LC LIN Control Register

Bit	Label	Description	Default
7	TEMPERR	Temperature error (read-only)	0
6	PSD	Pin short detect	0
5	NOMAX	No maximum	0
4, 3	SLEW[1:0]	Slew rate control	00
2	TOERR	Timeout error (read-only)	0
1	RXD	LIN receive data (read-only)	1
0	TXD	LIN transmit data	1

Table 10-8: LIN Control Register (LC)

TEMPERR Temperature error (read-only). When set, the LIN transmitter is disabled due to an over-temperature ($T_{Shutdown}$) condition. Bit is cleared when the temperature drops below $T_{Recover}$.

PSD Pin short detect. When set, the **TXD** hardware pin is checked as part of the short-to-power fail-safe with the result indicated by the **SR.LINPSE** bit. When **PSD** is clear, only the **TXD** bit is checked for short-to-power errors.

NOMAX No maximum. When set, the LIN transceiver dominant signal timeout is disabled and the **LIN** pin can be driven dominant (low) for an unlimited period of time. Normally, this bit is clear and the LIN transceiver only transmits a dominant (low) signal (from either the **TXD** pin or **TXD** bit) for t_{LIN_MAX} before disabling the LIN transceiver, and setting the **TOERR** bit. Once the **TXD** pin and **TXD** bit are both high, the LIN transceiver is automatically re-enabled and **TOERR** is cleared.

SLEW[1:0] Slew rate control. Determines the slew rate for the LIN transmitter. The higher slew rate settings support faster LIN bus communication; however, EMI increases with slew rate.

00 - 2 V/µs. Supports LIN transmission rates of 20 kbaud (default).
01 - 1 V/µs. Supports LIN transmission rates of 10.4 kbaud.
10 - No slope control. Supports the highest LIN baud rates. This setting is recommended for applications implementing high-speed LIN bus communication (20 kbaud or higher).
11 - 0.05 V/µs. Supports MOST ECL transmission rates and provides the lowest EMI.

TOERR Timeout error (read-only). When set, indicates that the LIN transceiver is disabled due to **LIN** being low for greater than t_{LIN_MAX}. This bit is automatically cleared and the LIN transmitter re-enabled once the **TXD** pin is high and the **TXD** bit is set. The LIN transceiver timeout can be disabled by setting the **NOMAX** bit if longer bit times are needed.

RXD LIN receive data (read-only). This bit tracks the **LIN** pin and **RXD** pin values, and can be used in lieu of the **RXD** pin when the LIN interface is used at lower frequencies (e.g. MOST ECL).

TXD LIN transmit data. This bit controls the LIN driver and is logically and'ed with the **TXD** pin. When either the **TXD** bit or the **TXD** pin is low, the LIN transceiver drives the **LIN** pin low. The **TXD** bit can be used in lieu of the **TXD** pin when the LIN interface is used at lower frequencies (e.g. MOST ECL), in which case, the **TXD** pin should be held high to not interfere with the **TXD** bit operation. The **TXD** bit is automatically set if the **SR.LINPSE** bit is set (indicating a power-short error). Once set, the **SR.LINPSE** bit must be cleared to allow writing the **TXD** bit again. When the **TOERR** bit is set, (indicating the LIN transceiver timed out and is disabled), clearing the **TXD** bit does not drive the **LIN** pin low. To re-enable the LIN driver, the **TXD** bit must be set (while the **TXD** pin is held high). This clears **TOERR** and allows **TXD** to drive **LIN** again.

10.2.7 Override Register (OR)

The *Override Register* (OR) contains bits that allow input activity pins to be ignored. This allows the MPM85000 to be placed in *Sleep Mode* even if qualified activity is present on activity inputs. This is particularly useful if hardware errors have occurred. The override bits are automatically cleared when the respective pin changes state, thereby indicating that the hardware error condition no longer exists and the input can once again be used to qualify activity and inactivity conditions.

06h OR Override Register

Bit	Label	Description	Default
7	rsvd	Reserved	0
6	oEPHY	Override ePHY network activity detector	0
5	oLIN	Override **LIN** pin activity detector	0
4	oONSW	Override **ON_SW** pin activity detector	0
3	oSTATUS	Override **STATUS** pin activity detector	0
2	HOLD	Hold bit	0
1, 0	rsvd	Reserved	00

Table 10-9: Override Register (OR)

oEPHY — Override ePHY network activity detector. When set, allows the device to enter *Sleep Mode* even when qualified activity exists at the ePHY network activity detector (**LSR.EPHY** set). This bit is automatically cleared when the ePHY network activity detector changes state (indicated by **LSR.EPHY** changes).

oLIN — Override **LIN** pin activity detector. When set, allows the device to enter *Sleep Mode* even when the **LIN** pin is stuck in the dominant state (low - **LSR.LIN** set). This bit is automatically cleared when **LIN** changes state (indicated by **LSR.LIN** changes).

oONSW — Override **ON_SW** pin activity detector. When set, allows the device to enter *Sleep Mode* even when the **ON_SW** pin is stuck low (**LSR.ONSW** set). This bit is automatically cleared when **ON_SW** changes state (indicated by **LSR.ONSW** changes).

oSTATUS — Override **STATUS** pin activity detector. When set, allows the device to enter *Sleep Mode* even when the **STATUS** pin is stuck low (**LSR.STATUS** set). This bit is automatically cleared when **STATUS** changes state (indicated by **LSR.STATUS** changes).

HOLD — Hold bit. Control signal for holding off *Sleep Mode*. When set, the MPM85000 is prevented from transitioning to *Sleep Mode* and the t_{WACK} timer is disabled. The EHC uses this bit (or the **PWROFF** hardware pin) to keep the MPM85000 from powering down until the EHC is ready. When this bit is cleared, the MPM85000 reverts to *Sleep Mode* after t_{POFF_DEL} time if no qualified input activity exists (assumes **PWROFF** is high and **VPRO** is not in the U_{Low} region). Under normal conditions, **HOLD** must be cleared, **PWROFF** must be high, and all activity inputs (e.g. **STATUS**, **ERXP**/**ERXN**, **LIN**, **ON_SW**) must be inactive for the MPM85000 to enter *Sleep Mode*. The **HOLD** bit is cleared when the $\overline{\textbf{RESET}}$ pin is low.

10.2.8 Configuration Register (CR)

08h CR Configuration Register

Bit	Label	Description	Default
7	$\overline{\text{WAKECV}}$	Wakeup in critical-voltage	*
6	NOSTP	Disable STP events	1
5	WAKESV	Wakeup in super-voltage	1
4	PDEPHY	Power-down ePHY network activity detector	0
3	rsvd	Reserved	0
2…0	EDELAY[2:0]	Reset generator delay (for ePHY network activity wakeup events)	111

* Default value set via the **WAKEHI** configuration pin.

Table 10-10: Configuration Register (CR)

$\overline{\text{WAKECV}}$ Wakeup in critical-voltage. This bit determines the lower bound of the *Allowed Wakeup Range* ($V_{WakeupRange}$). The default value (also used for initial power-up) is determined by the **WAKEHI** configuration pin, where **WAKEHI** tied to ground clears the initial state of $\overline{\text{WAKECV}}$ and **WAKEHI** tied to **VDDU** sets the initial state of $\overline{\text{WAKECV}}$.

When $\overline{\text{WAKECV}}$ is clear, the MPM85000 is allowed to wakeup from *Sleep Mode* when the **VPRO** pin voltage is in the *Critical Power Region* ($U_{Critical}$). The actual minimum wakeup threshold is V_{Th_Low}, which is set by the **VCT.LVTH[1:0]** bits.

When $\overline{\text{WAKECV}}$ is set, the MPM85000 is not allowed to wakeup from *Sleep Mode* when the **VPRO** pin voltage is in the *Critical Power Region* ($U_{Critical}$). The actual minimum wakeup threshold is $V_{Th\_Critical}$, which is set by the **VCT.CVTH[1:0]** bits.

NOSTP Disable STP events. When clear, STP events detection is enabled (STP events are combined with the initial power applied events bits **IR.iPOR** and **IWE.wPOR**). To support STP event detection and qualification, the hardware must be configured to support t_{STP} (as shown in Section 13.5). When **NOSTP** is set (default), STP event detection is disabled.

WAKESV Wakeup in super-voltage. This bit determines the upper bound of the *Allowed Wakeup Range* ($V_{WakeupRange}$). When set (default), the MPM85000 is allowed to wakeup from *Sleep Mode* when the **VPRO** voltage is in the *Super Power Region* (U_{Super}), implying no upper bound to $V_{WakeupRange}$. When clear, the actual maximum wakeup threshold is V_{Th_Super}, which is set by the **VCT.SVTH[1:0]** bits.

PDEPHY Power-down ePHY network activity detector. When set, the ePHY network activity detector block is powered-down, thereby lowering overall *Sleep Mode* current. This bit should be set when MOST50 electrical network activity wakeup events are not supported (**ERXP**/**ERXN** pins unused).

EDELAY[2:0] Reset generator delay (t_{RST_DELP}) for ePHY network activity wakeup events. The MPM85000 $\overline{\text{RESET}}$ pin is driven low when the **VDDP** voltage falls below V_{RST_FALL}. Once **VDDP** rises above V_{RST_RISE}, $\overline{\text{RESET}}$ remains low for an additional period of time (defined by these bits) before going high.

000 -	1.2 ms	100 -	5 ms
001 -	2 ms	101 -	6 ms
010 -	3 ms	110 -	8 ms
011 -	4 ms	111 -	10 ms (default)

EDELAY[2:0] assumes the MPM85000 woke up due to ePHY network activity (**IWE.wEPHY** set). If the MPM85000 transitioned to *Active Mode* due to activity at a different input (**IWE.wEPHY** clear), a different delay (t_{RST_DEL} - set by the **RD.DELAY[2:0]** bits) is used.

10.2.9 Mask Register (MR)

The *Mask Register* (MR) is used to prevent the various interrupt events from causing an $\overline{\text{INT}}$ pin assertion; however, they do not affect the corresponding bit in IR (see Section 10.2.1) from being set.

09h MR Mask Register

Bit	Label	Description	Default
7	rsvd	Reserved	0
6	mLIN	Mask **LIN** pin interrupts	1
5	rsvd	Reserved	0
4	mONSW	Mask **ON_SW** pin interrupts	1
3	mSTATUS	Mask **STATUS** pin interrupts	1
2	mEPHY	Mask ePHY network activity/inactvity interrupts	1
1	mTEMP	Mask temperature threshold interrupts	1
0	mVOLT	Mask **VPRO** voltage monitor interrupts	1

Table 10-11: Mask Register (MR)

mLIN — Mask **LIN** pin interrupts. When set (default), blocks the **IR.iLIN** bit from asserting the $\overline{\text{INT}}$ pin. The **IR.iLIN** bit is set on any change in the **LSR.LIN** bit (see Figure 6-1).

mONSW — Mask **ON_SW** pin interrupts. When set (default), blocks the **IR.iONSW** bit from asserting the $\overline{\text{INT}}$ pin. The **IR.iONSW** bit is set on any change in the **LSR.ONSW** bit (see Figure 5-5).

mSTATUS — Mask **STATUS** pin interrupts. When set (default), blocks the **IR.iSTATUS** bit from asserting the $\overline{\text{INT}}$ pin. The **IR.iSTATUS** bit is set on any change in the **LSR.STATUS** bit (see Figure 5-3).

mEPHY — Mask ePHY network activity/inactivity (on **ERXP**/**ERXN**) interrupts. When set (default), blocks the **IR.iEPHY** bit from assertion the $\overline{\text{INT}}$ pin. The **IR.iEPHY** bit is set on any change in the **LSR.EPHY** bit (see Figure 5-4).

mTEMP — Mask temperature threshold interrupts. When set (default), blocks the **SR.iTEMP** bit from asserting the $\overline{\text{INT}}$ pin. The **SR.iTEMP** bit is set when the temperature sensor crosses programmed thresholds (see Chapter 8, *Temperature Sensor* for more information).

mVOLT — Mask **VPRO** voltage monitor interrupts. When set (default), blocks the **IR.iVOLT** bit from asserting the $\overline{\text{INT}}$ pin. The **IR.iVOLT** bit is set on any change in the **SR.SV**, **SR.CV**, or **SR.LV** bits (see Chapter 4, *Voltage Monitors* for more information).

10.2.10 Temperature Sensor Registers

0Ah TEMPHI Temperature High Register

Bit	Label	Description	Default
7…0	TEMP[10:3]	Measured temperature (integer portion)	00h

Table 10-12: Temperature High Register (TEMPHI)

TEMP[10:3] Integer component of the measured temperature (in °C). This register stores the integer portion of the measured temperature, while the fractional portion is stored in TEMPLO. Temperature data is stored in two’s complement format, as shown in Table 10-14.

0Bh TEMPLO Temperature Low Register

Bit	Label	Description	Default
7…5	TEMP[2:0]	Measured temperature (fractional portion)	000
4…0	rsvd	Reserved	00000

Table 10-13: Temperature Low Register (TEMPLO)

TEMP[2:0] Fractional component of the measured temperature (in °C). This register stores the fractional portion of the measured temperature, while the integer portion is stored in TEMPHI. Temperature data is stored in two’s complement format, as shown in Table 10-14.

Temperature (°C)	TEMP[10:0]
-64.0	1100 0000 000
-63.0	1100 0001 000
-1.0	1111 1111 000
-0.125	1111 1111 111
0.0	0000 0000 000
1.0	0000 0001 000
1.875	0000 0001 111
64.0	0100 0000 000
127.0	0111 1111 000

Table 10-14: Temperature Bit Decode

10.2.11 Temperature Limit Registers

The temperature limit registers allow the EHC to be notified when a temperature threshold is crossed, rather than having to poll the device. Supporting two limits allows alerts on temperature conditions both above and below the current temperature value.

0Ch TLIMHI Temperature Limit High Register

Bit	Label	Description	Default
7	rsvd	Reserved	
6…0	TLHI[6:0]	High temperature threshold compare	55h

Table 10-15: Temperature Limit High Register (TLIMHI)

TLHI[6:0] High temperature threshold compare. Stores the high temperature limit (default of 85 °C) to compare against the measured temperature. The resolution is 1 °C. If the temperature measurement exceeds this limit (rising-check), then the **SR.iTEMP** bit is set. If the temperature then drops below this limit minus the **THHYS.HYS[4:0]** hysteresis (falling-check), then the **SR.iTEMP** bit is set again. If the **MR.mTEMP** mask bit is clear when **SR.iTEMP** is set, then the $\overline{\text{INT}}$ pin is asserted. When exiting *Sleep Mode* or when writing this register, the first interrupt based on **TLHI[6:0]** is always a rising-check. Falling-checks do not occur until after a rising-check interrupt occurs. This register does not support a sign bit; therefore, TLIMHI can only be set to non-negative values.

0Dh TLIMLO Temperature Limit Low Register

Bit	Label	Description	Default
7…0	TLLO[7:0]	Low temperature threshold compare	00h

Table 10-16: Temperature Limit Low Register (TLIMLO)

TLLO[7:0] Low temperature threshold compare. Stores the low temperature limit (default of 0 °C) to compare against the measured temperature. The resolution is 1 °C and bit 7 is the sign bit. If the temperature measurement drops below this limit (falling-check), then the **SR.iTEMP** bit is set. If the temperature then rises above this limit (rising-check), the **SR.iTEMP** bit is set again. If the **MR.mTEMP** mask bit is clear when **SR.iTEMP** is set, then the $\overline{\text{INT}}$ pin is asserted. When exiting *Sleep Mode* or when writing this register, the first interrupt based on **TLLO[7:0]** is always a falling-check. Rising-checks do not occur until after a falling-check interrupt occurs.

0Eh THHYS Temperature High Hysteresis Register

Bit	Label	Description	Default
7…5	rsvd	Reserved	000
4…0	HYS[4:0]	Hysteresis for high temperature threshold	00101

Table 10-17: Temperature High Hysteresis Register (THHYS)

HYS[4:0] Hysteresis for high temperature threshold. Stores the high temperature hysteresis (default of 5 °C). The resolution is 1 °C. Once the measured temperature has risen above the high temperature threshold (defined in TLIMHI), the temperature is then compared to the TLIMHI value minus this hysteresis value. When that threshold is crossed (falling-check), the **SR.iTEMP** bit is set. If the **MR.mTEMP** mask bit is clear when **SR.iTEMP** is set, then the $\overline{\text{INT}}$ pin is asserted.

10.2.12 Initial Wakeup Event Register (IWE)

The *Initial Wakeup Event Register* (IWE) indicates the reason the MPM85000 transitioned from *Sleep Mode* to *Active Mode*. The **VPRO** voltage must be in the *Allowed Wakeup Range*, $V_{WakeupRange}$ (defined in Section 4.1) to exit *Sleep Mode*. For MOST Network applications, this register can be used by the EHC to fill in the `NetBlock.DeviceInfo(WakeInfo)` parameters. Refer to the *MOST FunctionBlock NetBlock [8]* documentation for more information.

0Fh IWE Initial Wakeup Event Register (read-only)

Bit	Label	Description	Default
7, 6	rsvd	Reserved	00
5	wEPHY	Wakeup due to ePHY network activity	0
4	wONSW	Wakeup due to **ON_SW** pin low	0
3	wLIN	Wakeup due to **LIN** pin low	0
2	wPOR	Wakeup due to initial power applied (or STP event, when enabled)	0
1	wSTATUS	Wakeup due to **STATUS** pin low	0
0	rsvd	Reserved	0

Table 10-18: Initial Wakeup Event Register (IWE)

wEPHY — Wakeup due to ePHY network activity. When set, indicates qualified activity on the ePHY pins **ERXP**/**ERXN** (used in MOST50 electrical systems) as the wakeup event (network).

wONSW — Wakeup due to **ON_SW** pin low. When set, indicates the **ON_SW** pin going low (and qualified) as the wakeup event (local).

wLIN — Wakeup due to **LIN** pin low. When set, indicates the **LIN** pin going low (and qualified) as the wakeup event (network).

wPOR — Wakeup due to initial power applied (or STP event, when enabled). When set, indicates initial power applied to the MPM85000 or an STP event as the wakeup event (network). To support STP events, the **CR.NOSTP** bit must be cleared.

wSTATUS — Wakeup due to **STATUS** pin low. When set, indicates the **STATUS** pin going low (and qualified) as the wakeup event (network wakeup event when connected to FOR/OEC or Rx PHY; local wakeup event otherwise).

10.2.13 Data Registers

Sixteen *Data Storage Registers* (DS0 - DSF) are provided to store user-defined data while in *Sleep Mode*, when the rest of the ECU is powered off. These registers can be read or written multiple times as opposed to the *OTP Data Registers*, which can only be written once. The *Data Storage Registers* do not retain their values if MPM85000 input power (i.e. vehicle battery power) is removed.

10h-1Fh DS0-DSF Data Storage Registers 0 through Fh

Bit	Label	Description	Default
7…0	DSn[7:0]	Data storage register bits	00h

Table 10-19: Data Storage Registers (DS0 - DSF)

Eight *OTP Data Registers* (OD0 - OD7) provide access to 8 bytes (64 bits) of the 56 available one-time programmable (OTP) memory bytes, selected via the OTP control register, OCS. The 56 OTP bytes are provided to permanently (retained through battery power interruptions) store user-defined data. The OTP data is read and programmed 64 bits at a time. Once an OTP bit is programmed to a ’1’, it can never be reprogrammed to a ’0’; however, within a bank of 64 bits that have already been programmed, bits that are ’0’ can be reprogrammed to ’1’.

30h-37h OD0-OD7 OTP Data Registers 0 through 7h

Bit	Label	Description	Default
7…0	ODn[7:0]	OTP data register bits for OTP bank selected by **OCS.CELL[2:0]**	00h

Table 10-20: OTP Data Registers (OD0 - OD7)

10.2.14 OTP Control Registers

These registers are used to read and write data between actual OTP memory and *OTP Data Registers* OD0 to OD7.

2Fh OCS OTP Cell Select Register

Bit	Label	Description	Default
7…3	rsvd	Reserved	00000
2…0	CELL[2:0]	Selects which OTP register bank is visible through the *OTP Data Registers* OD0 through OD7 (30h to 37h).	000

Table 10-21: OTP Cell Select Register (OCS)

CELL[2:0] Pointer to OTP cell (8 bytes) to be read from or written to. Setting these bits alone does not cause the OTP memory to be accessed. Once **CELL[2:0]** are written, the **OTPC.UPDATE** bit must be set to read from OTP memory, or the **OTPP.PROG[3:0]** bits should be set to 1010b to cause a write to OTP memory.

000 - OTP cell 0: bytes 0 to 7 are mapped to registers OD0 to OD7, respectively.
001 - OTP cell 1: bytes 8 to 15 are mapped to registers OD0 to OD7, respectively.
010 - OTP cell 2: bytes 16 to 23 are mapped to registers OD0 to OD7, respectively.
011 - OTP cell 3: bytes 24 to 31 are mapped to registers OD0 to OD7, respectively.
100 - OTP cell 4: bytes 32 to 39 are mapped to registers OD0 to OD7, respectively.
101 - OTP cell 5: bytes 40 to 47 are mapped to registers OD0 to OD7, respectively.
110 - OTP cell 6: bytes 48 to 55 are mapped to registers OD0 to OD7, respectively.
111 - Reserved

38h OTPC OTP Control Register

Bit	Label	Description	Default
7	UPDATE	When set, updates the *OTP Data Registers* with the OTP cell contents pointed to by **OCS.CELL[2:0]**.	0
6…0	rsvd	Reserved	0000000

Table 10-22: OTP Control Register (OTPC)

UPDATE When set, causes the OTP memory cell, pointed to by **OCS.CELL[2:0]**, to be read into the *OTP Data Registers* (OD0 - OD7). The **UPDATE** bit is automatically cleared when the OTP memory read is finished; therefore, once **UPDATE** is set, OD0-OD7 should not be accessed until **UPDATE** is cleared.

39h OTPP OTP Programming Register

Bit	Label	Description	Default
7…4	rsvd	Reserved	0000
3…0	PROG[3:0]	When set to 1010b, the *OTP Data Registers* are used to program the OTP cell pointed to by **OCS.CELL[2:0]**.	0000

Table 10-23: OTP Programming Register (OTPP)

PROG[3:0] When set to 1010b, causes the data in the *OTP Data Registers* (OD0 - OD7) to be written to the OTP memory cell pointed to by the **OCS.CELL[2:0]** bits. The unprogrammed state of the OTP bits is '0'; therefore, only bits set to '1' are actually programmed. An OTP cell can be reprogrammed, provided the bits in the cell that change are initially '0'. The **PROG[3:0]** bits are automatically cleared when the OTP cell being programmed is finished; therefore, further operations shouldn't commence until **PROG[3:0]** is read as 0000b. When the **PROG[3:0]** bits are set to any value other than 1010b, no action is taken.

10.2.15 Product Information Registers

FCh PF Product Features Register (read-only)

Bit	Label	Description	Default
7…1	rsvd	Reserved	0000000
0	WAKEHI	Value of the **WAKEHI** pin sampled at initial power-up.	*

* Default value set via the **WAKEHI** configuration pin.

Table 10-24: Product Features Register (PF)

WAKEHI 0 - **WAKEHI** pin sampled low (ground) at power-up; **CR.WAKECV** initial state set to 0.
1 - **WAKEHI** pin sampled high (**VDDU**) at power-up; **CR.WAKECV** initial state set to 1.

FDh PID Product ID Register (read-only)

Bit	Label	Description	Default
7…0	PID[7:0]	Indicates the MPM85000 device	08h

Table 10-25: Product ID Register (PID)

FEh MID Manufacturer ID Register (read-only)

Bit	Label	Description	Default
7…0	MID[7:0]	Indicates SMSC	5Dh

Table 10-26: Manufacturer ID Register (MID)

FFh REV Revision Register (read-only)

Bit	Label	Description	Default
7…0	REV[7:0]	Indicates the revision of the MPM85000	*

* The default value of **REV[7:0]** is dependent on the actual hardware revision.

Table 10-27: Revision Register (REV)

REV[7:0] MPM85000 device revision:
84h - Revision E - The data sheet is applicable to this revision.
83h - Revision D
82h - Revision C
81h - Revision B
80h - Revision A

11 Electrical Characteristics

Specifications are subject to change without notice.

11.1 Absolute Maximum Ratings

Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this document is not implied.

Parameter			Min	Max	Unit
Storage Temperature			-55	150	°C
Power Supply Voltage for 12 V Core (**VPRO_HOLD**)		(Note 1)	-0.6	35	V
Power Supply (**VPRO_HOLD**) Ramp Rate		(Note 2)	50		µs/V
Maximum Input Voltage:	**LIN**	(Note 1)	-5	35	V
	VBATT_F	(Notes 1, 3, 4)	-0.3	35	V
	VPRO	(Notes 1, 5)	-0.3	35	V
	$\overline{\textbf{ENABLE}}$	(Note 1)	-0.3	35	V
	VDDU		-0.3	4	V
	All other pins		-0.3	**VDDU**+0.3	V
Current out of **VBATT_F**		(Notes 3, 4)		-50	mA
ESD Rating (HBM):	**LIN**, **ERXP**, **ERXN**			8000	V
	All other pins			2000	V

1. Immunity to transients greater than 40 V can be achieved with simple external circuitry, as shown in Figure 13-3.
2. This specification is typically satisfied by the ECU's load dump filter circuit. Depending on the application, an external RC network (shown in Figures 13-3, 13-4, and 13-5) can also be used to meet this requirement.
3. Current may be drawn from this pin if pulled below ground due to battery transients. This specification covers transient events and is not applicable at DC.
4. When used, a minimum series resistance of 27 kΩ is required between Battery Continuous Power and **VBATT_F**.
5. This **VPRO** value is equivalent to the $V_{SUP\_NON\_OP}$ parameter in the *LIN Specification [3]*.

Table 11-1: Absolute Maximum Ratings Electrical Characteristics

11.2 Guaranteed Operating Conditions

Parameter			Min	Typ	Max	Unit
Junction Temperature, T_J		(Notes 1, 2)	-40		110	°C
Power Supply Voltage:	**VPRO_HOLD**	(Notes 3, 4)	5.5	13.5	32	V
Voltage applied to pins:	**LIN**	(Note 3)	-3		32	V
	VBATT_F	(Note 3)	0		32	V
	VPRO	(Notes 3, 5)	5.5		32	V
	$\overline{\textbf{ENABLE}}$	(Note 3)	0		32	V
	VDDU		3.135		3.465	V
	All other pins		0		**VDDU**	V

1. Write operations to OTP memory are guaranteed from -40 to 85 °C.
2. Assumes the paddle is soldered to a solid ground plane using at least the recommended thermal via design consisting of four 20 mil vias connected with a 2×2 mm thermal landing.
3. Immunity to transients greater than 40 V can be achieved with simple external circuitry, as shown in Figure 13-3 and Figure 13-6.
4. See Section 11.9 for **VPRO_HOLD** minimum voltage requirements versus MicroPower regulator output current.
5. This **VPRO** value is equivalent to the V_{SUP} parameter in the *LIN Specification [3]*.

Table 11-2: Guaranteed Operating Conditions Electrical Characteristics

11.3 DC Characteristics

T_J = -40 to 110 °C; 5.5 V < **VPRO** = **VPRO_HOLD** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage: **SDA**, **SCL**, **ON_SW** **PWROFF**, **STATUS** **WAKEHI**, **RESET**, **TXD**	V_{IH}	 2.0 2.0 2.0			 V V V	
Input low voltage: **SDA**, **SCL**, **ON_SW** **PWROFF**, **STATUS** **WAKEHI**, **RESET**, **TXD**	V_{IL}			 0.8 0.8 0.8	 V V V	
Output low voltage: **SDA**, **PS1**, **PS0**, **INT**, **NOACT**, **RESET**, **RXD** **ENABLE**	V_{OL}			 0.4 0.4 0.4	 V V V	I_{SINK} = -4 mA I_{SINK} = -4 mA (Note 1)
VDDP input leakage current	I_{VDDP_IN}	-5		5	µA	
Active Mode Current:						
VBATT_F (Note 2)	$I_{ACT\_BATT\_F}$		2	7	µA	(Note 3)
VPRO and **VPRO_HOLD**	I_{ACT}		860 1300	1200 1900	µA µA	(Note 3) (Note 4)
Sleep Mode Current:						
VBATT_F (Note 2)	$I_{SL\_BATT\_F}$		2	4	µA	(Notes 3, 5)
VPRO and **VPRO_HOLD**	I_{SL}		40	62	µA	(Notes 3, 5)

1. I_{SINK} for **ENABLE** varies with **VPRO_HOLD**. To meet the maximum V_{OL} of 0.4 V across all operating voltages, a minimum pull-up resistor value of 10 kΩ is required on **ENABLE**.
2. **VBATT_F** is only used in legacy systems supporting the diagnostic *Switch-To-Power* (STP) pulse. Refer to Section 13.5 for more information. In most implementations, **VBATT_F** is tied directly to GND ($I_{ACT\_BATT\_F}$ = $I_{SL\_BATT\_F}$ = 0 µA).
3. **LIN** = **VPRO** (recessive state); 9 V < (**VBATT_F** = **VPRO** = **VPRO_HOLD**) < 16 V.
4. **LIN** = 0 V (dominant state); 9 V < (**VBATT_F** = **VPRO** = **VPRO_HOLD**) < 16 V.
5. **VDDP** = 0 V.

Table 11-3: DC Electrical Characteristics

11.4 AC Characteristics

T_J = -40 to 110 °C; 5.5 V < **VPRO** = **VPRO_HOLD** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Initial power-up and STP **PS1/PS0** hold time	$t_{PS\_HOLDSTP}$		205		ms	**VPRO** ≥ V_{Th_Low} + V_{Hys_Low}
PWROFF rising hold time	t_{POFF_DEL}		215		ms	**VPRO** ≥ V_{Th_Low} + V_{Hys_Low}
$\overline{\text{RESET}}$ low hold time	t_{RST_POFF}		5.1		s	
Initial wakeup from *Sleep Mode* and $\overline{\text{RESET}}$ release hold time	t_{WACK}	4.1	5.1		s	Measured from the falling edge of $\overline{\text{ENABLE}}$ or the rising edge of $\overline{\text{RESET}}$

Table 11-4: AC Electrical Characteristics

11.5 Activity Detectors

T_J = -40 to 110 °C; 5.5 V < **VPRO** = **VPRO_HOLD** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
STATUS Activity Detection:						
STATUS activity duration *	t_{STAT_ACT}		115		µs	
STATUS inactivity duration	t_{STAT_INACT}		115		µs	
ePHY Activity Detection:						
ERXP/N activity duration *	t_{ePHY_ACT}		115		µs	
ERXP/N inactivity duration	t_{ePHY_INACT}		115		µs	
ERXP/N input capacitance	C_{ERXP}, C_{ERXN}		2.5		pF	
ERXP/N input range	t_{ePHY_IN}	-0.15		3	V	
ERXP/ERXN differential activity	V_{ePHY_DIFF}	0.6		2.0	V	(based on transition from *Sleep Mode* to *Active Mode*; not state of **NOACT** pin)
LIN Activity Detection:						
LIN activity duration *	t_{LIN_ACT}		95		µs	
LIN inactivity duration	t_{LIN_INACT}		165		µs	
LIN wakeup delay	t_{LIN_D}		30		µs	(from qualified **LIN** activity to $\overline{\text{ENABLE}}$ assertion)
ON_SW Activity Detection:						
ON_SW internal pull-up resistor	R_{ON_PU}		90		kΩ	
ON_SW activity duration *	t_{ON_ACT}		40		ms	
ON_SW inactivity duration	t_{ON_INACT}		40		ms	

* If in *Sleep Mode* when activity is qualified, and the **VPRO** supply is within the *Allowed Wakeup Range* ($V_{WakeupRange}$), the device transitions from *Sleep Mode* to *Active Mode*. The inactivity counters have no effect on exiting *Sleep Mode*.

Table 11-5: Activity Detectors Electrical Characteristics

11.6 Temperature Sensor

T_J = -40 to 110 °C; 9 V < **VPRO** = **VPRO_HOLD** < 16 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Temperature accuracy	Temp		2		°C	
Temperature resolution	ΔTemp		0.125		°C	
Conversion rate	t_{CONV}		83		ms	

Table 11-6: Temperature Sensor Electrical Characteristics

11.7 Voltage Monitors

T_J = -40 to 110 °C; 5.5 V < **VPRO** = **VPRO_HOLD** < 32 V; 0 V < **VBATT_F** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
VPRO Pin:						
Super-Voltage Threshold (rising voltage)	V_{Th_Super}	15	15.5	16	V	Default setting - see Section 10.2.5 for options
Super-Voltage Hysteresis	V_{Hys_Super}	300	500	700	mV	
Critical-Voltage Threshold (falling voltage)	$V_{Th\_Critical}$	8	8.5	9	V	Default setting - see Section 10.2.5 for options
Critical-Voltage Hysteresis	$V_{Hys\_Critical}$	300	500	700	mV	
Low-Voltage Threshold (falling voltage)	V_{Th_Low}	5.6	6	6.4	V	Default setting - see Section 10.2.5 for options
Low-Voltage Hysteresis	V_{Hys_Low}	300	500	700	mV	
VBATT_F Pin						
STP Rising Edge Threshold	V_{STP_HI}	6.1	6.5	6.9	V	Default setting - see Section 10.2.5 for options
STP Falling Edge Threshold	V_{STP_LO}	2.5	3	3.5	V	
STP Hysteresis	V_{STP_Hys}	300	500	700	mV	(Note 1)
STP Event Qualification Time	t_{STP}	2	3	4	s	

1. The STP hysteresis applies to both V_{STP_HI} and V_{STP_LO}.

Table 11-7: Voltage Monitors Electrical Characteristics

11.8 Reset Generator

T_J = -40 to 110 °C; 5.5 V < **VPRO = VPRO_HOLD** < 16 V; 0 V ≤ **VDDP** ≤ 3.6 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Trip point with **VDDP** rising	V_{RST_RISE}	3.01	3.08	3.13	V	
Trip point with **VDDP** falling	V_{RST_FALL}	2.95	3.03	3.09	V	
RESET Hysteresis	V_{RST_HYST}		45		mV	
V_{RST_RISE} to **RESET** high: Wakeup due to ePHY activity Wakeup due to other events	 t_{RST_DELP} t_{RST_DEL}		 10 45		 ms ms	 default setting, see Note 1 default setting, see Note 1
V_{RST_FALL} to **RESET** assertion delay	t_{RST_FALL}		2		µs	Full dropout (**VDDP** = 0 V)
VDDP dropout time required to trigger reset generator	t_{RST_MIN}	500			ns	see Note 2
VDDP for which **RESET** output is valid	V_{VALID}	0		3.6	V	

1. The default setting is shown in the table; however, t_{RST_DEL} is configurable via the **RD.DELAY[2:0]** bits, and t_{RSR_DELP} is configurable via the **CR.EDELAY[2:0]** bits.
2. Transient **VDDP** events shorter than the minimum t_{RST_MIN} value are guaranteed to be ignored. The typical dropout time required to trigger the reset generator varies with overdrive, as shown in Figure 11-1. In this figure, a **VDDP** dropout below the curve will not cause the **RESET** pin to assert.

Table 11-8: Reset Generator Electrical Characteristics

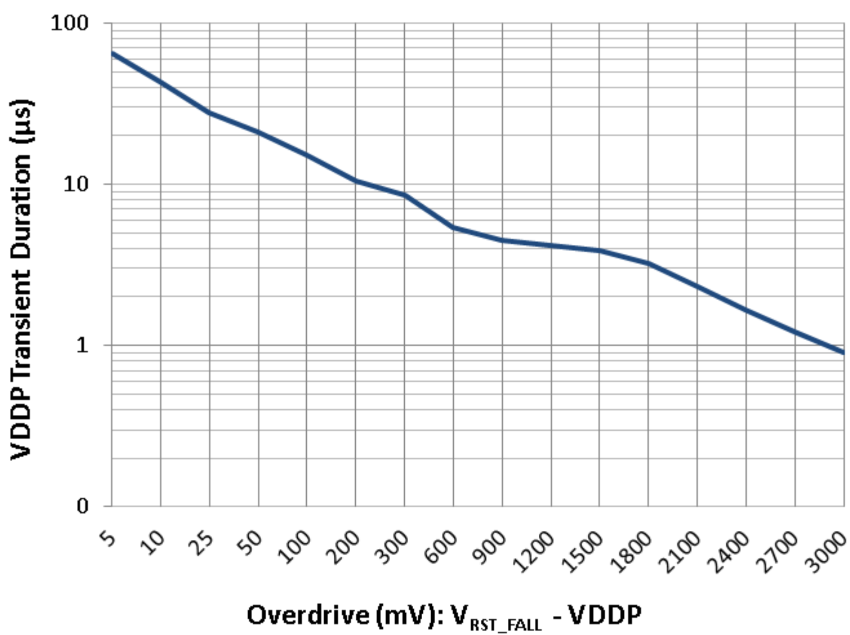


Figure 11-1: Typical Reset Generator Timing vs. Overdrive

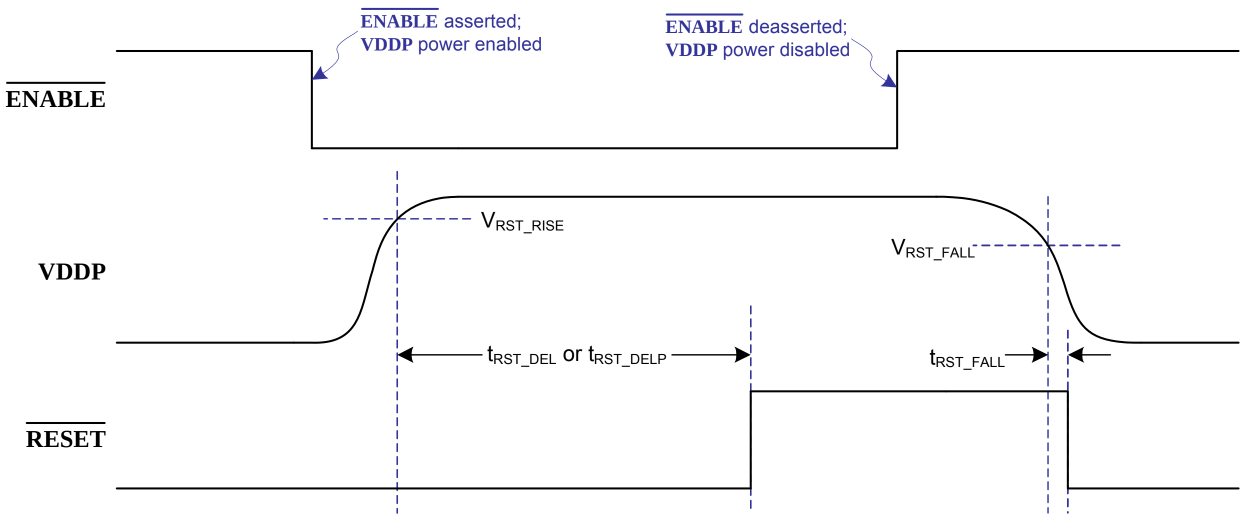


Figure 11-2: Reset Timing Diagram (internally driven)

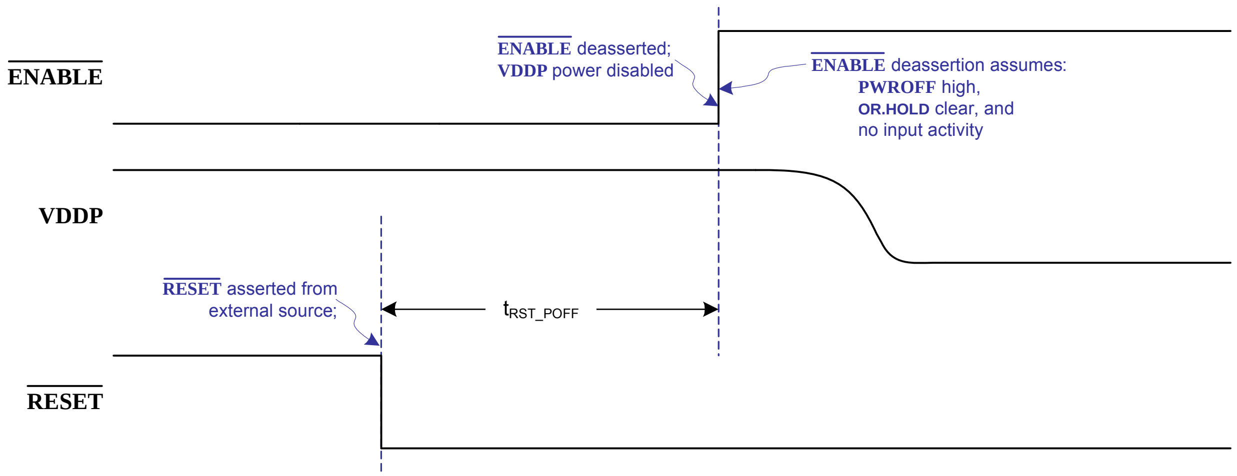


Figure 11-3: Reset Timing Diagram (externally driven)

11.9 MicroPower Regulator

T_J = -40 to 110 °C; 5.5 V < **VPRO** = **VPRO_HOLD** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	V_{DDU}	3.135	3.3	3.465	V	
Output current from **VDDU_OUT**	I_{LOAD}	90			µA	4.2 V ≤ **VPRO_HOLD** < 5.5 V
		860			µA	5.5 V ≤ **VPRO_HOLD** < 32 V
External NPN emitter current	I_{NPN_LOAD}	50			mA	**VDDU_OUT** = (**VDDU** + 1 V) h_{FE_NPN} > 100 V_{BE} < 1 V
Short-circuit current	I_{SHORT}			8	mA	**VDDU** = **VDDP** = 0 V **VPRO_HOLD** = 27 V No external NPN (Note 1)
External load capacitor	C_{ELOAD}		1		µF	No external NPN
			10		µF	External NPN connected
Load capacitor ESR (f = 10 kHz)	R_{ESR}		0.3	2	Ω	No external NPN
			0.3	1	Ω	External NPN connected

1. The I_{SHORT} parameter specifies the short-circuit current due to the MicroPower regulator's internal circuitry. If **VDDU** is shorted to ground while the **VDDP** supply is up, the **RESET** pin could be asserted and additional current will be pulled into the device due to internal ESD protection structures. The additional current is a function of the **VDDP** voltage and the external resistor value (typically 1 kΩ).

Table 11-9: MicroPower Regulator Electrical Characteristics

11.10 Control Port

T_J = -40 to 110 °C; 5.5 V < **VPRO = VPRO_HOLD** < 32 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high/low current	I_{IH}/I_{IL}			±5	μA	T_A < 85 °C
Hysteresis			650		mV	
Input capacitance	C_{IN}		2		pF	For **SCL**, **SDA** and $\overline{\textbf{INT}}$
Clock frequency	f_{SCL}			400	kHz	
Bus free time (Start to Stop)	t_{BUF}	1.3			μs	
Hold time (Start)	$t_{HD:STA}$	0.6			μs	
Setup time (Start)	$t_{SU:STA}$	0.6			μs	
Setup time (Stop)	$t_{SU:STP}$	0.6			μs	
Data hold time	$t_{HD:DAT}$	0			μs	
Data setup time	$t_{SU:DAT}$	0.6			μs	
Clock low period	t_{LOW}	1.3			μs	
Clock high period	t_{HIGH}	0.6			μs	
Clock/Data fall time (Note 1)	t_{FALL}			300	ns	
Clock/Data rise time (Note 1)	t_{RISE}			300 1000	ns ns	f_{SCL} > 100 kHz f_{SCL} ≤ 100 kHz

1. Rise and fall time specifications are based on the V_{IL} and V_{IH} values given in the *I2C-Bus Specification [5]* and not the V_{IL} and V_{IH} specifications given in Table 11-3.

Table 11-10: Control Port Electrical Characteristics

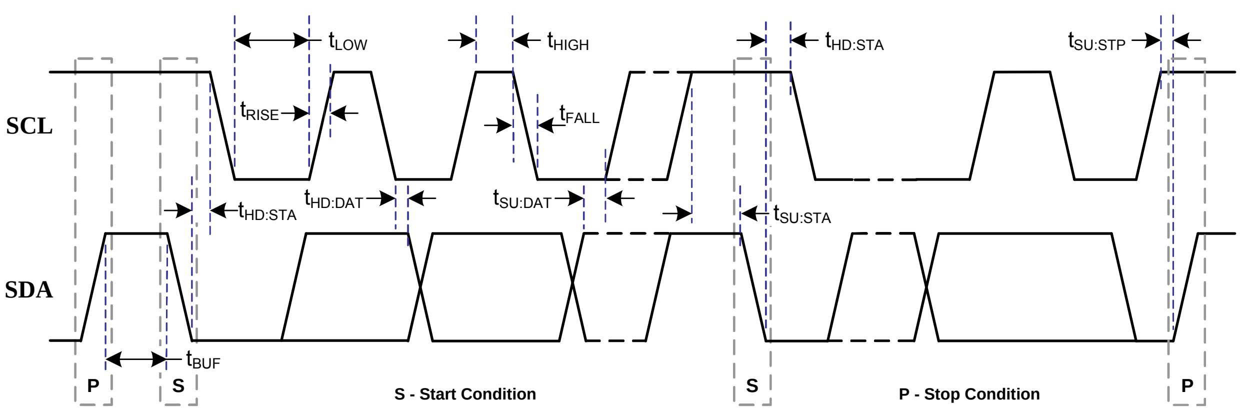


Figure 11-4: Control Port Timing Diagram

11.11 LIN Transceiver

The $V_{SUP\_NOM\_OP}$ and V_{SUP} equivalent LIN parameters can be found in Section 11.1 and Section 11.2, respectively. See Section 11.3 for **VPRO** supply currents. The **LIN** pin activity qualification time (glitch protection) to wakeup from *Sleep Mode* is t_{LIN_ACT} and is listed in Section 11.5.

11.11.1 General

T_J = -40 to 110 °C; 7V < **VPRO = VPRO_HOLD** < 18 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Bus leakage current - Dominant (driver off)	$I_{BUS\_PAS\_dom}$	-1			mA	**VPRO** = 14 V, **LIN** = 0 V; *Active Mode*
Bus leakage current - Recessive (driver off)	$I_{BUS\_PAS\_rec}$			10	µA	8 V ≤ **VPRO** ≤ 18 V 8 V ≤ **LIN** ≤ 18 V **LIN** ≥ **VPRO**
Bus leakage current - Loss of ground	$I_{BUS\_NO\_GND}$	-300		10	µA	**GND** = **VPRO** = 12 V 0 V < **LIN** ≤ 18 V
Bus leakage current - Loss of battery	$I_{BUS\_NO\_BAT}$	-23		23	µA	0 V < **LIN** ≤ 18 V
Operation bit time	t_{Bit}		50 96		µs µs	20 kbps transaction rate 10.4 kbps transaction rate
Short-To-Power detection	t_{SHORT}		10.5		ms	
TXD Timeout duration	t_{LIN_MAX}		750		ms	(see Section 10.2.6)
Thermal shutdown temperature	$T_{Shutdown}$		127		°C	
Thermal recovery temperature	$T_{Recover}$		110		°C	

Table 11-11: LIN Transceiver General Electrical Characteristics

11.11.2 DC Characteristics

T_J = -40 to 110 °C; 7 V < **VPRO = VPRO_HOLD** < 18 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
LIN Transmitter:						
Dominant output voltage	V_{BUSdom_DRV}			0.2 ×**VPRO**	V	R_{BUS} = 500 Ω
VPRO pull-up resistor (via diode)	R_{SLAVE}	20	35 650	47	kΩ kΩ	*Active Mode* *Sleep Mode*
Voltage drop across pull-up diode	$V_{SerDiode}$		0.7	1	V	
LIN short circuit current	I_{BUS_LIM}	40		125	mA	**LIN** = **VPRO** = 18 V Dominant state driven
LIN Receiver:						
Dominant input voltage	V_{BUSdom}			0.338 ×**VPRO**	V	
Recessive input voltage	V_{BUSrec}	0.608 ×**VPRO**			V	
Falling Threshold	V_{th_dom}	0.338 ×**VPRO**		0.512 ×**VPRO**	V	recessive-to-dominant
Rising Threshold	V_{th_rec}	0.5 ×**VPRO**		0.608 ×**VPRO**	V	dominant-to-recessive
Center voltage	V_{BUS_CNT}	0.44 ×**VPRO**	0.5 ×**VPRO**	0.56 ×**VPRO**	V	
Hysteresis	V_{HYS}	0.07 ×**VPRO**		0.219 ×**VPRO**	V	

Table 11-12: LIN Transceiver DC Electrical Characteristics

11.11.3 AC Characteristics

T_J = -40 to 110 °C; 7 V < **VPRO = VPRO_HOLD** < 18 V; **VDDP** = 3.3 V; **VDDU_OUT** connected to **VDDU**; unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Transmitter:						
LIN Slew rate: 20 kbps (**LC.SLEW[1:0]** = 00b) 10.4 kbps (**LC.SLEW[1:0]** = 01b) ECL (**LC.SLEW[1:0]** = 11b) Off (**LC.SLEW[1:0]** = 10b)	$\|SR_f\|$, SR_r	0.5	2.15 1.1 0.05 6.8	1.512	V/µs V/µs V/µs V/µs	(Notes 1, 2) (Note 2) (Note 2) R_{BUS}/C_{BUS}: 1 kΩ/1 nF
Receiver:						
LIN-to-**RXD** propagation delay	t_{rx_pdf}, t_{rx_pdr}			6	µs	(Note 3)
Propagation delay symmetry	t_{rx_sym}	-2		2	µs	(Note 3)

1. For applications implementing high-speed LIN bus communication at the 20 kbps speed mode, SMSC recommends disabling the slew rate control by setting **LC.SLEW[1:0]** = 10b.
2. SR_r assumes external R/C bus loading is not limiting the slew rate.
3. **RXD** load: 20 pF/2.4 kΩ pull-up.

Table 11-13: LIN Transceiver AC Electrical Characteristics

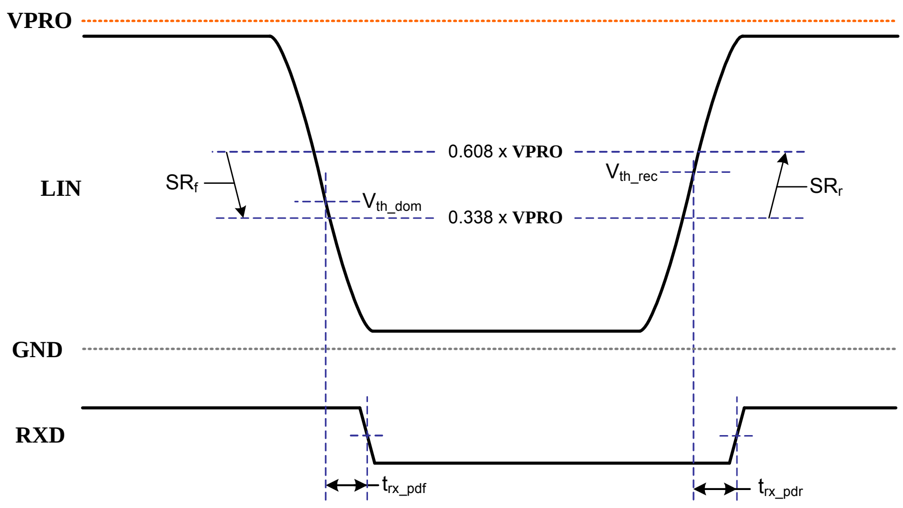


Figure 11-5: LIN RXD Delay and TXD Slew Rate

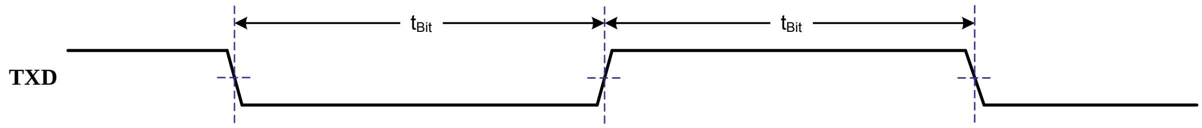
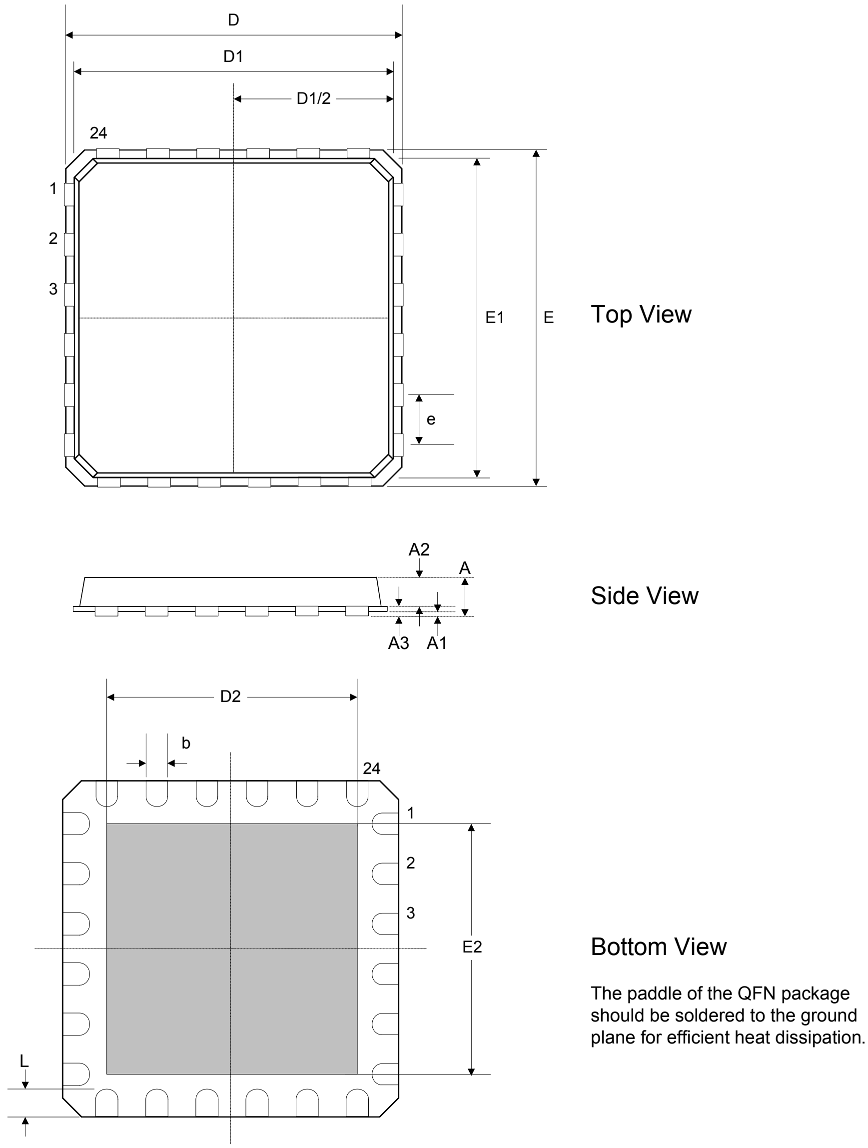


Figure 11-6: LIN TXD Timing

12 Package Outline (QFN24)

MPM85000 is packaged in a 24-pin, QFN, with relevant package specifications provided below. Thermal characteristics of the package are outlined in Table 12-2.



	A	A1	A2	D	D1	D2	E	E1	E2	L	e	b
Min	0.70	0		3.85	3.55	2.40	3.85	3.55	2.40	0.30		0.18
Typ		0.02		4.00		2.50	4.00		2.50		0.50	0.25
Max	1.00	0.05	0.9	4.15	3.95	2.60	4.15	3.95	2.60	0.50		0.30

Table 12-1: Package Outline Dimensions in mm

Parameter *	Symbol	Value	Unit
Typical Junction to Ambient	θ_{JA}	40	°C/W

* Thermal characteristics are applicable to PCBs that adhere to the JEDEC standard (J-STD-020). The package power dissipation specification assumes a recommended thermal via design consisting of four 13 mil vias connected to the ground plane with a 2×2 mm thermal landing.

Table 12-2: Thermal Characteristics

13 Application Information

The MPM85000 is a flexible power management solution which offers many optional features, not all of which are intended for use in any one design. Overall system architectures are described in the *MOST INIC Hardware Concepts Technical Bulletin [1]*. This chapter offers examples of more detailed power management architectures when using the MPM85000 in conjunction with a MOST *Intelligent Network Interface Controller* (INIC) device. For more information on SMSC's INIC devices, refer to the respective INIC documentation *[9, 10]*.

Section 13.1 illustrates a typical communication interface between the MPM85000, a MOST INIC device, and an *External Host Controller* (EHC). The MPM85000 supports all MOST Network speeds (MOST25, MOST50, and MOST150); however, the implementation details may vary across network speed grades. Section 13.2 describes an alternative reset implementation for use when both the INIC and EHC must use the MPM85000 power-on reset.

A typical network configuration and power diagram for each speed grade is provided in Section 13.3. The typical external circuitry required when using the MPM85000 LIN transceiver for either LIN bus communication or MOST ECL communication is shown in Section 13.4. If the MPM85000 is being used to detect the diagnostic *Switch-To-Power* (STP) pulse, a non-standard power supply arrangement is required. STP events are typically only used in systems that do not support LIN/ECL communication. A system power diagram for STP pulse detection is shown in Section 13.5.

Section 13.6 discusses MPM85000 PCB layout guidelines including recommendations for the ePHY network activity detector (**ERXP**/**ERXN**) and the LIN/ECL interface (**LIN**). This section also contains recommendations for the MPM85000 exposed package paddle for effective thermal dissipation.

Although this chapter focuses on configurations used in MOST Network systems, the communication and power supply examples are also suitable for use in non-MOST applications. The *MPM85000 Evaluation Platform User's Manual [11]* provides access to all MPM85000 features (without a MOST Network interface) for use during non-MOST application development or stand-alone LIN testing.

Part numbers listed in the figures are recommendations only; specific parts chosen should be validated for the particular design requirements.

13.1 Communication Interface

Figure 13-1 illustrates a typical MPM85000 communication interface for use with any INIC device. The EHC is assumed to have an internal power-on reset (POR) generator.

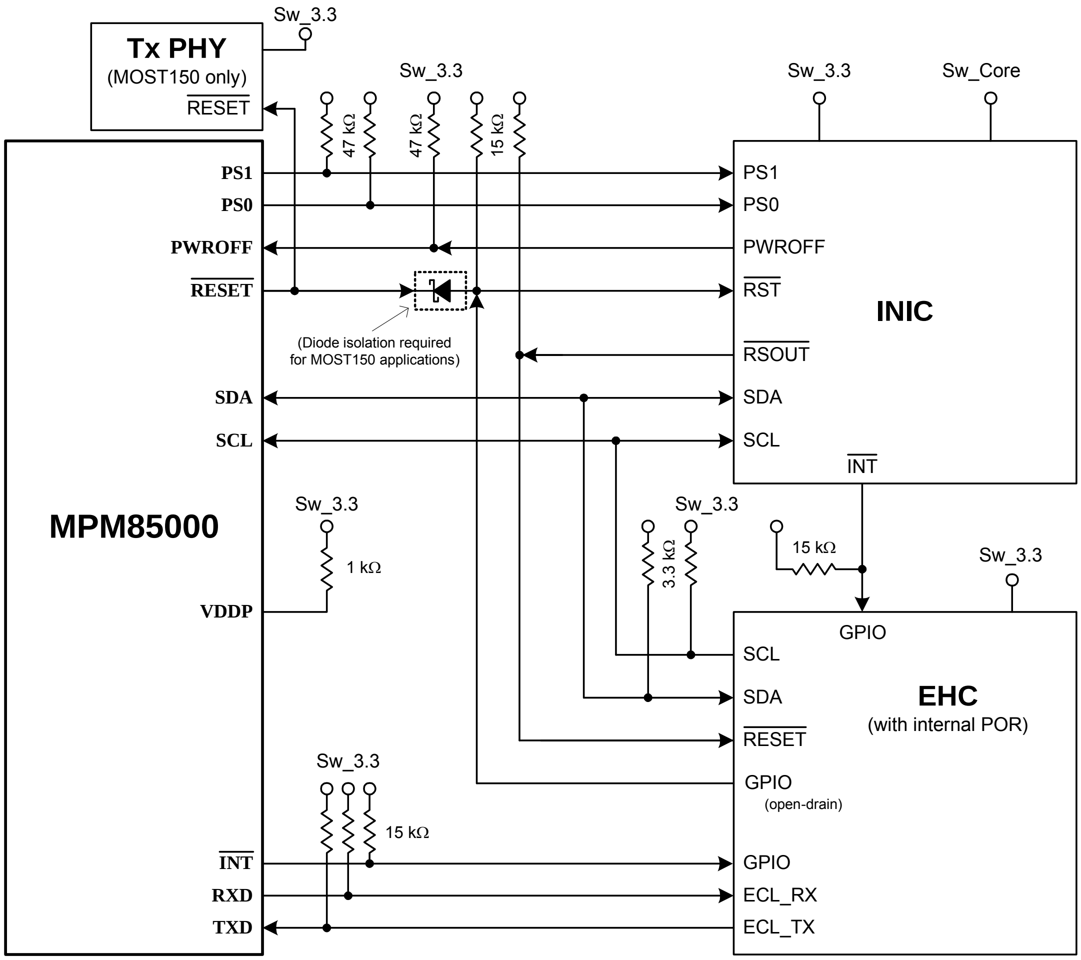


Figure 13-1: MPM85000 Communication Diagram

The Tx PHY for MOST150 systems requires a power-on reset (POR). The MPM85000 reset generator provides the POR for the Tx PHY and the INIC. The EHC has an open-drain GPIO connected to the INIC reset line to support INIC flash memory updates as well as provide an INIC reset for exceptional conditions. Note that diode isolation is used to prevent the EHC from also resetting the Tx PHY, so as not to interfere with MOST Network operation. Figure 13-1 does not depict all the requirements for INIC flashing; see the *INIC Flash Guide Application Note [12]* for more information. The EHC's reset GPIO must be high-impedance during power-up/reset so that an application reset at the EHC does not interfere with MOST Network operation. Since the MPM85000 implements a delay (t_{POFF_DEL}) before responding to rising edges on **PWROFF**, the EHC is not required to keep the MPM85000 in *Active Mode* while issuing a short INIC reset. However, the EHC must keep the MPM85000 in *Active Mode* when updating INIC flash program memory. This is easily accomplished by setting the **OR.HOLD** bit during the INIC flashing process.

In Figure 13-1, the EHC communicates with the MPM85000 (and INIC) over an I^2C bus, as the I^2C master. The MPM85000 contains internal registers which indicate the reason for exiting *Sleep Mode* as well as other status information. These registers are read by the EHC and used to fill in the `NetBlock.DeviceInfo(WakeInfo)` parameters (further described in the *MOST FunctionBlock NetBlock [8]* documentation). The MPM85000 also includes a temperature sensor with programmable interrupt capabilities which may be used to implement the over-temperature management mentioned in Chapter 8.

13.2 EHC POR From MPM85000

In the previous example, the assumption was made that the EHC contains an internal power-on-reset circuit, or that the EHC POR was handled independently from the MOST INIC and the MPM85000. However, if the EHC requires an external POR and operates from the same power supply as the INIC, the MPM85000 reset can be used, as illustrated in Figure 13-2. In this scenario, diode isolation is required so that when either component (INIC or the EHC) drives the reset line of the other device, the driving component does not reset itself.

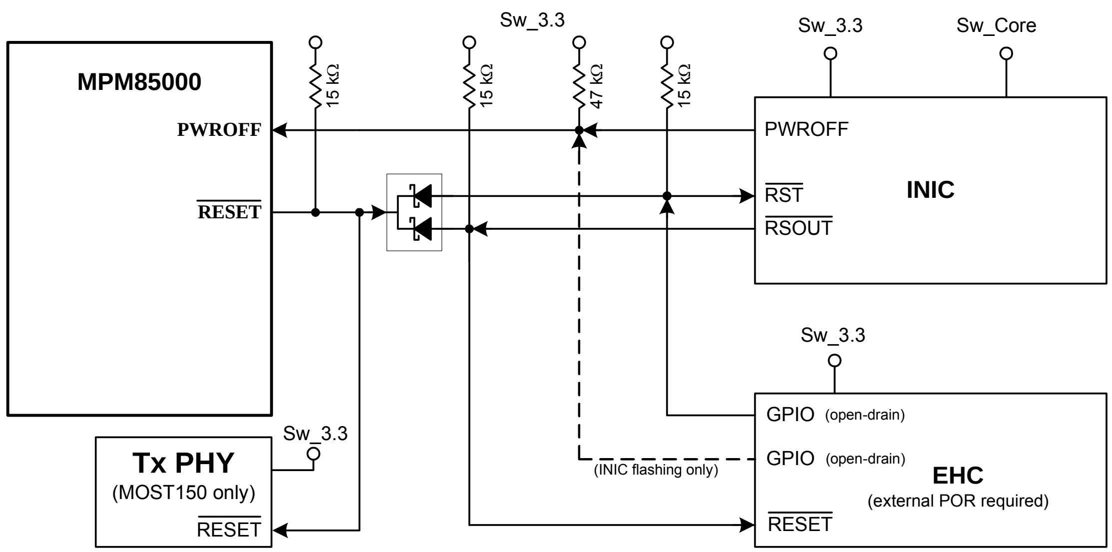


Figure 13-2: EHC Power-On Reset from MPM85000

13.3 Power Supply Arrangements

The power diagrams in this section include additional protection circuitry that provide the MPM85000 with immunity to power supply transients greater than 40 V. If the protected power supply voltage does not exceed the MPM85000 maximum ratings, these extra components can be removed. The configurations shown in this section also assume that *Switch-To-Power* (STP) pulse detection is not used. For ECUs that require STP support, refer to Section 13.5.

13.3.1 MOST150 Network/Power Configuration

Figure 13-3 illustrates the MPM85000 in a MOST150 Network system with an OS81110 INIC device.

The *OS81110 Evaluation Board Hardware Data Sheet [13]* provides a functional ECU to test the MPM85000 capabilities in a MOST150 Network. The board contains component population options to support all the MPM85000 functionality available for use in a MOST150 implementation.

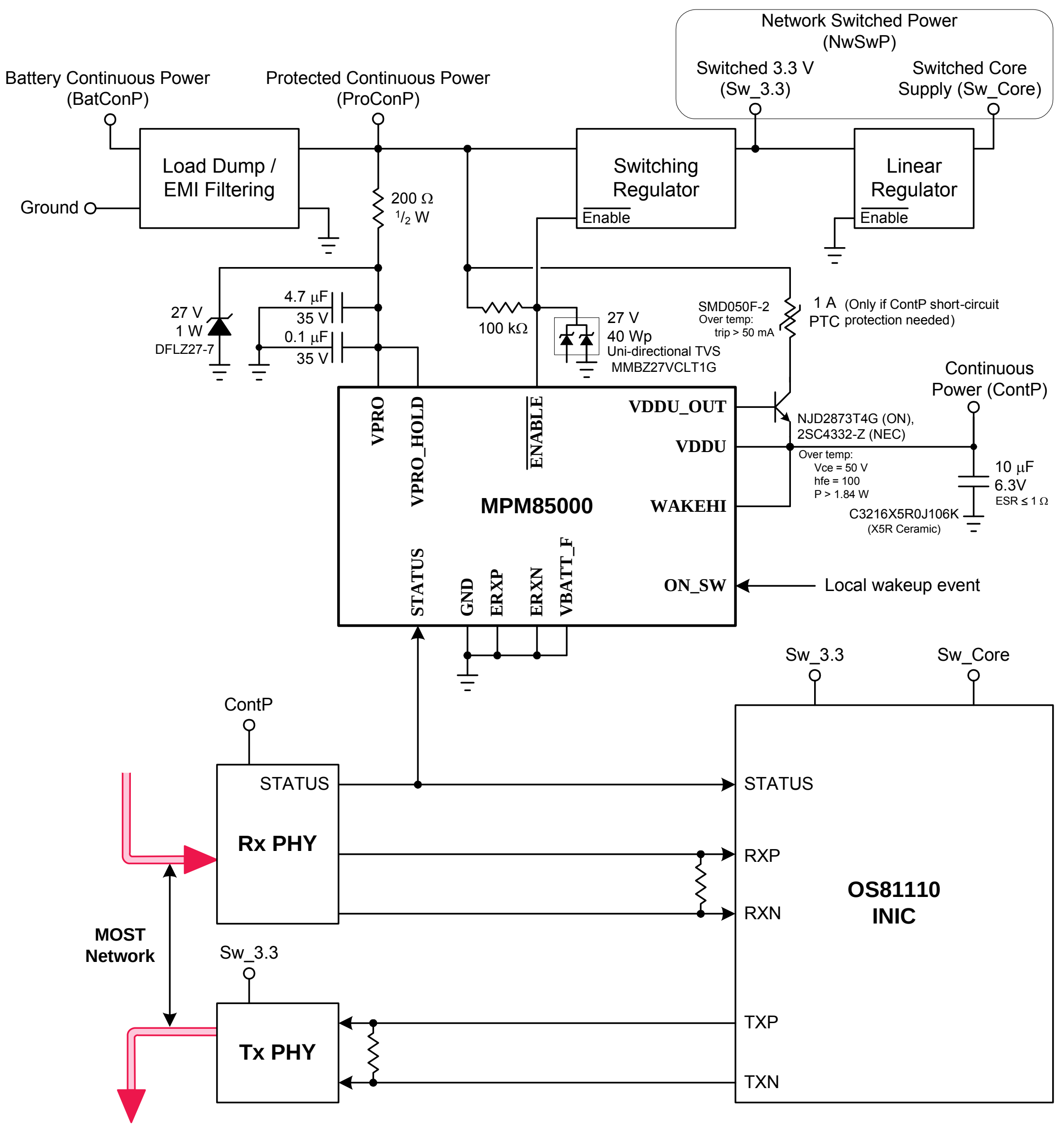


Figure 13-3: MOST150 Power/Network Section

In Figure 13-3 on page 76, the MPM85000 **VDDU** continuous supply powers the Rx PHY in both *Sleep Mode* and *Active Mode*. An external NPN transistor is required due to the *Active Mode* current required by the Rx PHY. The transistor should have a gain of at least 100 and its V_{CE} should be able to withstand the maximum voltage seen at Protected Continuous Power (ProConP). If short-circuit protection is required on the continuous supply, then a series PTC element can be used, as illustrated. The PTC device should be sized not to trip at the maximum *Active Mode* current draw while operating at the maximum temperature. When using the external pass transistor, a 10 µF capacitor with an ESR less than 1 Ω is required.

13.3.2 MOST50 Network/Power Configuration

Figure 13-4 illustrates the MPM85000 in a MOST50 Network circuit with an OS81092 INIC device.

The *OS81092 Evaluation Board Hardware Data Sheet [14]* provides a functional ECU to test the MPM85000 capabilities in a MOST50 Network. The board contains component population options to support all the MPM85000 functionality available for use in a MOST50 implementation.

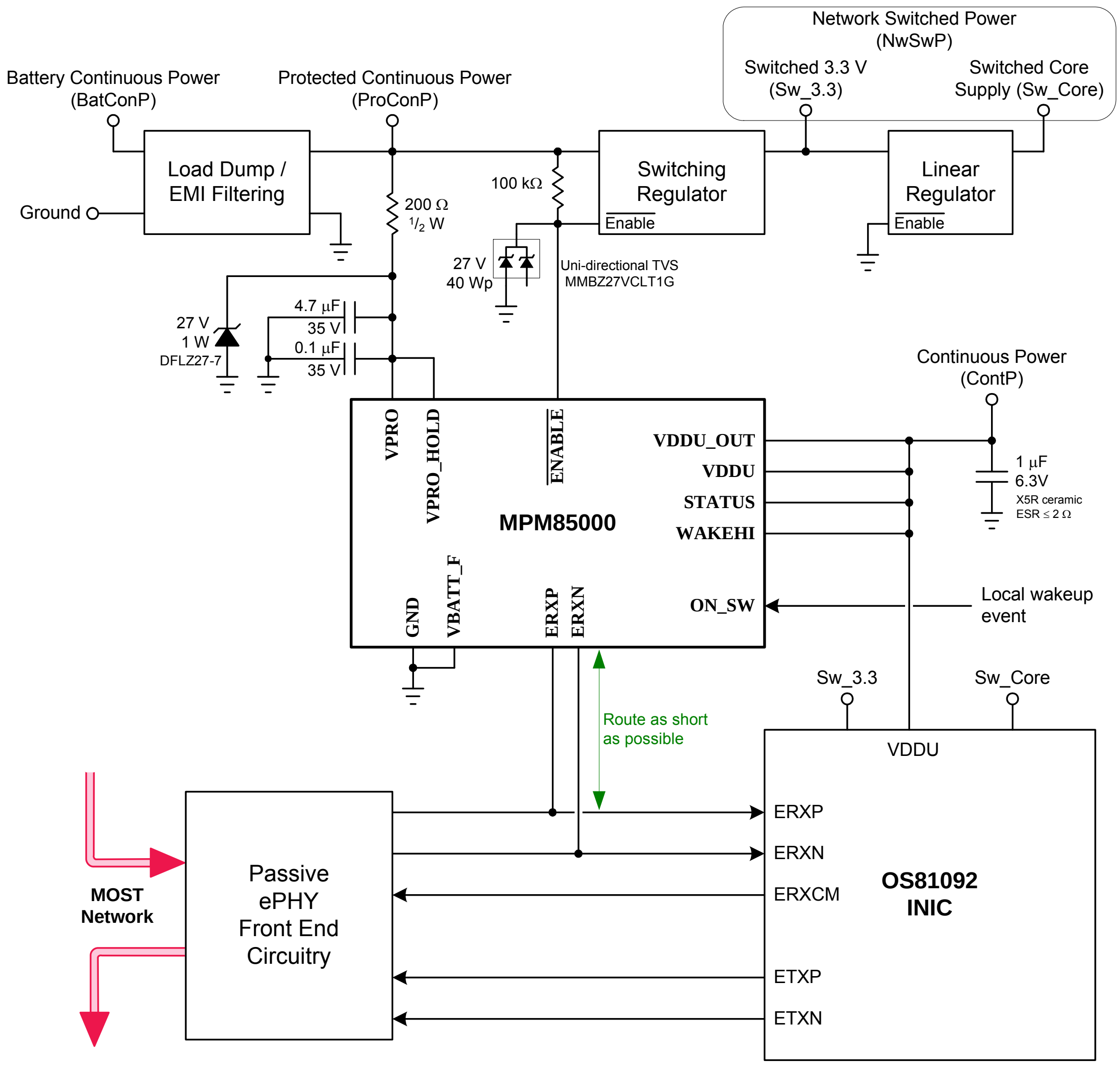


Figure 13-4: MOST50 Power/Network Section

In Figure 13-4 on page 77, the external pass transistor on VDDU can be eliminated since no Rx PHY exists in a MOST50 electrical system, and VDDU is only used to power persistent memory in the OS81092 ROM INIC device. When not using the external transistor, a 1 µF capacitor with an ESR less than 2 Ω is required. The STATUS pin is shown as unused and tied to VDDU; however, it can be used for a local wakeup event, as it provides a faster response time than the ON_SW pin. In addition, the ERXP/ERXN pins are directly connected to the INIC network receive pins to support the ability to wakeup the ECU from electrical network activity (same functionality as provided by the STATUS pin in optical networks).

13.3.3 MOST25 Network/Power Configuration

MOST25 optical systems are similar to MOST150 optical systems. Figure 13-5 illustrates the power connections needed when using the OS81060 ROM INIC device. This connection diagram only differs from the MOST150 version in that the MPM85000 VDDU continuous supply is also connected to the INIC VDDU pin to keep persistent memory powered during in *Sleep Mode*.

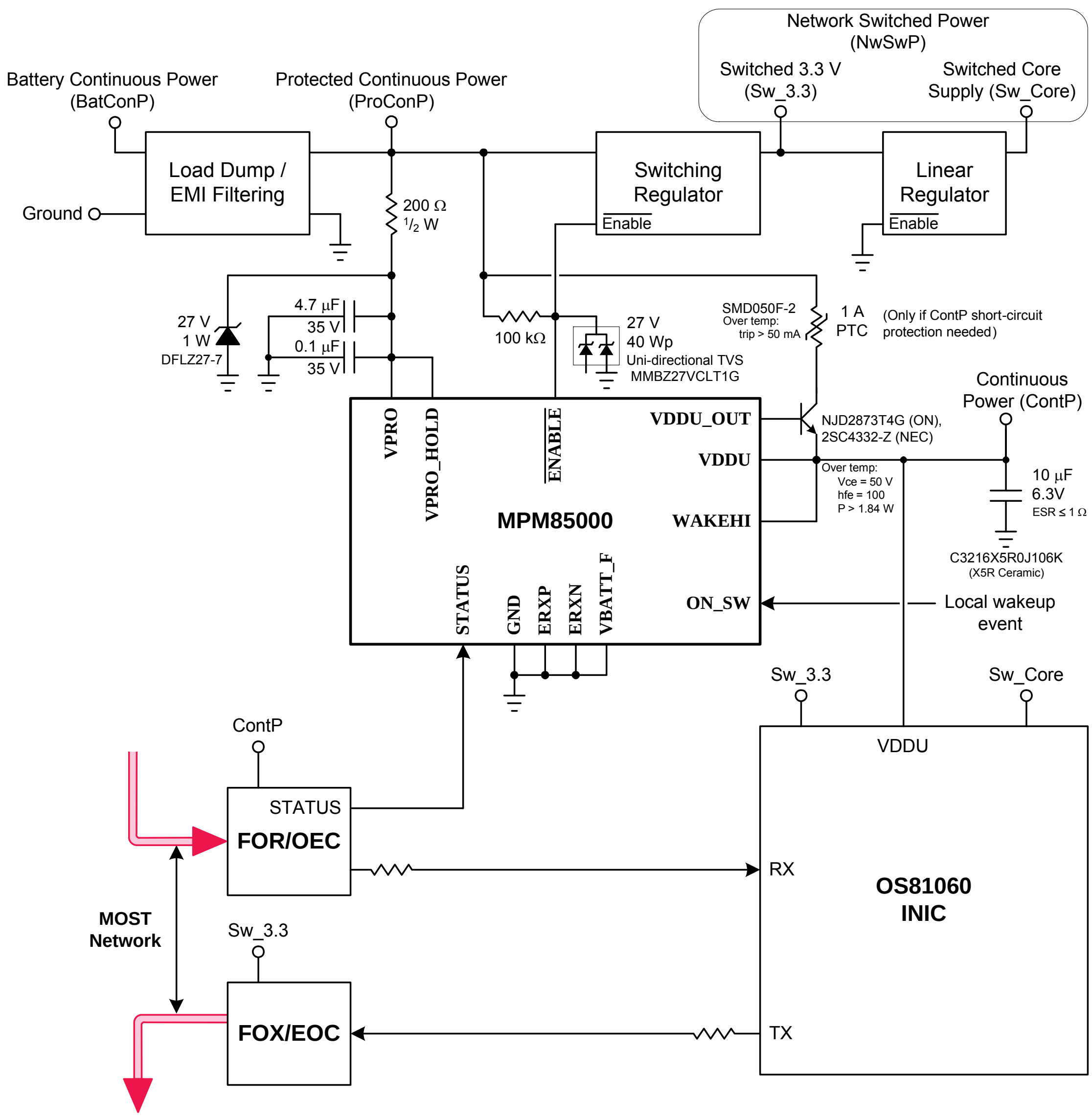


Figure 13-5: MOST25 Power/Network Section

13.4 ECL/LIN Support

The MPM85000 supports both *Local Interconnect Network* (LIN) *[3]* communication and *MOST Electrical Control Line Specification [4]* communication. If LIN/ECL wakeup and communication is not required, the **LIN** pin can be left floating (since it contains an internal pull-up) and the external components can be eliminated. Both LIN and ECL are wired-or'ed lines between all ECUs. In MOST Networks, they are used for diagnostics and electrical network wakeup. Although the hardware interface can be the same between LIN and ECL, MOST ECL is a less complex (and also slower) interface that is suitable for bit-banging by an EHC.

Figure 13-6 illustrates the connections when using LIN/ECL. If the ECU is the LIN master, an external diode and pull-up resistor to protected battery power should be added, as described in the *LIN Specification [3]*. All other nodes do not need these two external components since the MPM85000 contains the slave circuitry internally. Example **LIN** pin input protection circuitry is shown; however, the actual circuitry used in production applications varies depending on the EMI and EMC requirements as well as PCB layout.

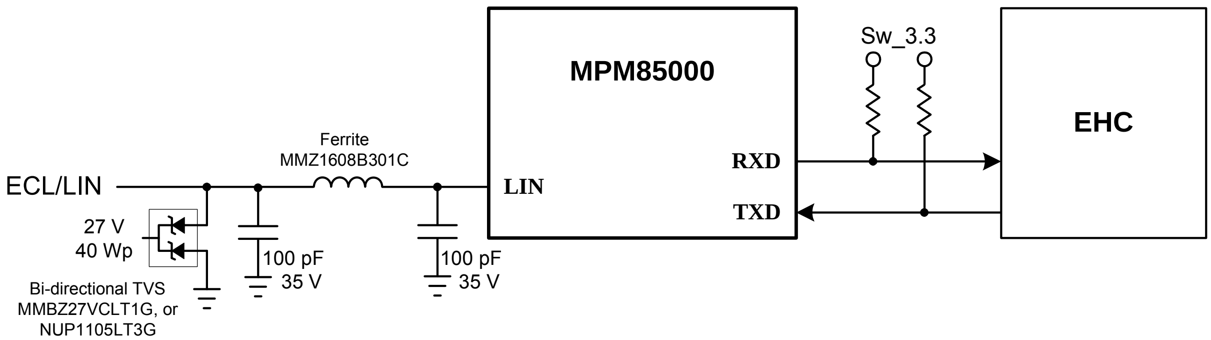


Figure 13-6: ECL/LIN Connections

Figure 13-6 also depicts the EHC using the MPM85000 **RXD** and **TXD** pins which are unidirectional and level-shifted versions of the **LIN** pin. When using the interface for higher speed LIN, these pins are generally connected to an ECU's LIN or UART interface. When using LIN, the **MR.mLIN** mask bit should be set (default) so LIN transitions do not cause extraneous interrupts to the EHC. In addition, the **LC.SLEW[1:0]** bits control the LIN driver slope and should be set, based on the desired LIN speed, to minimize EMI.

When using MOST ECL, the MPM85000 Control Port I^2C interface can be used in lieu of the **RXD** and **TXD** pins, since the ECL data speed is substantially slower than LIN. In this scenario, the EHC can set the register bit **LC.TXD** to drive the **LIN** pin low. The EHC can also read the **LC.RXD** bit to determine the state of the **LIN** pin. When the **MR.mLIN** mask bit is clear, the $\overline{\textbf{INT}}$ pin is asserted whenever the **LIN** pin changes state, eliminating the need for EHC polling. The **LC.SLEW[1:0]** bits can also be set to 11b, which is the longest LIN driver slope (lowest EMI) and is designed specifically for MOST ECL.

13.5 STP Event Detection

In some system designs (generally those without ECL/LIN support), the diagnostic *Switch-To-Power* (STP) pulse can be used to wakeup the ECU from *Sleep Mode*, which initiates ring-break diagnostics (RBD). The MPM85000 supports STP by clearing the **CR.NOSTP** bit, and configuring the power supplies as illustrated in Figure 13-7. In this scenario, the **VBATT_F** pin detects the removal of power for more than three seconds. The **VBATT_F** pin must be connected before the Load Dump circuitry to be able to detect the battery voltage drop. Otherwise, the Load Dump storage capacitors would delay detection until too late. The **VPRO_HOLD** pin is also separated from the **VPRO** pin by a diode and a charge-reserve capacitor, which keeps the MPM85000 powered for over four seconds, even in *Active Mode*. Part numbers in the figure below are only recommendations provided for convenience.

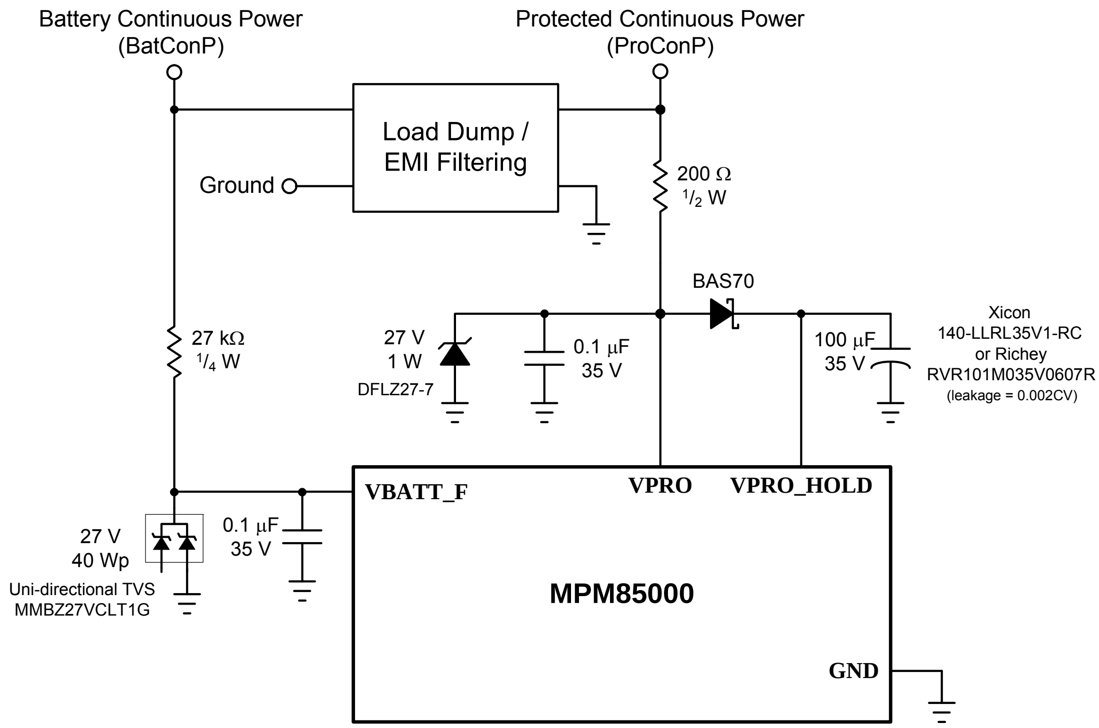


Figure 13-7: STP Power Supply Arrangement

13.6 Layout Guidelines

13.6.1 MOST50 Network Activity Detection

When the MPM85000 ePHY activity detector is used to implement network activity wakeup functionality, the MPM85000 **ERXP** and **ERXN** pins should connect to the network at MOST50 specification point four (also known as SP4E; see the *MOST Specification of Electrical Physical Layer [7]* for more information). SP4E exists between the INIC/RX termination and the isolation transformer/RX filtering components.

Figure 13-8 shows a typical layout with the MPM85000 connected to the MOST50 Network at SP4E. When the MPM85000 is attached to the ePHY receiver circuitry, stub lengths on the differential transmission line must be minimized. Two 0 Ω resistors (R1 and R2) allow the MPM85000 to be disconnected (without leaving stubs on the receive-side transmission line) for flexibility during testing. R2 also allows the **ERXN** signal to jump over the **ERXP** signal without using vias to route the signal on a different layer. This approach is consistent with the best practice PCB design techniques of routing high-speed transmission lines on a single layer to avoid impedance bumps and provide an uninterrupted path for return currents.

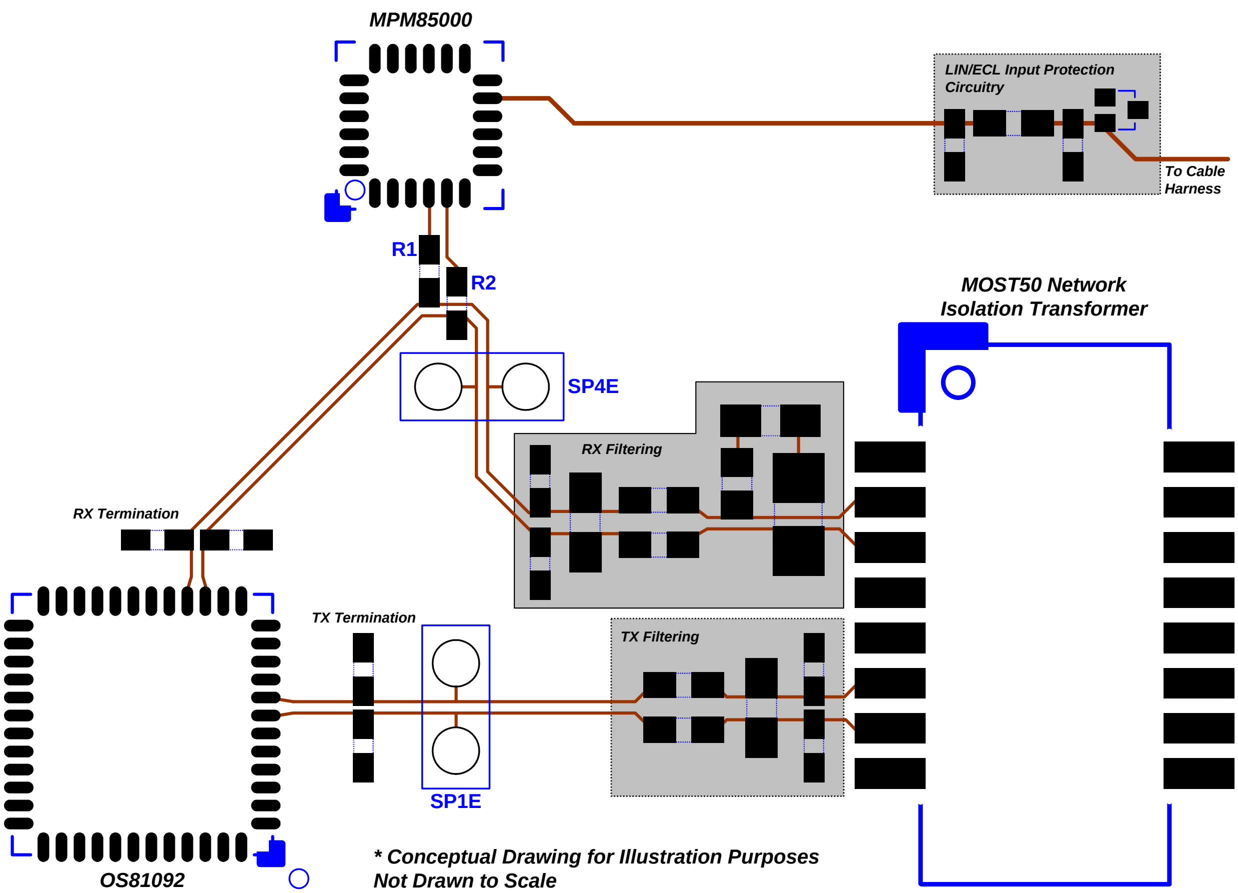


Figure 13-8: ePHY Activity Detector Placement Diagram

13.6.2 LIN/ECL Input Protection

Figure 13-8 on page 81 also includes the protection circuitry for the **LIN** pin (further described in Section 13.4). The MPM85000 LIN/ECL interface is typically connected to the cable harness and then tied to other network nodes to permit electrical signalling between devices. The input protection circuitry should be placed as close as possible to the cable harness to prevent external interference and transient events from entering the system.

13.6.3 Thermal Considerations

The paddle of the MPM85000 QFN package should be soldered to the thermal land (thermal pad) for efficient heat dissipation. The thermal pad should measure 2×2 mm and be connected to the internal ground plane(s) of the board using heat tubes (vias without thermal reliefs). At least four heat tubes are recommended, with a drill hole size no larger than 0.33 mm (13 mils).

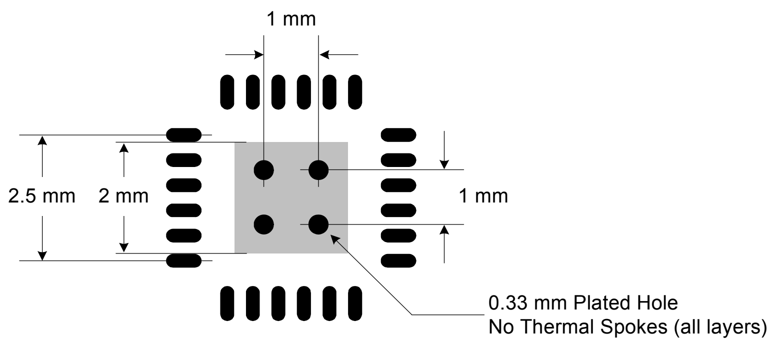


Figure 13-9: Example Layout - Drill Holes

Appendix A: Register Summary

Table A-1 lists all MPM85000 registers accessible via the I^2C Control Port.

Addr	Name	B7	B6	B5	B4	B3	B2	B1	B0	Register Name	Pg.
		Control/Status Registers:									
00h	IR			iEPHY	iONSW	iLIN	iPOR	iSTATUS	iVOLT	Interrupt Register	47
01h	SR		LINPSE		iTEMP		SV	CV	LV	Status Register	48
02h	LSR			RESET	EPHY	ONSW	LIN	STATUS		Line Status Register	49
03h	RD						DELAY2	DELAY1	DELAY0	Reset Delay Register	50
04h	VCT			SVTH1	SVTH0	CVTH1	CVTH0	LVTH1	LVTH0	VPRO Comparator Threshold Register	51
05h	LC	TEMP-ERR	PSD	NOMAX	SLEW1	SLEW0	TOERR	RXD	TXD	LIN Control Register	52
06h	OR		oEPHY	oLIN	oONSW	oSTATUS	HOLD			Override Register	53
08h	CR	$\overline{\text{WAKECV}}$	NOSTP	WAKESV	PDEPHY		EDELAY2	EDELAY1	EDELAY0	Configuration Register	54
09h	MR		mLIN		mONSW	mSTATUS	mEPHY	mTEMP	mVOLT	Mask Register	55
0Ah	TEMPHI	TEMP10	TEMP9	TEMP8	TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	Temperature High Value Register	56
0Bh	TEMPLO	TEMP2	TEMP1	TEMP0						Temperature Low Value Register	56
0Ch	TLIMHI		TLHI6	TLHI5	TLHI4	TLHI3	TLHI2	TLHI1	TLHI0	Temperature Limit High Register	57
0Dh	TLIMLO	TLLO7	TLLO6	TLLO5	TLLO4	TLLO3	TLLO2	TLLO1	TLLO0	Temperature Limit Low Register	57
0Eh	THHYS				HYS4	HYS3	HYS2	HYS1	HYS0	Temperature High Hysteresis Register	57
0Fh	IWE			wEPHY	wONSW	wLIN	wPOR	wSTATUS		Initial Wakeup Event Register	58
2Fh	OCS						CELL2	CELL1	CELL0	OTP Cell Select Register	60
38h	OTPC	UPDATE								OTP Control Register	60
39h	OTPP					PROG3	PROG2	PROG1	PROG0	OTP Programming Register	60
		Data Storage Space:									
10h	DS0									Data Storage Register 0	59
11h	DS1									Data Storage Register 1	
	…										
1Fh	DSF									Data Storage Register F	
		OTP Data Space									
30h	OD0									OTP Data Register 0	59
31h	OD1									OTP Data Register 1	
	…										
37h	OD7									OTP Data Register 7	
		Product Information Registers:									
FCh	PF								WAKEHI	Product Features Register	61
FDh	PID	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	Product ID Register	61
FEh	MID	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	Manufacturer ID Register	61
FFh	REV	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	Revision Register	61

Table A-1: Register Summary

Appendix B: References

Documents listed below and referenced within this publication are current as of the release of this publication and may have been reissued with more current information. To obtain the latest releases of SMSC documentation please visit the SMSC website. Please note, some SMSC documentation may require approval from SMSC. SMSC contact information can be found at www.smsc-ais.com/contact.

All non-SMSC documentation should be retrieved from the applicable website locations listed below. SMSC is not responsible for the update, maintenance or distribution of non-SMSC documentation.

Because the Internet is a constantly changing environment, all Internet links mentioned below and throughout this document are subject to change without notice.

[1] MOST INIC Hardware Concepts Technical Bulletin
TB0520AN1: Sep.2009. SMSC. www.smsc-ais.com.

[2] MOST Specification 3.0
Rev. 3.0 E2: Jul. 2010. MOST Cooperation. www.mostcooperation.com.

[3] Local Interconnect Network (LIN) Specification Package
Revision 2.1: 2008. LIN Consortium. www.lin-subbus.de.

[4] Electrical Control Line Specification
Revision 1.1: Nov. 2010. MOST Cooperation. www.mostcooperation.com.

[5] I^{2}C-Bus Specification
NXP (formerly a division of Philips). www.nxp.com.

[6] MOST Specification 2.5
Rev. 2.5: Oct. 2006. MOST Cooperation. www.mostcooperation.com.

[7] MOST Specification of Electrical Physical Layer
MOST Cooperation. www.mostcooperation.com.

[8] MOST FunctionBlock NetBlock
Rev 3.0.2: Mar. 2011. MOST Cooperation. www.mostcooperation.com.

[9] INIC Hardware Data Sheets
SMSC. www.smsc-ais.com.

MOST25: OS81050 MOST25 INIC Data Sheet (Flash). DS81050AP11: Oct. 2010.
OS81060 MOST25 INIC Data Sheet (ROM). DS81060AP4: Nov. 2010.

MOST50 OS81082 MOST50 INIC Hardware Data Sheet (Flash). DS81082FP5: Feb. 2011.
OS81092 MOST50 INIC Hardware Data Sheet (ROM). DS81092AP3: Apr. 2011.

MOST150: OS81110 MOST150 INIC Hardware Data Sheet (Flash). DS81110AP5: Nov. 2010

[10] INIC API User's Manuals
SMSC. www.smsc-ais.com.

MOST25: OS8105x/OS8106x MOST25 INIC API User's Manual. Rev 1.8.2-5: Sep. 2010

MOST50: OS81082 MOST50 INIC API User's Manual. Rev 1.6.0-5: June 2009
OS81092 MOST50 INIC API User's Manual. Rev 1.3.0-1: Dec. 2010

MOST150: OS81110 MOST150 INIC API User's Manual. Rev 1.8.1-1: Nov. 2010

[11] MPM85000 Evaluation Platform User's Manual
V1.0.0-1: Dec. 2009. SMSC. www.smsc-ais.com.

[12] INIC Flash Guide Application Note
V2.0.x-3, Sep. 2007. SMSC. www.smsc-ais.com.

[13] OS81110 Evaluation Board Hardware Data Sheet
DBH81110DS1B1: Mar. 2010. SMSC. www.smsc-ais.com.

[14] OS81092 Evaluation Board Hardware Data Sheet
DBH81092DS1B1: Dec. 2009. SMSC. www.smsc-ais.com.

Appendix C: Revision History

The most extensive and pertinent application changes are listed in Table C-1, although various other differences may be observed between document revisions.

Location	Description of Changes
DS85000AP4: Dec. 2012	
General	- Added Microchip logo and branding
Ordering Information	- Updated *Ordering Information* table to correctly indicate valid MPM85000 order numbers
Pinout	- Corrected termination instructions for **VDDP** and **$\overline{\text{RESET}}$** pins for applications not utilizing the reset generator
Control Port	- Updated contents of the *Revision Register* (REV) for Revision E silicon - Added usage recommendations for **LC.SLEW[1:0]** to the *LIN Control Register* (LC) section

Electrical Specifications	- Updated the *Absolute Maximum Ratings* section, as follows:
	  - Changed the minimum input voltages for **VBATT_F**, **VPRO**, and **$\overline{\text{ENABLE}}$**
	  - Added minimum and maximum voltage specifications for **VDDU**
	  - Changed the maximum current out of **VBATT_F**
	- Added minimum and maximum voltage specifications for **LIN** and **VDDU** to the *Guaranteed Operationg Conditions* section
	- Updated typical values for $t_{PS\_HOLDSTP}$, t_{POFF_DEL}, t_{RST_POFF} and t_{WACK} in the *AC Characteristics* section
	- Updated the *DC Characteristics* section, as follows:
	  - Changed maximum Active Mode Current for **VBATT_F**
	  - Combined **VPRO** and **VPRO_HOLD** operating current specifications
	- Updated the *Activity Detectors* section as follows:
	  - Updated the typical **ERXP/ERXN** input capacitance specification
	  - Updated the maximum **ERXP/ERXN** differential activity specification
	  - Updated the typical **LIN** wakeup delay specification
	  - Updated the **ON_SW** pull-up resistor typical value
	- Removed the maximum accuracy specification from the *Temperature Sensor* section
	- Updated the *Reset Generator* section, as follows:
	  - Updated the typical values for V_{RST_FALL}, V_{RST_HYST}, t_{RST_FALL} and t_{RST_MIN}
	  - Updated the minimum **VDDP** dropout time (t_{RST_MIN}) specification
	- Updated the *MicroPower Regulator* section, as follows:
	  - Updated minimum output current specifications
	  - Updated short-circuit current specifications
	  - Removed typical operating curve for output current
	Updated the *Control Port* section as follows:
	  - Updated the typical **SDA/SCL/$\overline{\text{INT}}$** input capacitance and hysteresis specifications
	  - Removed spike suppression, capacitive load, and minimum rise/fall time specifications
	- Updated the *LIN Transceiver* section, as follows:
	  - Updated the typical value for short-to-power detection
	  - Updated the typical values for **VPRO** pull-up resistor
	  - Updated input levels, thresholds, center voltage, and hysteresis values for LIN Receiver
	  - Updated LIN Transmitter slew rates; added recommended usage note for 20 kbps mode

DS85000AP3: Sep. 2011	
General	- Added SMSC TrueAuto Quality marker and automotive quality process overview - General rewrites throughout document for consistency and clarity
Pinout	- Updated all pin descriptions to better describe recommended use-cases - Added termination guidelines for unused pins

Table C-1: Data Sheet Revision Summary

Location	Description of Changes
Voltage Monitors	- Renamed *Allowed Operating Region* and *Allowed Wake Region* (both referred to as U_{Active}) to *Allowed Wakeup Range* (now referred to as $V_{WakeupRange}$)
Reset Generator and VDDP	- Corrected the action taken for the **LC.TXD** register bit when **$\overline{\text{RESET}}$** is driven low
Control Port	- Clarified that all registers retain their values through *Sleep Mode* cycles - Added LIN transceiver short-to-power error (**SR.LINPSE**) to list of interrupts in Table 10-1 - Changed minimum **RD.DELAY[2:0]** and **CR.EDLAY[2:0]** to 1.2 ms - Corrected the V_{STP_HI} configuration information in the VCT register section - Clarified requirements for clearing interrupt conditions - Added missing overbar to **CR.$\overline{\text{WAKECV}}$** register bit and clarified functionality description
Electrical Characteristics	- Updated *Absolute Maximum Ratings* section as follows: - Added minimum power supply ramp rate specification - Added minimum series resistor value requirement for **VBATT_F** - Removed explicit voltage ratings for **SCL**/**SDA** (now included with "all other input pins") - Updated *Guaranteed Operating Conditions* section as follows: - Updated maximum Junction Temperature (T_J) specification - Removed Ambient Temperature (T_A) specification - Changed minimum voltage specifications for **VPRO** and **VPRO_HOLD** pins - Removed explicit voltage ratings for **SCL**/**SDA** (now included with "all other input pins") - Added Note 1 defining temperature range for OTP writes - Updated *DC Characteristics* section as follows: - Added Note 1 describing pull-up resistor value requirements on **$\overline{\text{ENABLE}}$** - Updated various specficiations for *Active Mode* and *Sleep Mode* supply currents - Removed the I_{SL_VPRO} specification for the LIN bus dominant state (error condition) - Updated *Sleep Mode* current test conditions (added Note 5) - Updated *Activity Detectors* section as follows: - Updated minimum differential voltage level (V_{ePHY_DIFF}) for **ERXP**/**ERXN** activity - Updated typical t_{STAT_ACT}, t_{STAT_INACT}, t_{ePHY_ACT}, t_{ePHY_INACT}, t_{LIN_ACT}, and t_{LIN_INACT} - Updated the *Temperature Sensor* section as follows: - Updated **VPRO** and **VPRO_HOLD** voltage range - Updated typical temperature accuracy specification - Updated the *Voltage Monitors* section as follows: - Updated hysteresis specifications (V_{Hys_Super}, $V_{Hys\_Critical}$, V_{Hys_Low}, and V_{STP_Hys}) - Updated the STP Rising Edge Threshold (V_{STP_HI}) specifications - Updated the typical **$\overline{\text{RESET}}$** pin hysteresis (V_{RST_HYS}) specification - Updated the *MicroPower Regulator* section as follows: - Updated test conditions, minimum value, and removed typical value for I_{LOAD} - Updated test conditions for I_{SHORT} - Updated the *Control Port* section as follows: - Updated minimum data hold time ($t_{HD:DAT}$) specification - Removed maximum data setup and hold time ($t_{SU:DAT}$ and $t_{HD:DAT}$) specifications - Updated the *LIN Transceiver* section as follows: - Updated **VPRO** and **VPRO_HOLD** voltage range for Table 11-11 and Table 11-12 - Updated the minimum $I_{BUS\_NO\_GND}$ specification - Updated the maximum V_{BUSdom_DRV} specification - Added typical R_{SLAVE} specification for *Sleep Mode* (in lieu of $I_{BUS\_SL\_dom}$) - Updated the minimum I_{BUS_LIM} specification - Removed duty cycle specifications (D1, D2, D3 and D4) from *AC Characteristics* - Updated **LIN**-to-**RXD** propagation delays (t_{rx_pdf} and t_{rx_pdr}) and symmetry (t_{rx_sym})
Application Information	- Restructured chapter for clarity and to provide additional application information, as needed - Added PCB layout guidelines section

Table C-1: Data Sheet Revision Summary (Continued)

Location	Description of Changes
DS85000AP2: Nov. 2009	
	- Complete data sheet rewrite and reformat. Updated to match Revision C silicon
Revision 1.89: Feb. 2009	
	- Preliminary release of the data sheet

Table C-1: Data Sheet Revision Summary (Continued)

Appendix D: List of Tables

Appendix E: List of Figures