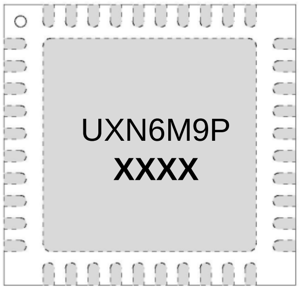
# 9 GHz Divide-by-8 to 511
# Programmable Integer Divider

## Features
- Wide Operating Range: DC-9 GHz
- Contiguous Divide Ratios: 8 to 511
- Large Output Swings: >1 Vpp/side
- Single-Ended or Differential Drive
- Size: 6 mm x 6 mm
- Parallel Control Lines
- Low Power Consumption

## Description
The UXN6M9P is a highly programmable integer divider covering all integer divide ratios between 8 and 511. The device features single-ended or differential inputs and outputs. Parallel control inputs are CMOS and LVTTL compatible for ease of system integration. The UXN6M9P is packaged in a 40-pin, 6 mm x 6 mm leadless plastic surface mount package.

## Application
The UXN6M9P can be used as a low power, general purpose, highly configurable, divider in a variety of high frequency synthesizer applications. Fast switching combined with a wide range of divide ratios make the UXN6M9P an excellent choice for programmable frequency generation.

## Pad Metallization
The QFN package pad metallization consists of a 300-800 micro-inch (typical thickness 435 micro-inch or 11.04 µm) 100% matte Sn plate. The plating covers a Cu (C194) leadframe. The packages are manufactured with a >1hr 150 ºC annealing/heat treating process, and the matte (non-glossy) plating, specifically to mitigate tin whisker growth.

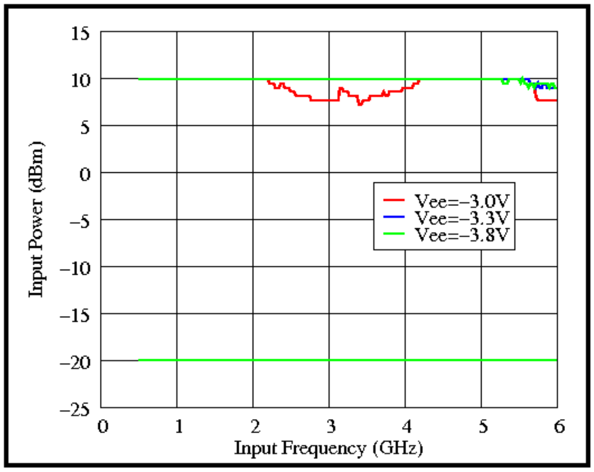



**Key Specifications (T = 25˚C):**
Vee = -3.3 V, Iee = 140 mA, Zi = 50 Ω, Zo=100 Ω

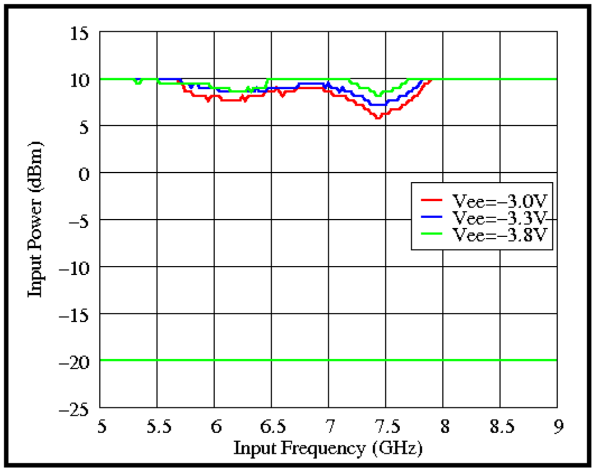
| Parameter | Description | Min | Typ | Max |
|---|---|---|---|---|
| Fin (GHz) | Input Frequency | DC[1] | - | 9[2] |
| Pin (dBm) | Input Power | -15 | 0 | +5[3] |
| Pout (dBm) | Output Power | - | +4 | - |
| PDC (mW) | DC Power Dissipation | - | 460 | - |
| Vee (V) | Negative DC Supply | -3 | -3.3 | -3.6 |
| θjc (ºC/W) | Junction-Case Thermal Resistance | - | 34 | - |

*[1] Low frequency limit dependent on input edge speed*
*[2] Use FRS to extend frequency range beyond 6 GHz. (see page 10)*
*[3] Operating Temperature = 25 ºC*

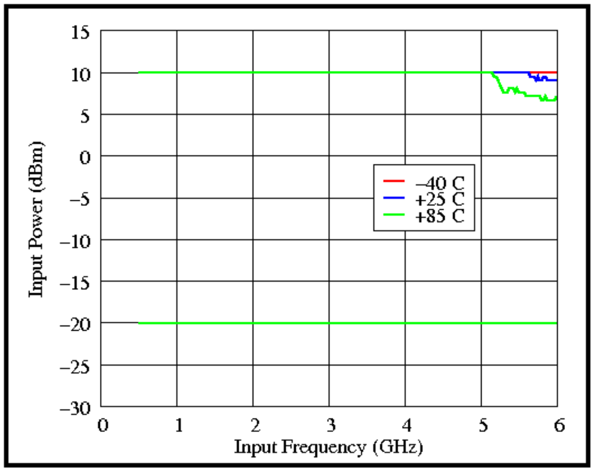
# Typical Performance



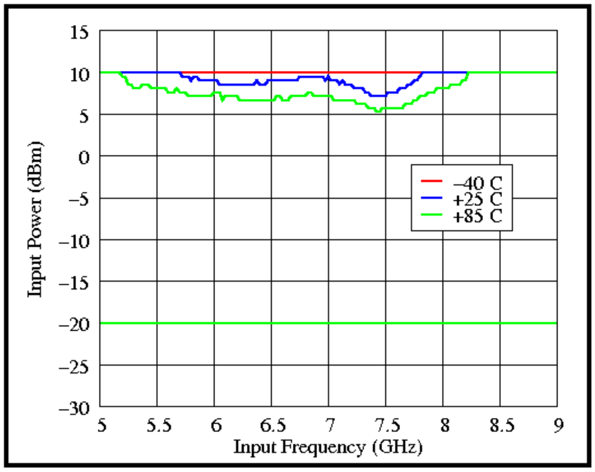

*Min/Max Single-Ended Input Power, INP**
*Input Sensitivity, T=25º C, Divide-by-10, FRS=0*



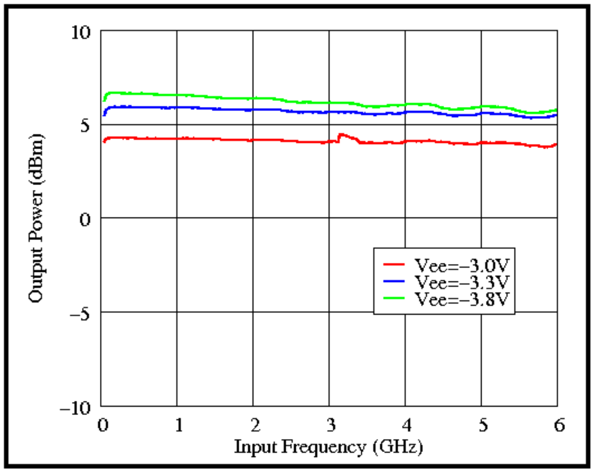

*Min/Max Single-Ended Input Power, INP**
*Input Sensitivity, T=25º C, Divide-by-10, FRS=1*



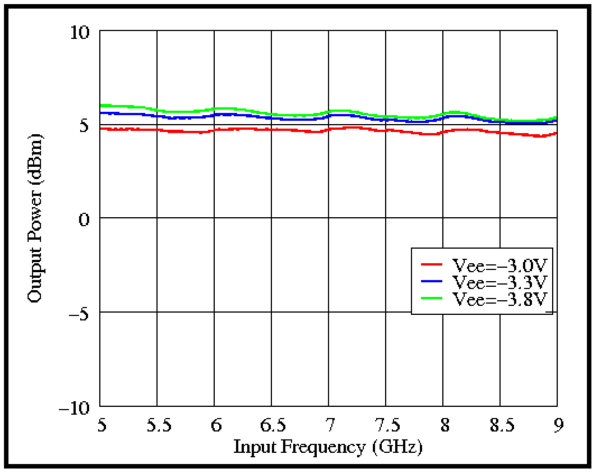

*Min/Max Single-Ended Input Power, INP**
*Input Sensitivity, -3.3 V, Divide-by-10, FRS=0*




*Min/Max Single-Ended Input Power, INP**
*Input Sensitivity, -3.3 V, Divide-by-10, FRS=1*

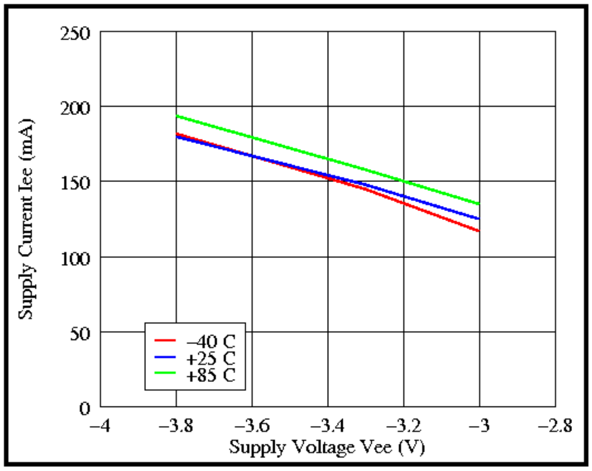



*Output Power*

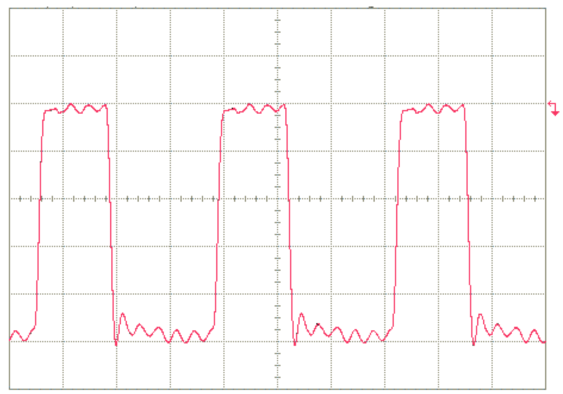



*Output Power*

# Typical Performance

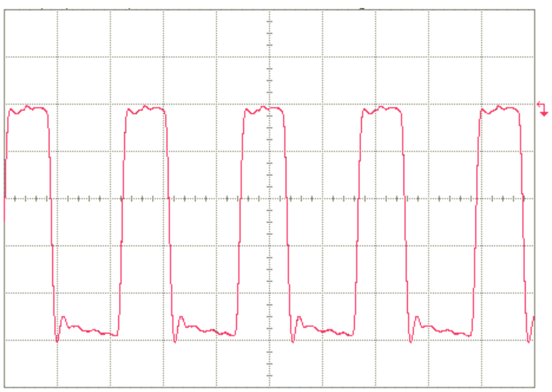



*Min/Max Single-Ended Input Power, INP**
*Input Sensitivity, T=25º C, Divide-by-10, FRS=0*



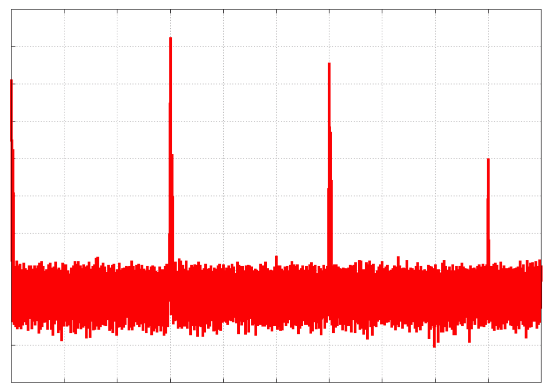
*500 ps/DIV, 200 mV/DIV*

*Waveform, Static Divide-by-10 Configuration*
*Input Freq = 6 GHz, FRS=0*



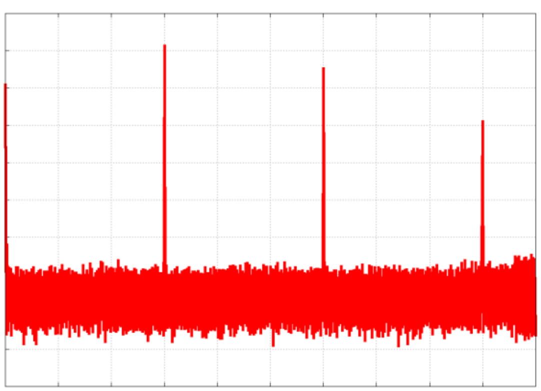
*500 ps/DIV, 200 mV/DIV*

*Waveform, Static Divide-by-10 Configuration*
*Input Freq = 9 GHz, FRS=1*



*10dB/DIV, Center=1GHz, Span=2GHz*

*Spectrum, Static Divide-by-10 Configuration*
*Input Freq = 6 GHz, FRS=0*



*10dB/DIV, Center=1.5GHz, Span=3GHz*

*Spectrum, Static Divide-by-10 Configuration*
*Input Freq = 9 GHz, FRS=1*

# Functional Block Diagram

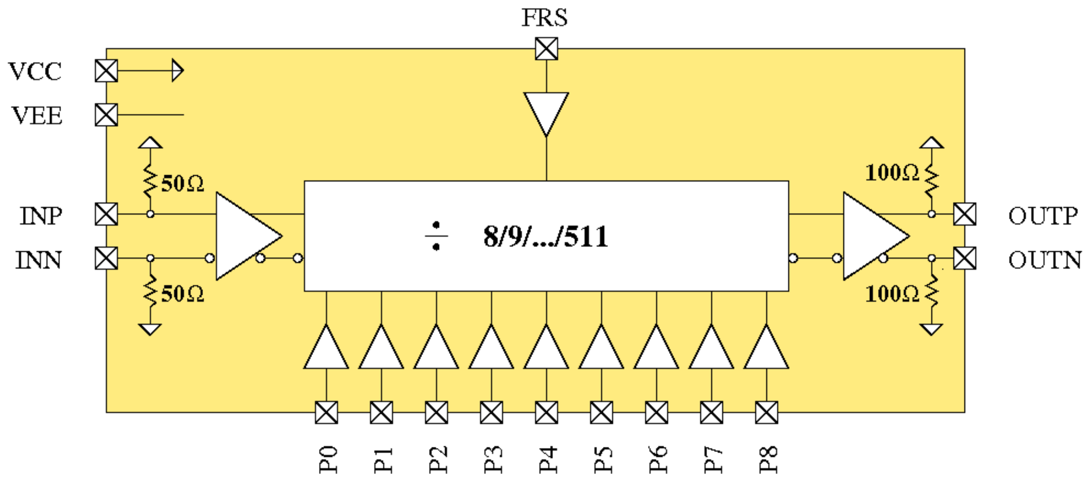



**Table 1: Pin Description**

| Port Name | Description | Notes |
|---|---|---|
| INP | Divider Input, Positive Terminal | CML signal levels |
| INN | Divider Input, Negative Terminal | CML signal levels |
| OUTP | Divider Output, Positive Terminal | CML signal levels |
| OUTN | Divider Output, Negative Terminal | CML signal levels |
| P0-P8 | Divider Modulus Control (P8=MSB) | CMOS levels, see Equation 1, defaults to logic 0 |
| FRS | Frequency Range Selector | CMOS levels, defaults to logic 0, see page 9 |
| VCC | RF & DC Ground | Positive Supply Voltage |
| VEE | -3.3 V @ 140 mA | Negative Supply Voltage |

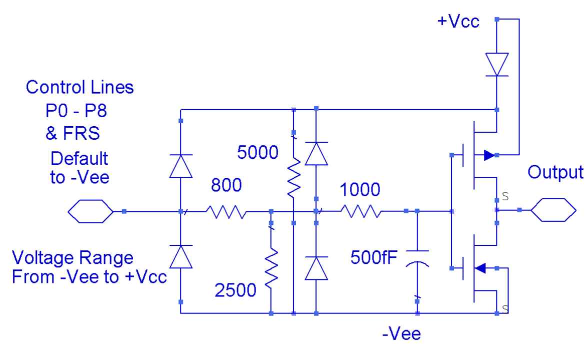
## Equation 3:

$$\text{Divider Modulus} = N = P_0 \cdot 2^0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \ldots + P_8 \cdot 2^8 \qquad \text{for } 8 \leq N \leq 511$$

**Table 2: CMOS Levels for control line P0-P8**

| Logic Level | Minimum | Typical | Maximum |
|---|---|---|---|
| 1 (High) | Vcc-1.25 V | Vcc | Vcc |
| 0 (Low) | Vee | Vee | Vee+1.25 V |

**Simplified Control Logic Schematic**



# Application Notes

## Low Frequency Operation:

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O’s) is determined by the lowest frequency the IC will be operated at.

$$C \gg \frac{1}{2 \cdot \pi \cdot 50\Omega \cdot f_{lowest}}$$

For example to use the device below 30 kHz, coupling capacitors should be larger than 0.1 µF.

## IC Assembly:

The device is designed to operate with either single-ended or differential inputs. Figures 1, 2 & 3 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside paddle of the QFN package should be connected to a good thermal heat sink.

All RF I/O’s are connected to Vcc through on-chip termination resistors. This implies that when Vcc is not DC grounded (as in the case of positive supply), the RF inputs and outputs should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

## ESD Sensitivity:

Although SiGe IC’s have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling.

Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400 V through a human body model (HBM) power limiting impedance.

**Table 3: Negative CML Logic Levels for DC Coupling (T=25˚C) Assuming 50Ω terminations at inputs and outputs**

| Parameter | | | Minimum | Typical | Maximum |
|---|---|---|---|---|---|
| Input | Differential | Logic $Input_{high}$ | Vcc | Vcc | Vcc |
| | | Logic $Input_{low}$ | Vcc - 0.05 V | Vcc - 0.3 V | Vcc - 1 V |
| | Single | Logic $Input_{high}$ | Vcc + 0.05 V | Vcc + 0.3 V | Vcc + 1 V |
| | | Logic $Input_{low}$ | Vcc - 0.05 V | Vcc - 0.3 V | Vcc - 1 V |
| Output | Differential & Single | Logic $Input_{high}$ | Vcc | Vcc | Vcc |
| | | Logic $Input_{low}$ | Vcc - 0.2 V | Vcc - 0.3 V | Vcc - 1 V |

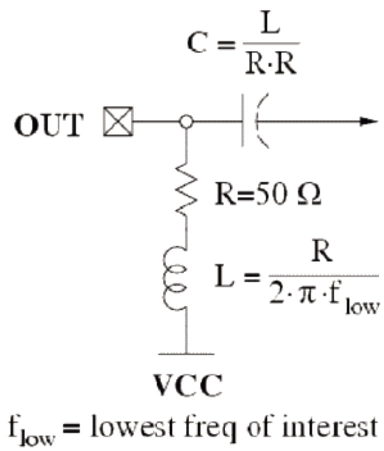
## Differential vs. Single-Ended:

The UXN6M9P is fully differential to maximize signal-to-noise ratios for high-speed operation. All high-speed inputs and outputs are terminated to Vcc with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to Vcc +/- 1 V to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$VCC-1 < VAC/4 + VDC < VCC+1$$

Where VAC is the input signal p-p voltage and VDC is common-mode voltage.

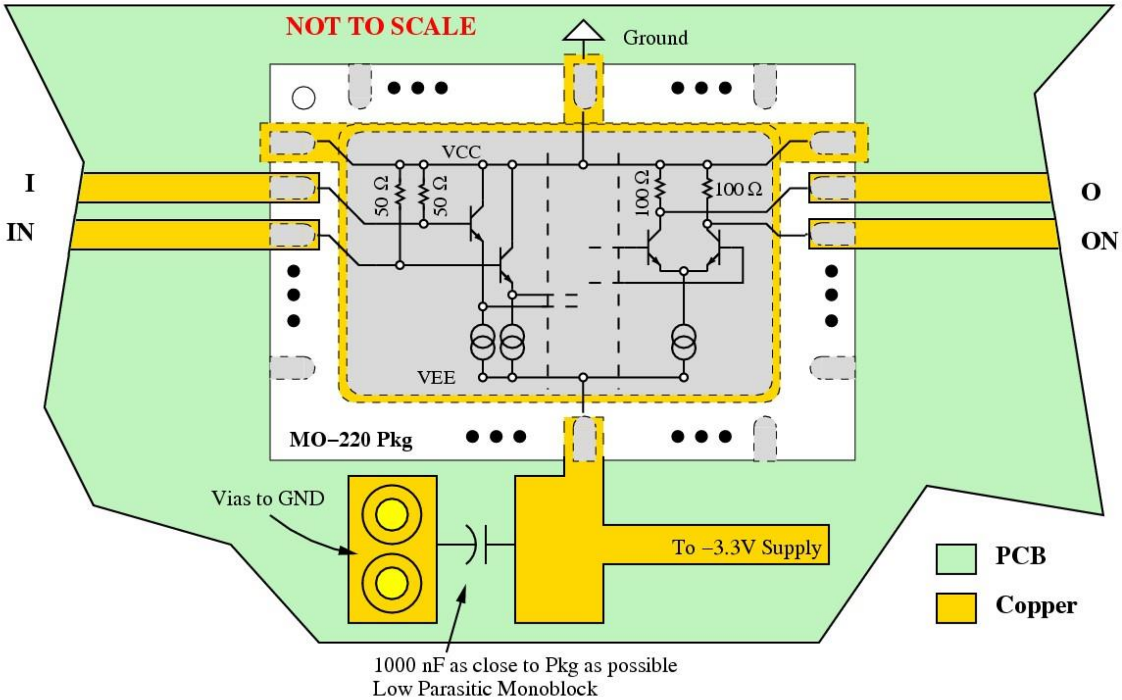
The outputs require a DC return path capable of handling ~30 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be 50 ohms to Vcc. If AC coupling is used, a bias tee circuit should be used such as shown below. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.




In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to Vcc for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest.

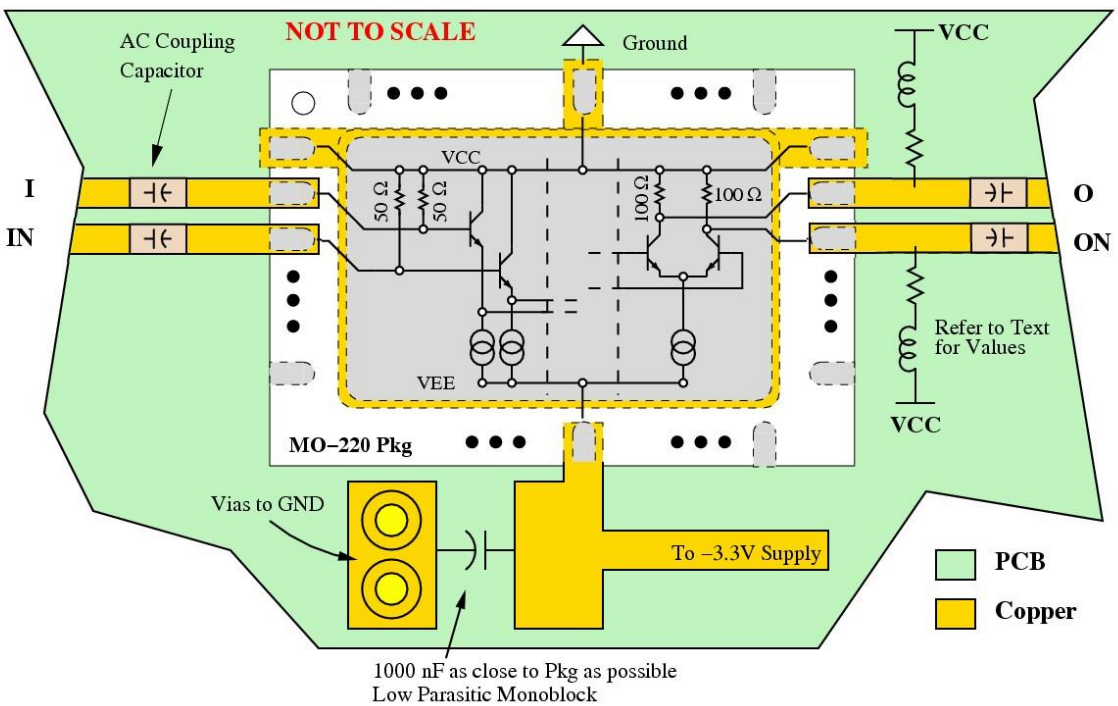
Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Connecting a 10k ohm resistor between the unused input and Vee should provide sufficient offset to prevent oscillation.

## Negative Supply (DC Coupling)



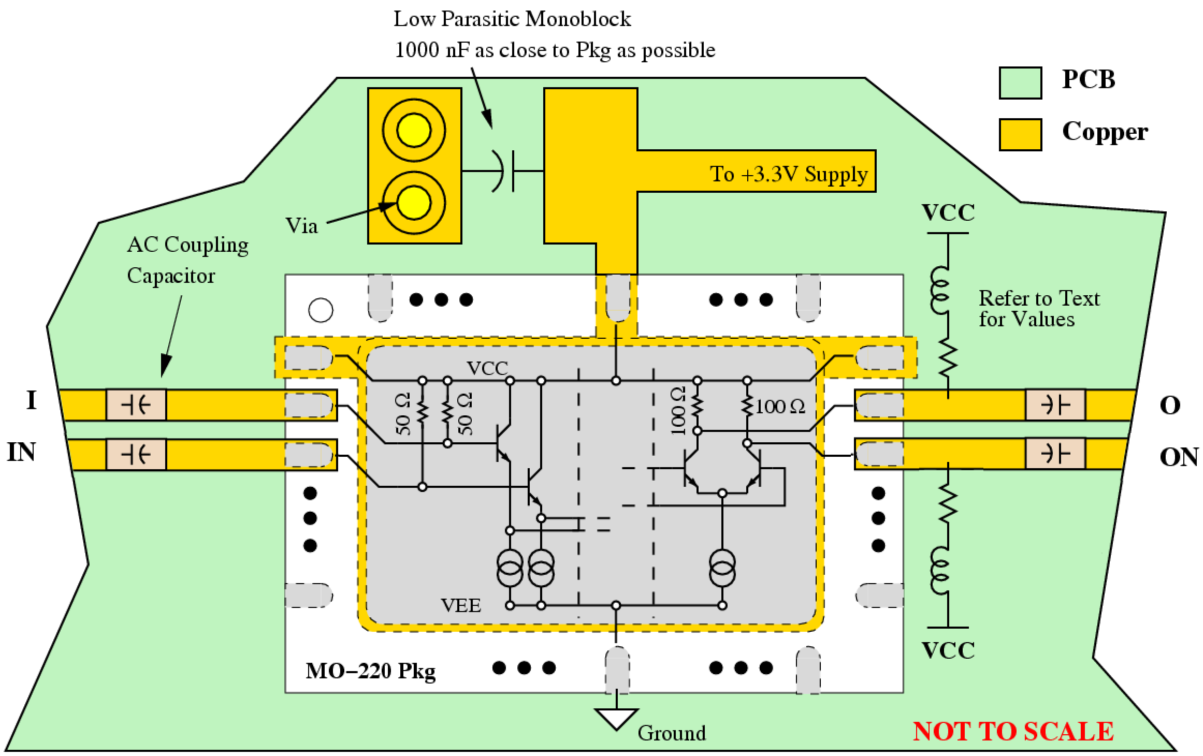

*Negative Supply-DC Coupling*

## Negative Supply (AC Coupling)




*Negative Supply-AC Coupling*

**Positive Supply (AC Coupling)**




We recommend attaching the backside paddle to a good thermal heat sink.

*Positive Supply-AC Coupling*

## Duty Cycle:

The UXN6M9P output duty cycle varies between 25% and 64% as a function of the divide ratio. For divide ratios between 16 and 511, the pulse width remains constant in each octave band (e.g. between 128 and 255), and gives a duty cycle of 50% for powers of 2. Thus, the duty cycle is bounded between 25 and 50% for divide ratios between 16 and 511.

For divide ratios between 8 and 15, the pulse width does not stay fixed, but varies with the divide ratio. The duty cycle ranges from 33% to 64% for these divide ratios.

The table shown below gives pulse width and other necessary information for computing the duty cycle, given the divide ratio. The equation provided allows calculation of the duty cycle based on the information supplied by the table. A chart below summarizes the duty cycles for all possible divide ratios.

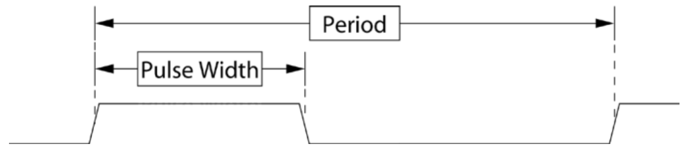
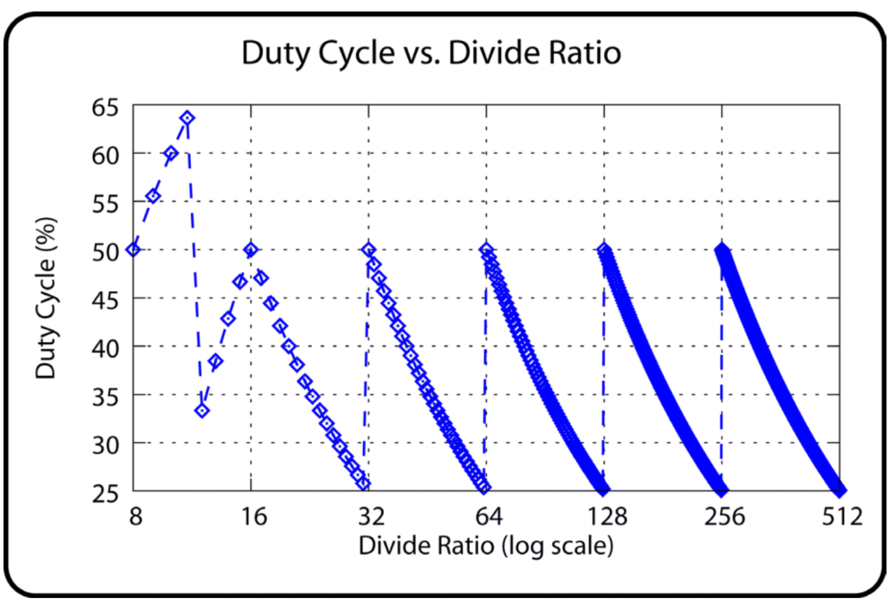



**Table 4: Duty Cycle Summary**

| Divide Ratio | Pulse Width (Input Cycles) | Duty Cycle (%) |
|---|---|---|
| 8 | 4 | 50 |
| 9 | 5 | 55.6 |
| 10 | 6 | 60 |
| 11 | 7 | 63.6 |
| 12 | 4 | 33.3 |
| 13 | 5 | 38.5 |
| 14 | 6 | 42.9 |
| 15 | 7 | 46.7 |
| 16-31 | 8 | 50-25 |
| 32-63 | 16 | 50-25 |
| 64-127 | 32 | 50-25 |
| 128-255 | 64 | 50-25 |
| 256-511 | 128 | 50-25 |

$$\text{Duty Cycle (1\%)} = \frac{\text{Pulse Width}}{\boxed{\phantom{Divide Ratio}}} \times 100\%$$



## Application Notes: Frequency Range Selector

The UXN6M9P includes an internal retimer using a clean signal r(t) derived from the input clock in order to reduce jitter accumulated from passing through multiple divider stages. The UXN6M9P also features a frequency range selector control FRS for changing the phase of r(t) by 180 degrees, or equivalently called a “clock flip”. This clock flip extends the maximum usable input frequency to 9 GHz. See the table provided on how to set FRS for the desired input frequency range.

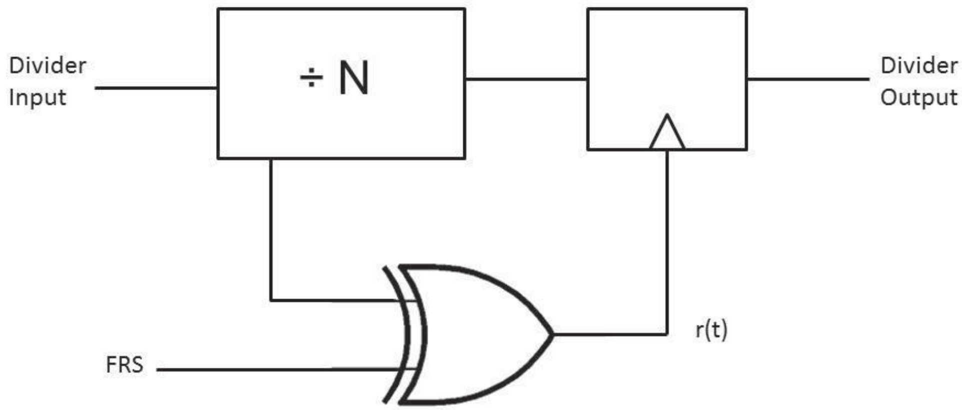



**Table 5: Frequency Range Selector**

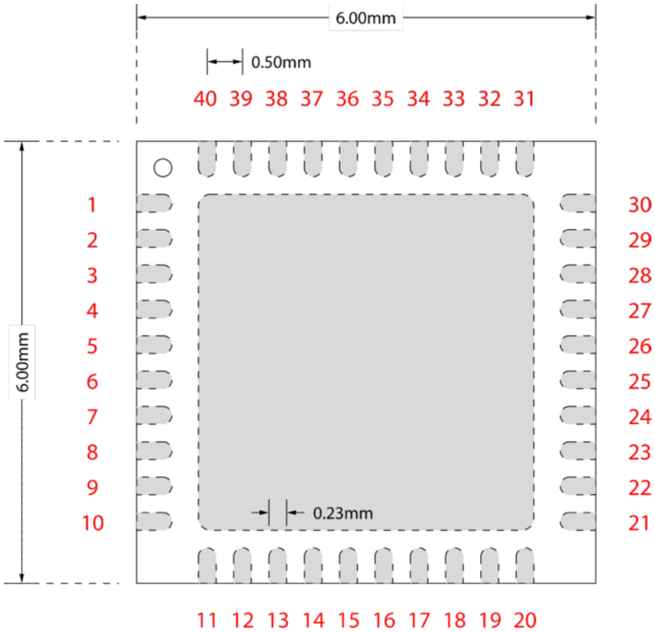
| Input Frequency Range | FRS |
|---|---|
| DC – 6 GHZ | 0 |
| 5 GHz – 9 GHz | 1 |

**Table 6: Frequency Range Selector**

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage (VEE) | -3.8 | V* |
| RF Input Power (INP, INN) | 10 | dBm |
| Operating Temperature | -40 to 85 | ºC |
| Storage Temperature | -85 to 125 | ºC |
| Junction Temperature | 125 | ºC |

**This operating condition may reduce the lifetime of the part and is not recommended.*

## UXN6M9P Physical Characteristics




| | |
|---|---|
| Pkg size: | 6.00 x 6.00 mm |
| Pkg size tolerance: | +/- 0.25 mm |
| Pkg thickness: | 0.9 +/- 0.1 mm |
| Pad dimensions: | 0.23 x 0.4 mm |
| Center paddle: | 4.20 x 4.20 mm |
| JEDEC designator: | MO-220 |

**Top View**

**Table 7: UXN6M9P Pin Definition**

| | Function | Notes |
|---|---|---|
| 5-7,14,24,39 (Vcc) | RF and DC Ground | 0 V |
| 2-4,11,17,25,36,40 (Vee) | Negative Supply Voltage | Nominally -3.3 V |
| 1 (FRS) | Frequency Range Selector | Defaults to logic 0, connect to Vcc for logic 1 |
| 15 (OUTN) | Divider Output | Negative Terminal of differential output |
| 16 (OUTP) | Divider Output | Positive Terminal of differential output |
| 26 (P8) | Divide Modulus Control (MSB) | Defaults to logic 0, connect to Vcc for logic 1 |
| 27 (P7) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 28 (P7) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 29 (P5) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 30 (P4) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 31 (P3) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 32 (P2) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 33 (P1) | Divide Modulus Control | Defaults to logic 0, connect to Vcc for logic 1 |
| 34 (P0) | Divide Modulus Control (LSB) | Defaults to logic 0, connect to Vcc for logic 1 |
| 37 (INN) | Divider Input | Negative Terminal of differential input |
| 38 (INP) | Divider Input | Positive Terminal of differential output |
| Paddle (Backside of Package) | Floating | Tie to ground for heat dissipation |
| 8-10,12,13,18-23,35 (NC) | Floating Pins | |

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.