Features

- Single 2.7V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0 and 3
- 33 MHz Maximum Clock Frequency
- Flexible, Uniform Erase Architecture
  - 4-Kbyte Blocks
  - 32-Kbyte Blocks
  - 64-Kbyte Blocks
  - Full Chip Erase
- Optimized Physical Sectoring for Code Shadowing and Code + Data Storage Applications
  - One 16-Kbyte Top Boot Sector
  - Two 8-Kbyte Sectors
  - One 32-Kbyte Sector
  - Seven 64-Kbyte Sectors
- Individual Sector Protection for Program/Erase Protection
- Hardware Controlled Locking of Protected Sectors
- Byte Program Architecture with Sequential Byte Program Mode Capability
  - Sequential Byte Program Mode Improves Throughput for Programming Multiple Bytes
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 7 mA Active Read Current (Typical)
  - 15 µA Deep Power-down Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-lead SOIC (150-mil and 208-mil wide)
  - 8-pad MLF (6 x 5 x 1.00 mm)

4-megabit 2.7-volt Only Serial Firmware DataFlash® Memory

AT26F004

For New Designs Use AT25DF041A

1. Description

The AT26F004 is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT26F004, with its erase granularity as small as 4 Kbytes, makes it ideal for data storage as well, eliminating the need for additional data storage EEPROM devices.

The physical sectoring and the erase block sizes of the AT26F004 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the physical sectors and erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own protected sectors, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

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The AT26F004 also offers a sophisticated method for protecting individual sectors against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect sectors, a system can unprotect a specific sector to modify its contents while keeping the remaining sectors of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis, or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments.

Specifically designed for use in 3-volt systems, the AT26F004 supports read, program, and erase operations with a supply voltage range of 2.7V to 3.6V. No separate voltage is required for programming and erasing.

2. Pin Descriptions and Pinouts

Table 2-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally placed in standby mode (not Deep Power-down mode), and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**SERIAL CLOCK:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	–	Input
SI	**SERIAL INPUT:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK.	–	Input
SO	**SERIAL OUTPUT:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.	–	Output
$\overline{WP}$	**WRITE PROTECT:** The $\overline{WP}$ pin controls the hardware locking feature of the device. Refer to section "Protection Commands and Features" on page 13 for more details on protection features and the $\overline{WP}$ pin. The $\overline{WP}$ pin is not internally pulled-high and cannot be left floating. If hardware controlled locking will not be used, then the $\overline{WP}$ pin must be externally connected to V_{CC}.	Low	Input
$\overline{HOLD}$	**HOLD:** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, and the SO pin will be in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. Please refer to section "Hold" on page 27 for additional details on the Hold operation. The $\overline{HOLD}$ pin is not internally pulled-high and cannot be left floating. If the Hold function will not be used, then the $\overline{HOLD}$ pin must be externally connected to V_{CC}.	Low	Input
V_{CC}	**DEVICE POWER SUPPLY:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	–	Power
GND	**GROUND:** The ground reference for the power supply. GND should be connected to the system ground.	–	Power

Figure 2-1. 8-SOIC Top View

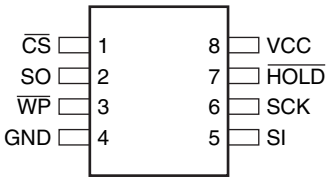
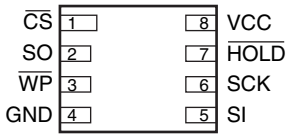
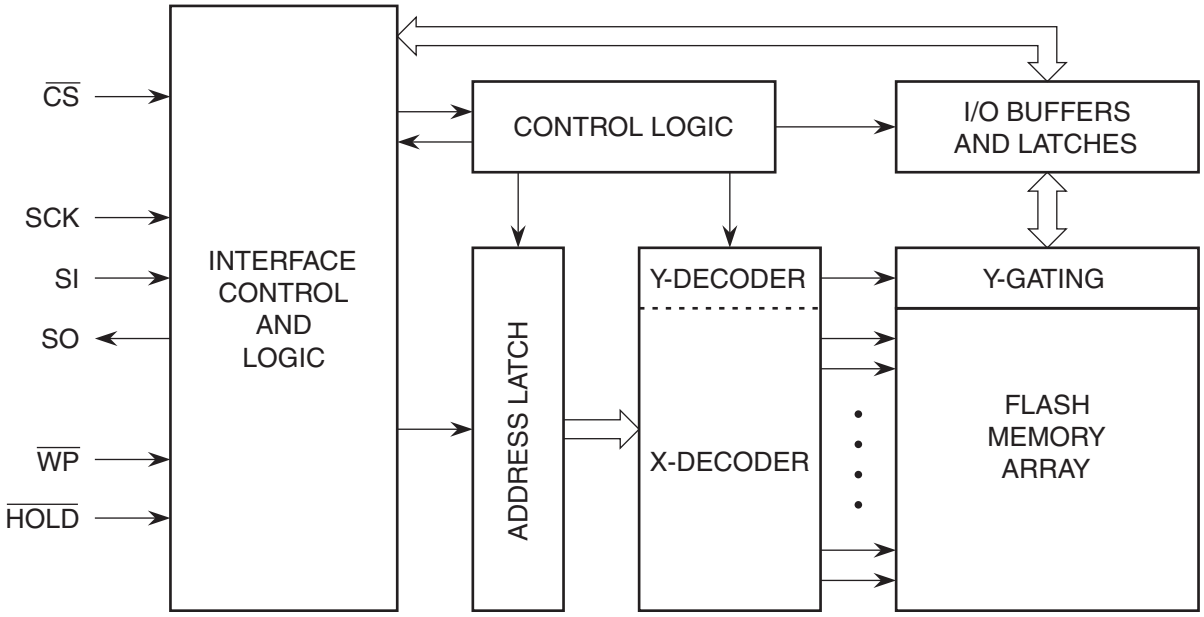


Figure 2-2. 8-MLF Top View



3. Block Diagram



4. Memory Array

To provide the greatest flexibility, the memory array of the AT26F004 can be erased in four levels of granularity including a full chip erase. In addition, the array has been divided into physical sectors of various sizes, of which each sector can be individually protected from program and erase operations. The sizes of the physical sectors are optimized for both code and data storage applications, allowing both code and data segments to reside in their own isolated regions. The Memory Architecture Diagram illustrates the breakdown of each erase level as well as the breakdown of each physical sector.

Figure 4-1. Memory Architecture Diagram

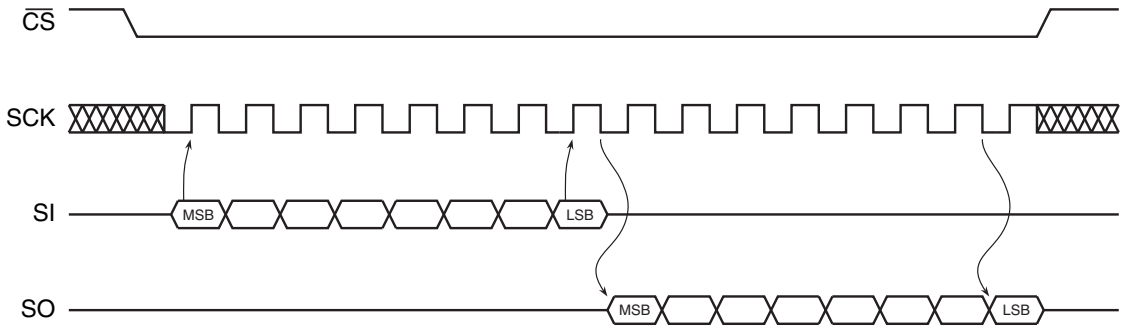
Internal Sectoring for Sector Protection Function	Block Erase Detail: 64KB Block Erase (D8h Command)	Block Erase Detail: 32KB Block Erase (52h Command)	Block Erase Detail: 4KB Block Erase (20h Command)	Block Address Range
16KB (Sector 10)	64KB	32KB	4KB	7FFFFh – 7F000h
			4KB	7EFFFh – 7E000h
			4KB	7DFFFh – 7D000h
			4KB	7CFFFh – 7C000h
8KB (Sector 9)			4KB	7BFFFh – 7B000h
			4KB	7AFFFh – 7A000h
8KB (Sector 8)			4KB	79FFFh – 79000h
			4KB	78FFFh – 78000h
32KB (Sector 7)		32KB	4KB	77FFFh – 77000h
			4KB	76FFFh – 76000h
			4KB	75FFFh – 75000h
			4KB	74FFFh – 74000h
			4KB	73FFFh – 73000h
			4KB	72FFFh – 72000h
			4KB	71FFFh – 71000h
			4KB	70FFFh – 70000h
64KB (Sector 6)	64KB	32KB	4KB	6FFFFh – 6F000h
			4KB	6EFFFh – 6E000h
			4KB	6DFFFh – 6D000h
			4KB	6CFFFh – 6C000h
			4KB	6BFFFh – 6B000h
			4KB	6AFFFh – 6A000h
			4KB	69FFFh – 69000h
			4KB	68FFFh – 68000h
		32KB	4KB	67FFFh – 67000h
			4KB	66FFFh – 66000h
			4KB	65FFFh – 65000h
			4KB	64FFFh – 64000h
			4KB	63FFFh – 63000h
			4KB	62FFFh – 62000h
			4KB	61FFFh – 61000h
			4KB	60FFFh – 60000h
⋮	⋮	⋮	⋮	
64KB (Sector 0)	64KB	32KB	4KB	0FFFFh – 0F000h
			4KB	0EFFFh – 0E000h
			4KB	0DFFFh – 0D000h
			4KB	0CFFFh – 0C000h
			4KB	0BFFFh – 0B000h
			4KB	0AFFFh – 0A000h
			4KB	09FFFh – 09000h
			4KB	08FFFh – 08000h
		32KB	4KB	07FFFh – 07000h
			4KB	06FFFh – 06000h
			4KB	05FFFh – 05000h
			4KB	04FFFh – 04000h
			4KB	03FFFh – 03000h
			4KB	02FFFh – 02000h
			4KB	01FFFh – 01000h
			4KB	00FFFh – 00000h

5. Device Operation

The AT26F004 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the AT26F004 via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{CS}$), Serial Clock (SCK), Serial Input (SI), and Serial Output (SO).

The SPI protocol defines a total of four modes of operation (mode 0, 1, 2, or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT26F004 supports the two most common modes, SPI modes 0 and 3. The only difference between SPI modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI Master is in standby mode and not transferring any data). With SPI modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK.

Figure 5-1. SPI Mode 0 and 3



6. Commands and Addressing

A valid instruction or operation must always be started by first asserting the $\overline{CS}$ pin. After the $\overline{CS}$ pin has been asserted, the SPI Master must then clock out a valid 8-bit opcode on the SPI bus. Following the opcode, instruction dependent information such as address and data bytes would then be clocked out by the SPI Master. All opcode, address, and data bytes are transferred with the most significant bit (MSB) first. An operation is ended by deasserting the $\overline{CS}$ pin.

Opcodes not supported by the AT26F004 will be ignored by the device and no operation will be started. The device will continue to ignore any data presented on the SI pin until the start of the next operation ($\overline{CS}$ pin being deasserted and then reasserted). In addition, if the $\overline{CS}$ pin is deasserted before all eight bits of an opcode are sent to the device, then the device will simply return to the idle state and wait for the next operation.

Addressing of the device requires a total of three bytes of information to be sent, representing address bits A23 - A0. Since the upper address limit of the AT26F004 memory array is 07FFFFh, address bits A23 - A19 are always ignored by the device.

Table 6-1. Command Listing

Command	Opcode		Address Bytes	Dummy Bytes	Data Bytes
Read Commands					
Read Array	0Bh	0000 1011	3	1	1+
Read Array (Low Frequency)	03h	0000 0011	3	0	1+
Program and Erase Commands					
Block Erase (4 KBytes)	20h	0010 0000	3	0	0
Block Erase (32 KBytes)	52h	0101 0010	3	0	0
Block Erase (64 KBytes)	D8h	1101 1000	3	0	0
Chip Erase	60h	0110 0000	0	0	0
	C7h	1100 0111	0	0	0
Byte Program	02h	0000 0010	3	0	1
Sequential Byte Program Mode	AFh	1010 1111	3, 0[1]	0	1
Protection Commands					
Write Enable	06h	0000 0110	0	0	0
Write Disable	04h	0000 0100	0	0	0
Protect Sector	36h	0011 0110	3	0	0
Unprotect Sector	39h	0011 1001	3	0	0
Read Sector Protection Registers	3Ch	0011 1100	3	0	1+
Status Register Commands					
Read Status Register	05h	0000 0101	0	0	1+
Write Status Register	01h	0000 0001	0	0	1
Miscellaneous Commands					
Read Manufacturer and Device ID	9Fh	1001 1111	0	0	1 to 4
Deep Power-down	B9h	1011 1001	0	0	0
Resume from Deep Power-down	ABh	1010 1011	0	0	0

Notes: 1. Three address bytes are only required for the first operation to designate the address at which to start the programming. Afterwards, the internal address counter automatically increments, so subsequent Sequential Program Mode operations only require clocking in of the opcode and the data byte until the Sequential Program Mode has been exited.

7. Read Commands

7.1 Read Array

The Read Array command can be used to sequentially read a continuous stream of data from the device by simply providing the SCK signal once the initial starting address has been specified. The device incorporates an internal address counter that automatically increments on every clock cycle.

Two opcodes, 0Bh and 03h, can be used for the Read Array command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the device. The 0Bh opcode can be used at any SCK frequency up to the maximum specified by f_{SCK}. The 03h opcode can be used for lower frequency read operations up to the maximum specified by f_{RDLF}.

To perform the Read Array operation, the $\overline{CS}$ pin must first be asserted and the appropriate opcode (0Bh or 03h) must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the memory array. If the 0Bh opcode is used, then one don't care byte must also be clocked in after the three address bytes.

After the three address bytes (and the one don't care byte if using opcode 0Bh) have been clocked in, additional clock cycles will result in serial data being output on the SO pin. The data is always output with the MSB of a byte first. When the last byte (07FFFFh) of the memory array has been read, the device will continue reading back at the beginning of the array (000000h). No delays will be incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the $\overline{CS}$ pin will terminate the read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Figure 7-1. Read Array - 0Bh Opcode

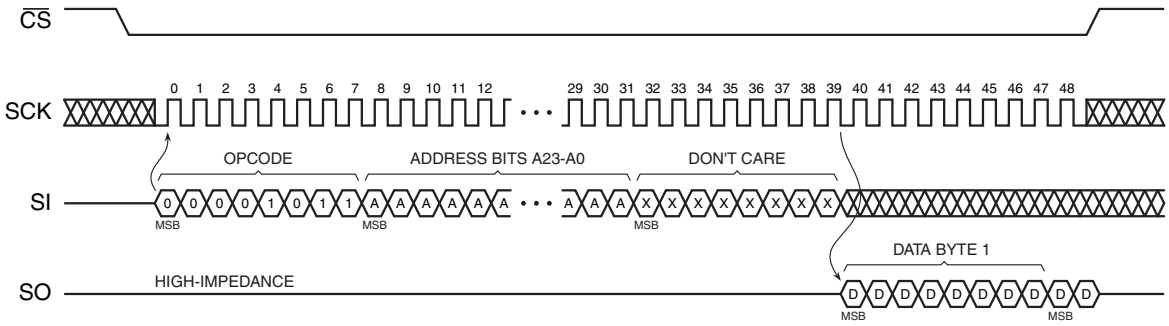
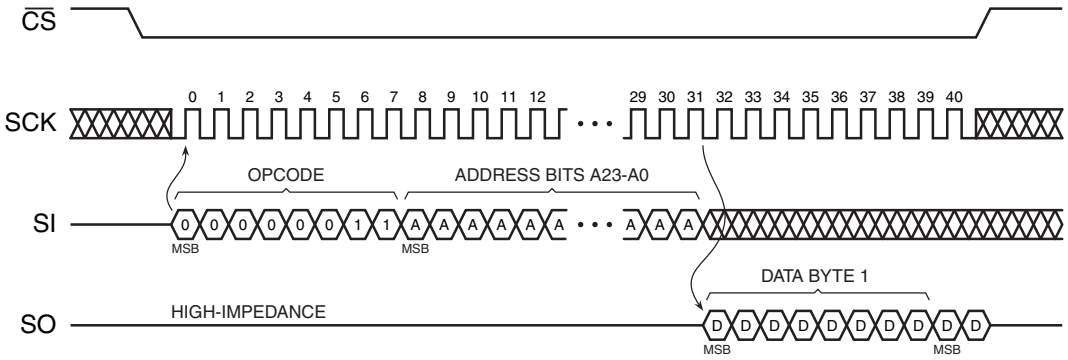


Figure 7-2. Read Array - 03h Opcode



8. Program and Erase Commands

8.1 Byte Program

The Byte Program command allows a single byte of data to be programmed into a previously erased memory location. An erased memory location is one that has all eight bits set to the logical “1” state (a byte value of FFh). Before a Byte Program command can be started, the Write Enable command must have been previously issued to the device (see “Write Enable” on page 13) to set the Write Enable Latch (WEL) bit of the Status Register to a logical “1” state.

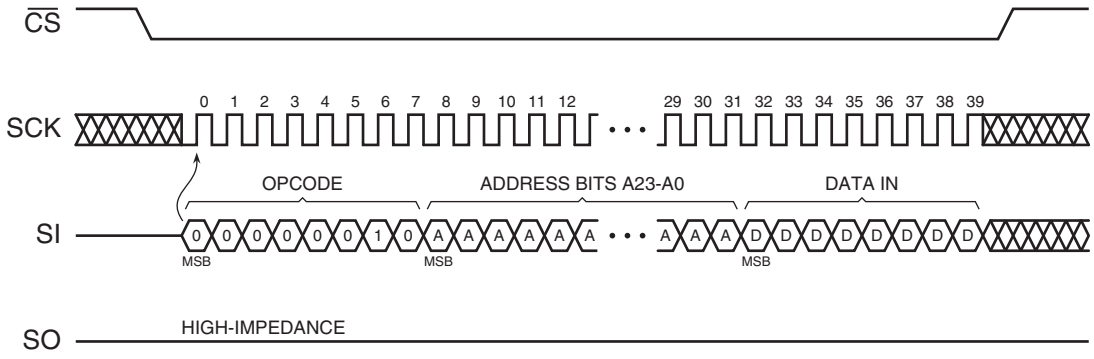
To perform a Byte Program command, an opcode of 02h must be clocked into the device followed by the three address bytes denoting which byte location of the memory array to program. After the address bytes have been clocked in, the next byte of data clocked into the device will be latched internally. If more than one byte of data is clocked in, then only the first byte of data sent on the SI pin will be stored in the internal latches and all subsequent bytes will be ignored.

When the $\overline{CS}$ pin is deasserted, the device will take the one byte stored in the internal latches and program it into the memory array location specified by A23 - A0. The programming of the byte is internally self-timed and should take place in a time of t_{BP}. The three address bytes and a complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and no data will be programmed into the memory array. In addition, if the address specified by A23 - A0 points to a memory location within a sector that is in the protected state (see “Protect Sector” on page 15), then the Byte Program command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will be reset back to the logical “0” state if the program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, or because the memory location to be programmed is protected.

While the device is programming, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{BP} time to determine if the byte has finished programming. At some point before the program cycle completes, the WEL bit in the Status Register will be reset back to the logical “0” state.

The Byte Program mode is the default programming mode after the device powers-up or resumes from a device reset.

Figure 8-1. Byte Program



8.2 Sequential Byte Program Mode

The Sequential Byte Program mode improves throughput over the single Byte Program operation when programming multiple bytes of data into consecutive address locations. When using the Sequential Byte Programming mode, an internal address counter keeps track of the byte location to program, thereby eliminating the need to supply an address sequence to the device for every byte to program. All address locations to be programmed using the Sequential Byte Program mode must be in the erased state. Before the Sequential Byte Program mode can first be entered, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical “1” state.

To start the Sequential Byte Program mode, the $\overline{CS}$ pin must first be asserted, and the opcode of AFh must be clocked into the device. For the first program cycle, three address bytes must be clocked in after the opcode to designate the first byte location to program. After the address bytes have been clocked in, the next byte of data clocked into the device will be latched internally. Deasserting the $\overline{CS}$ pin will start the internally self-timed program operation, and the first byte will be programmed into the memory location specified by A23 - A0.

After the first byte has been successfully programmed, a second byte can be programmed by simply reasserting the $\overline{CS}$ pin, clocking in the AFh opcode, and then clocking in the next byte of data. When the $\overline{CS}$ pin is deasserted, the second byte of data will be programmed into the next sequential memory location. The process would be repeated for any additional bytes. There is no need to reissue the Write Enable command once the Sequential Byte Program mode has been entered.

When the last desired byte has been programmed into the memory array, the Sequential Byte Program mode operation can be terminated by reasserting the $\overline{CS}$ pin and sending the Write Disable command to the device to reset the WEL bit in the Status Register back to the logical “0” state.

If more than one byte of data is ever clocked in during each program cycle, then only the first byte of data sent on the SI pin will be stored in the internal latches and all subsequent bytes will be ignored. The programming of each byte is internally self-timed and should take place in a time of t_{BP}. For each program cycle, a complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation, the byte of data will not be programmed into the memory array, and the WEL bit in the Status Register will be reset back to the logical “0” state.

If the address initially specified by A23 - A0 points to a memory location within a sector that is in the protected state, then the Sequential Byte Program mode command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will also be reset back to the logical “0” state.

There is no address wrapping when using the Sequential Byte Program mode. Therefore, when the last byte (07FFFFh) of the memory array has been programmed, the device will automatically exit the Sequential Byte Program mode and reset the WEL bit in the Status Register back to the logical “0” state. In addition, the Sequential Byte Program mode will not automatically skip over protected sectors; therefore, once the highest unprotected memory location in a programming sequence has been programmed, the device will automatically exit the Sequential Byte Program mode and reset the WEL bit in the Status Register. For example, if Sector 1 was protected and Sector 0 was currently being programmed, once the last byte of Sector 0 was programmed, the Sequential Byte Program mode would automatically end. To continue programming with Sector 2, the Sequential Byte Program mode would have to be restarted by supplying the AFh opcode, the three address bytes, and the first byte of Sector 2 to program.

While the device is programming a byte, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled at the end of each program cycle rather than waiting the t_{BP} time to determine if the byte has finished programming before starting the next Sequential Byte Program mode cycle.

Figure 8-2. Sequential Byte Program Mode – Status Register Polling

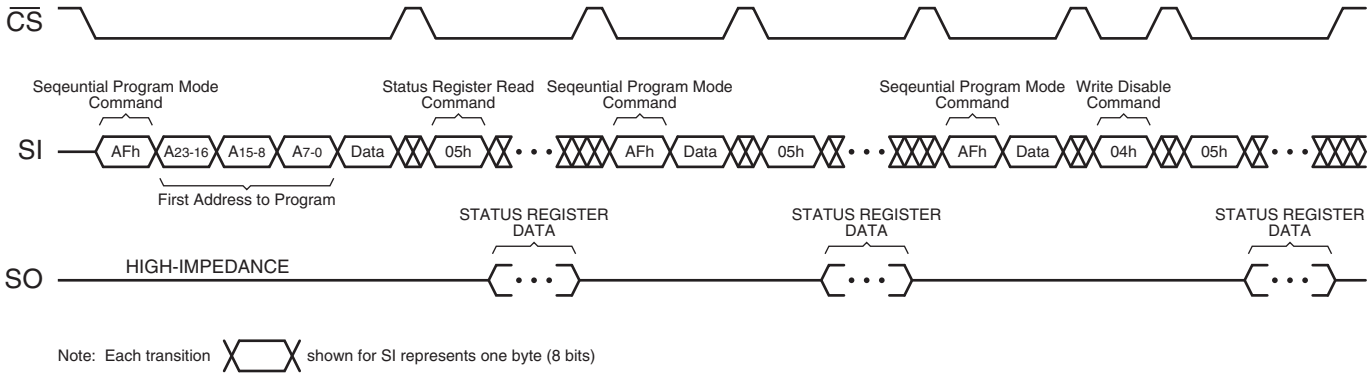
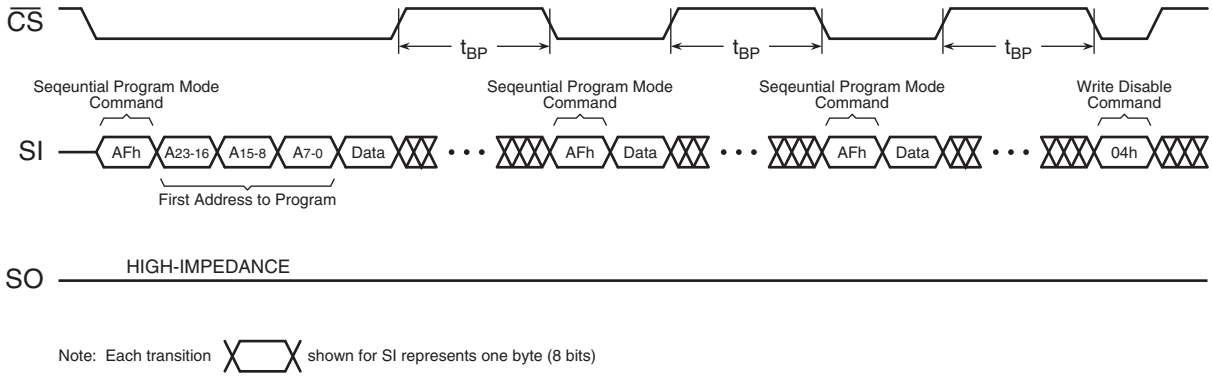


Figure 8-3. Sequential Byte Program Mode – Waiting Maximum Byte Program Time



8.3 Block Erase

A block of 4 Kbytes, 32 Kbytes, or 64 Kbytes can be erased (all bits set to the logical “1” state) in a single operation by using one of three different opcodes for the Block Erase command. An opcode of 20h is used for a 4-Kbyte erase, an opcode of 52h is used for a 32-Kbyte erase, and an opcode of D8h is used for a 64-Kbyte erase. Before a Block Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical “1” state.

To perform a Block Erase, the $\overline{CS}$ pin must first be asserted and the appropriate opcode (20h, 52h or D8h) must be clocked into the device. After the opcode has been clocked in, the three address bytes specifying an address within the 4-Kbyte, 32-Kbyte, or 64-Kbyte block to be erased must be clocked in. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the device will erase the appropriate block. The erasing of the block is internally self-timed and should take place in a time of t_{BLKE}.

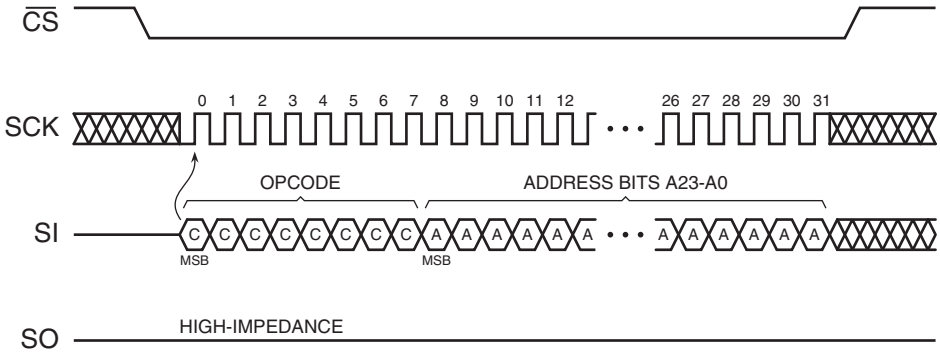
Since the Block Erase command erases a region of bytes, the lower order address bits do not need to be decoded by the device. Therefore, for a 4-Kbyte erase, address bits A11 - A0 will be ignored by the device and their values can be either a logical “1” or “0”. For a 32-Kbyte erase, address bits A14 - A0 will be ignored, and for a 64-Kbyte erase, address bits A15 - A0 will be ignored by the device. Despite the lower order address bits not being decoded by the device, the complete three address bytes must still be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and no erase operation will be performed.

If the address specified by A23 - A0 points to a memory location within a sector that is in the protected state, then the Block Erase command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. In addition, with the larger Block Erase sizes of 32 Kbytes and 64 Kbytes, more than one physical sector may be erased (e.g. sectors 10, 9 and 8) at one time. Therefore, in order to erase a larger block that may span more than one sector, all of the sectors in the span must be in the unprotected state. If one of the physical sectors within the span is in the protected state, then the device will ignore the Block Erase command and will return to the idle state once the $\overline{CS}$ pin is deasserted.

The WEL bit in the Status Register will be reset back to the logical “0” state if the erase cycle aborts due to an incomplete address being sent or because a memory location within the region to be erased is protected.

While the device is executing a successful erase cycle, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{BLKE} time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register will be reset back to the logical “0” state.

Figure 8-4. Block Erase



8.4 Chip Erase

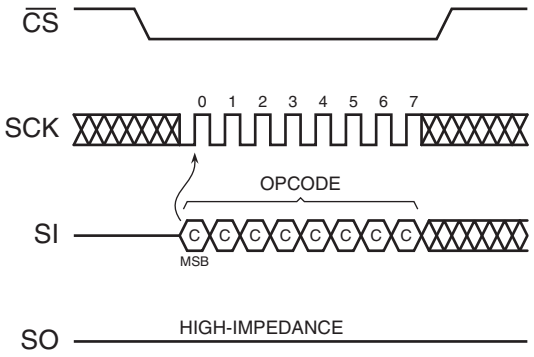
The entire memory array can be erased in a single operation by using the Chip Erase command. Before a Chip Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical “1” state.

Two opcodes, 60h and C7h, can be used for the Chip Erase command. There is no difference in device functionality when utilizing the two opcodes, so they can be used interchangeably. To perform a Chip Erase, one of the two opcodes (60h or C7h) must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will erase the entire memory array. The erasing of the device is internally self-timed and should take place in a time of t_{CHPE}.

The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, no erase will be performed. In addition, if any sector of the memory array is in the protected state, then the Chip Erase command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will be reset back to the logical “0” state if a sector is in the protected state.

While the device is executing a successful erase cycle, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{CHPE} time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register will be reset back to the logical “0” state.

Figure 8-5. Chip Erase



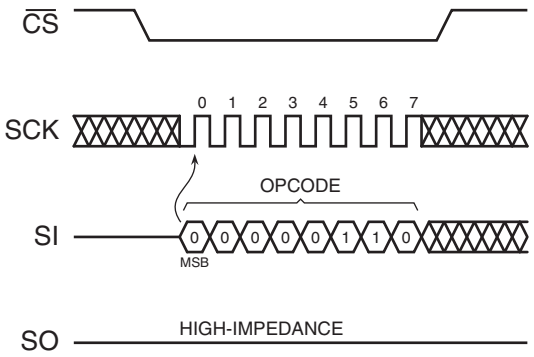
9. Protection Commands and Features

9.1 Write Enable

The Write Enable command is used to set the Write Enable Latch (WEL) bit in the Status Register to a logical “1” state. The WEL bit must be set before a program, erase, Protect Sector, Unprotect Sector, or Write Status Register command can be executed. This makes the issuance of these commands a two step process, thereby reducing the chances of a command being accidentally or erroneously executed. If the WEL bit in the Status Register is not set prior to the issuance of one of these commands, then the command will not be executed.

To issue the Write Enable command, the $\overline{CS}$ pin must first be asserted and the opcode of 06h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register will be set to a logical “1”. The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and the state of the WEL bit will not change.

Figure 9-1. Write Enable

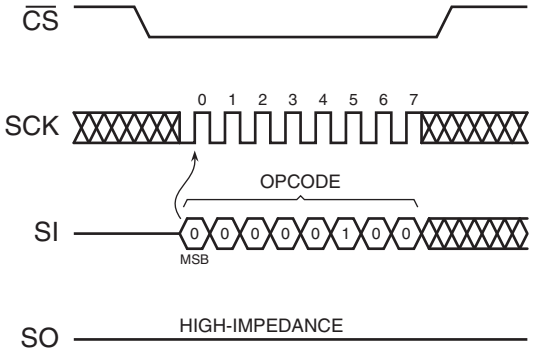


9.2 Write Disable

The Write Disable command is used to reset the Write Enable Latch (WEL) bit in the Status Register to the logical “0” state. With the WEL bit reset, all program, erase, Protect Sector, Unprotect Sector, and Write Status Register commands will not be executed. The Write Disable command is also used to exit the Sequential Program mode. Other conditions can also cause the WEL bit to be reset; for more details, refer to the “WEL Bit” on page 20.

To issue the Write Disable command, the $\overline{CS}$ pin must first be asserted and the opcode of 04h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register will be reset to a logical “0”. The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and the state of the WEL bit will not change.

Figure 9-2. Write Disable



9.3 Protect Sector

Every physical sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector. Upon device power-up or after a device reset, each Sector Protection Register will default to the logical “1” state indicating that all sectors are protected and cannot be programmed or erased.

Issuing the Protect Sector command to a particular sector address will set the corresponding Sector Protection Register to the logical “1” state. The following table outlines the two states of the Sector Protection Registers.

Table 9-1. Sector Protection Register Values

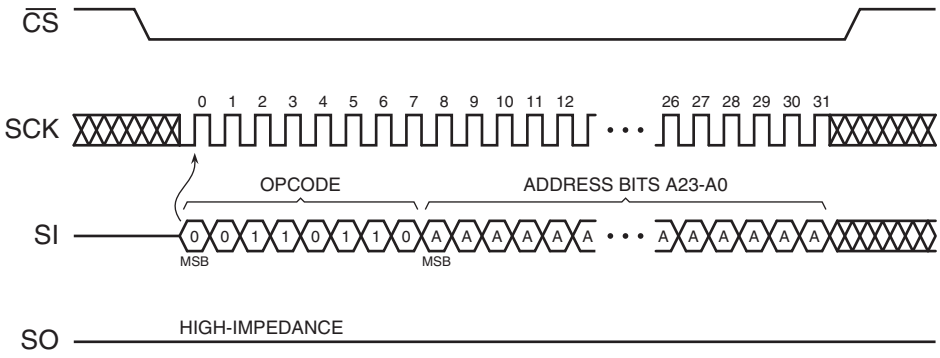
Value	Sector Protection Status
0	Sector is unprotected and can be programmed and erased.
1	Sector is protected and cannot be programmed or erased. This is the default state.

Before the Protect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical “1”. To issue the Protect Sector command, the $\overline{CS}$ pin must first be asserted and the opcode of 36h must be clocked into the device followed by three address bytes designating any address within the sector to be locked. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the Sector Protection Register corresponding to the physical sector addressed by A23 - A0 will be set to the logical “1” state, and the sector itself will then be protected from program and erase operations. In addition, the WEL bit in the Status Register will be reset back to the logical “0” state.

The complete three address bytes must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation, the state of the Sector Protection Register will be unchanged, and the WEL bit in the Status Register will be reset to a logical “0”.

As a safeguard against accidental or erroneous protecting or unprotecting of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (refer to “Status Register Commands” on page 19 for more details). If the Sector Protection Registers are locked, then any attempts to issue the Protect Sector command will be ignored, and the device will reset the WEL bit in the Status Register back to a logical “0” and return to the idle state once the $\overline{CS}$ pin has been deasserted.

Figure 9-3. Protect Sector



9.4 Unprotect Sector

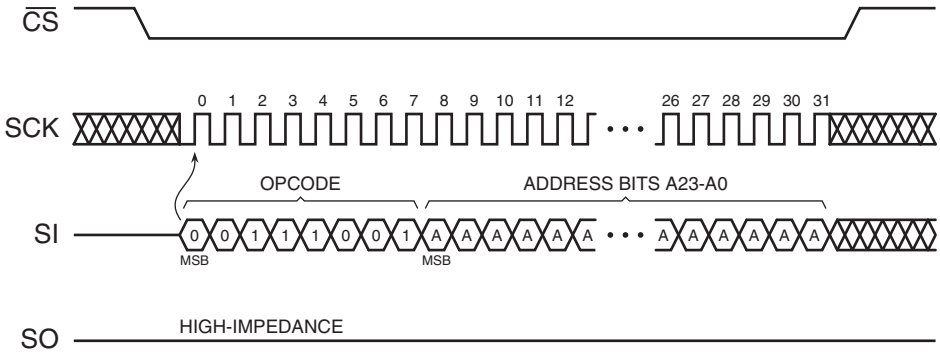
Issuing the Unprotect Sector command to a particular sector address will reset the corresponding Sector Protection Register to the logical “0” state (see Table 9-1 for Sector Protection Register values). Every physical sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector.

Before the Unprotect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical “1”. To issue the Unprotect Sector command, the $\overline{CS}$ pin must first be asserted and the opcode of 39h must be clocked into the device. After the opcode has been clocked in, the three address bytes designating any address within the sector to be unlocked must be clocked in. Any additional data clocked into the device after the address bytes will be ignored. When the $\overline{CS}$ pin is deasserted, the Sector Protection Register corresponding to the sector addressed by A23 - A0 will be reset to the logical “0” state, and the sector itself will be unprotected. In addition, the WEL bit in the Status Register will be reset back to the logical “0” state.

The complete three address bytes must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation, the state of the Sector Protection Register will be unchanged, and the WEL bit in the Status Register will be reset to a logical “0”.

As a safeguard against accidental or erroneous locking or unlocking of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (refer to “Status Register Commands” on page 19 for more details). If the Sector Protection Registers are locked, then any attempts to issue the Unprotect Sector command will be ignored, and the device will reset the WEL bit in the Status Register back to a logical “0” and return to the idle state once the $\overline{CS}$ pin has been deasserted.

Figure 9-4. Unprotect Sector



9.5 Read Sector Protection Registers

The Sector Protection Registers can be read to determine the current software protection status of each sector. Reading the Sector Protection Registers, however, will not determine the status of the $\overline{WP}$ pin.

To read the Sector Protection Register for a particular sector, the $\overline{CS}$ pin must first be asserted and the opcode of 3Ch must be clocked in. Once the opcode has been clocked in, three address bytes designating any address within the sector must be clocked in. After the last address byte has been clocked in, the device will begin outputting data on the SO pin during every subsequent clock cycle. The data being output will be a repeating byte of either FFh or 00h to denote the value of the appropriate Sector Protection Register.

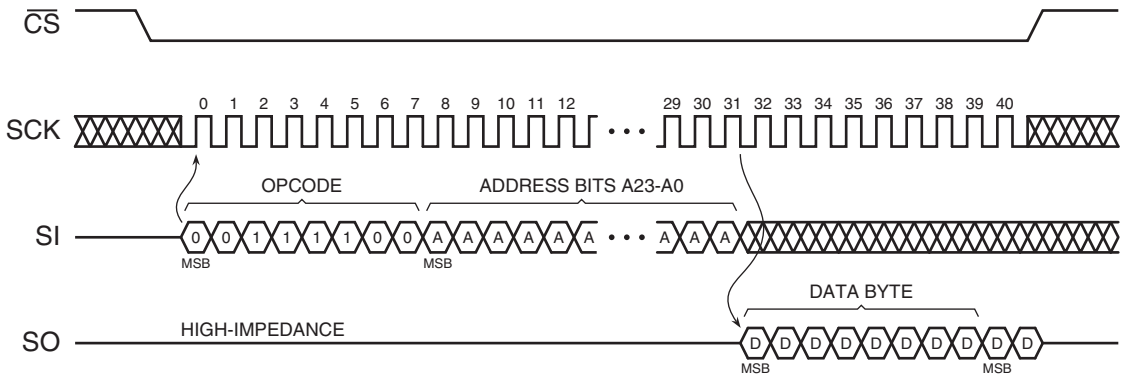
Table 9-2. Read Sector Protection Register – Output Data

Output Data	Sector Protection Register Value
00h	Sector Protection Register value is 0 (sector is unprotected).
FFh	Sector Protection Register value is 1 (sector is protected).

Deasserting the $\overline{CS}$ pin will terminate the read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

In addition to reading the individual Sector Protection Registers, the Software Protection Status (SWP) bit in the Status Register can be read to determine if all, some, or none of the sectors are software protected (refer "Status Register Commands" on page 19 for more details).

Figure 9-5. Read Sector Protection Register



9.6 Protected States and the Write Protect ($\overline{WP}$) Pin

The $\overline{WP}$ pin is not linked to the memory array itself and has no direct effect on the protection status of the memory array. Instead, the $\overline{WP}$ pin, in conjunction with the SPRL (Sector Protection Registers Locked) bit in the Status Register, is used to control the hardware locking mechanism of the device. For hardware locking to be active, two conditions must be met-the $\overline{WP}$ pin must be asserted and the SPRL bit must be in the logical "1" state.

When hardware locking is active, the Sector Protection Registers are locked and the SPRL bit itself is also locked. Therefore, sectors that are protected will be locked in the protected state, and sectors that are unprotected will be locked in the unprotected state. These states cannot be changed as long as hardware locking is active, so the Protect Sector, Unprotect Sector, and Write Status Register commands will be ignored. In order to modify the protection status of a sector, the $\overline{WP}$ pin must first be deasserted, and the SPRL bit in the Status Register must be reset back to the logical "0" state.

If the $\overline{WP}$ pin is permanently connected to GND, then once the SPRL bit is set to a logical "1", the only way to reset the bit back to the logical "0" state is to power-cycle or reset the device. This allows a system to power-up with all sectors software protected but not hardware locked. Therefore, sectors can be unprotected and protected as needed and then hardware locked at a later time by simply setting the SPRL bit in the Status Register.

When the $\overline{WP}$ pin is deasserted, or if the $\overline{WP}$ pin is permanently connected to VCC, the SPRL bit in the Status Register can still be set to a logical "1" to lock the Sector Protection Registers. This provides a software locking ability to prevent erroneous Protect Sector or Unprotect Sector commands from being processed.

Tables 9-3 and 9-4 detail the various protection and locking states of the device.

Table 9-3. Software Protection

$\overline{WP}$	Sector Protection Register n(1)	Sector n(1)
X (Don't Care)	0	Unprotected
	1	Protected

Note: 1. "n" represents a sector number

Table 9-4. Hardware and Software Locking

$\overline{WP}$	SPRL	Locking	SPRL	Sector Protection Registers
0	0	–	Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands
0	1	Hardware locked	Locked	Locked in current state. Protect and Unprotect Sector commands will be ignored.
1	0	–	Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands
1	1	Software locked	Can be modified from 1 to 0	Locked in current state. Protect and Unprotect Sector commands will be ignored.

10. Status Register Commands

10.1 Read Status Register

The Status Register can be read to determine the device's ready/busy status, as well as the status of many other functions such as Hardware Locking and Software Protection. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the $\overline{CS}$ pin must first be asserted and the opcode of 05h must be clocked into the device. After the last bit of the opcode has been clocked in, the device will begin outputting Status Register data on the SO pin during every subsequent clock cycle. After the last bit (bit 0) of the Status Register has been clocked out, the sequence will repeat itself starting again with bit 7 as long as the $\overline{CS}$ pin remains asserted and the SCK pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence will output new data.

Deasserting the $\overline{CS}$ pin will terminate the Read Status Register operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 10-1. Status Register Format

Bit[1]	Name		Type[2]	Description	
7	SPRL	Sector Protection Registers Locked	R/W	0 1	Sector Protection Registers are unlocked (default). Sector Protection Registers are locked.
6	SPM	Sequential Program Mode Status	R	0 1	Byte programming mode (default). Sequential Programming mode entered.
5	RES	Reserved for future use	R	0	Reserved for future use.
4	WPP	Write Protect ($\overline{WP}$) Pin Status	R	0 1	$\overline{WP}$ is asserted. $\overline{WP}$ is deasserted.
3:2	SWP	Software Protection Status	R	00 01 10 11	All sectors are software unprotected. Some sectors are software protected. Read Sector Protection Registers. Reserved for future use. All sectors are software protected (default).
1	WEL	Write Enable Latch Status	R	0 1	Device is not write enabled (default). Device is write enabled.
0	RDY/BSY	Ready/Busy Status	R	0 1	Device is ready. Device is busy with an internal operation.

Notes: 1. Bit 7 of the Status Register is the only bit that can be user modified

2. R/W = Readable and writable
   R = Readable only

10.1.1 SPRL Bit

The SPRL bit is used to control whether the Sector Protection Registers can be modified or not. When the SPRL bit is in the logical “1” state, all Sector Protection Registers are locked and cannot be modified with the Protect Sector and Unprotect Sector commands (the device will ignore these commands). Any sectors that are presently protected will remain protected, and any sectors that are presently unprotected will remain unprotected.

When the SPRL bit is in the logical “0” state, all Sector Protection Registers are unlocked and can be modified (the Protect Sector and Unprotect Sector commands will be processed as normal). The SPRL bit defaults to the logical “0” state after a power-up or a device reset.

The SPRL bit can be modified freely whenever the $\overline{WP}$ pin is deasserted. However, if the $\overline{WP}$ pin is asserted, then the SPRL bit may only be changed from a logical “0” (Sector Protection Registers are unlocked) to a logical “1” (Sector Protection Registers are locked). In order to reset the SPRL bit back to a logical “0” using the Write Status Register command, the $\overline{WP}$ pin will have to first be deasserted.

The SPRL bit is the only bit of the Status Register than can be user modified via the Write Status Register command.

10.1.2 SPM Bit

The SPM bit indicates whether the device is in the Byte Program mode or the Sequential Program mode. The default state after power-up or device reset is the Byte Program mode.

10.1.3 WPP Bit

The WPP bit can be read to determine if the $\overline{WP}$ pin has been asserted or not.

10.1.4 SWP Bits

The SWP bits provide feedback on the software protection status for the device. There are three possible combinations of the SWP bits that indicate whether none, some, or all of the sectors have been protected using the Protect Sector command. If the SWP bits indicate that some of the sectors have been protected, then the individual Sector Protection Registers can be read with the Read Sector Protection Registers command to determine which sectors are in fact protected.

10.1.5 WEL Bit

The WEL bit indicates the current status of the internal Write Enable Latch. When the WEL bit is in the logical “0” state, the device will not accept any program, erase, Protect Sector, Unprotect Sector, or Write Status Register commands. The WEL bit defaults to the logical “0” state after a device power-up or reset. In addition, the WEL bit will be reset to the logical “0” state automatically under the following conditions:

- Write Disable operation completes successfully
- Write Status Register operation completes successfully or aborts
- Protect Sector operation completes successfully or aborts
- Unprotect Sector operation completes successfully or aborts
- Byte Program operation completes successfully or aborts
- Sequential Program Mode reaches highest unprotected memory location
- Sequential Program Mode reaches the end of the memory array
- Sequential Program Mode aborts

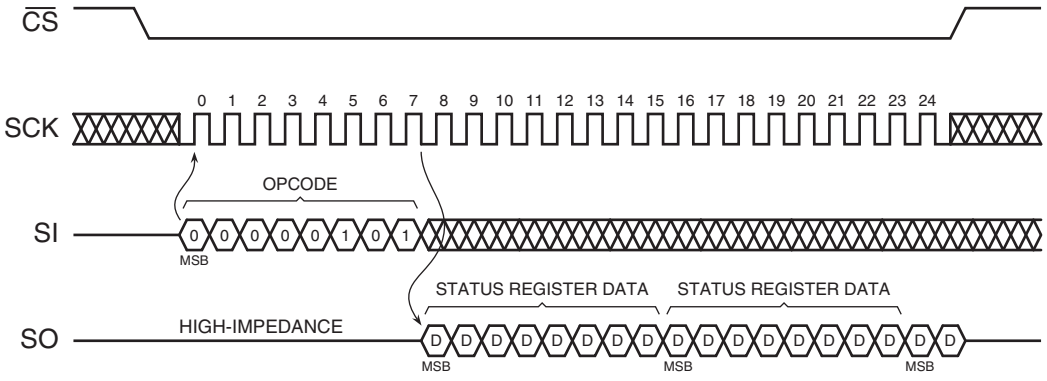
- Block Erase operation completes successfully or aborts
- Chip Erase operation completes successfully or aborts

If the WEL bit is in the logical “1” state, it will not be reset to a logical “0” if an operation aborts due to an incomplete or unrecognized opcode being clocked into the device before the $\overline{CS}$ pin is deasserted. In order for the WEL bit to be reset when an operation aborts prematurely, the entire opcode for a program, erase, Protect Sector, Unprotect Sector, or Write Status Register command must have been clocked into the device.

10.1.6 RDY/BSY Bit

The RDY/BSY bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/BSY bit to detect the completion of a program or erase cycle, new Status Register data must be continually clocked out of the device until the state of the RDY/BSY bit changes from a logical “1” to a logical “0”.

Figure 10-1. Read Status Register



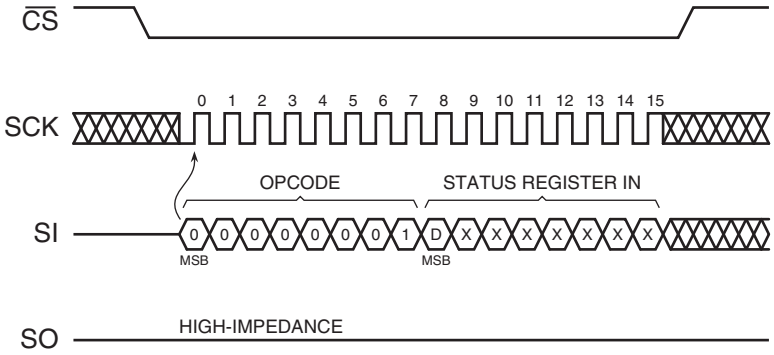
10.2 Write Status Register

The Write Status Register command is used to modify the SPRL bit of the Status Register. Before the Write Status Register command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical “1”.

To issue the Write Status Register command, the $\overline{CS}$ pin must first be asserted and the opcode of 01h must be clocked into the device. After the opcode has been clocked in, one byte of data comprised of the SPRL bit value and seven don't care bits must be clocked in. Any additional data bytes that are sent to the device will be ignored. When the $\overline{CS}$ pin is deasserted, the SPRL bit in the Status Register will be modified, and the WEL bit in the Status Register will be reset back to a logical “0”. The complete one byte of data must be clocked into the device before the CS# pin is deasserted; otherwise, the device will abort the operation, the state of the SPRL bit will not change, and the WEL bit in the Status Register will be reset back to the logical “0” state.

If the $\overline{WP}$ pin is asserted, then the SPRL bit can only be set to a logical “1”. If an attempt is made to reset the SPRL bit to a logical “0” while the $\overline{WP}$ pin is asserted, then the Write Status Register command will be ignored, and the WEL bit in the Status Register will be reset back to the logical “0” state. In order to reset the SPRL bit to a logical “0”, the $\overline{WP}$ pin must be deasserted.

Figure 10-2. Write Status Register



11. Other Commands and Functions

11.1 Read Manufacturer and Device ID

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in system. The identification method and the command opcode comply with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC defined Manufacturer ID, the vendor specific Device ID, and the vendor specific Extended Device Information.

To read the identification information, the $\overline{CS}$ pin must first be asserted and the opcode of 9Fh must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte that will be output will be the Manufacturer ID followed by two bytes of Device ID information. The fourth byte output will be the Extended Device Information String Length, which will be 00h indicating that no Extended Device Information follows. After the Extended Device Information String Length byte is output, the SO pin will go into a high-impedance state; therefore, additional clock cycles will have no affect on the SO pin and no data will be output. As indicated in the JEDEC standard, reading the Extended Device Information String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin will terminate the Manufacturer and Device ID read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

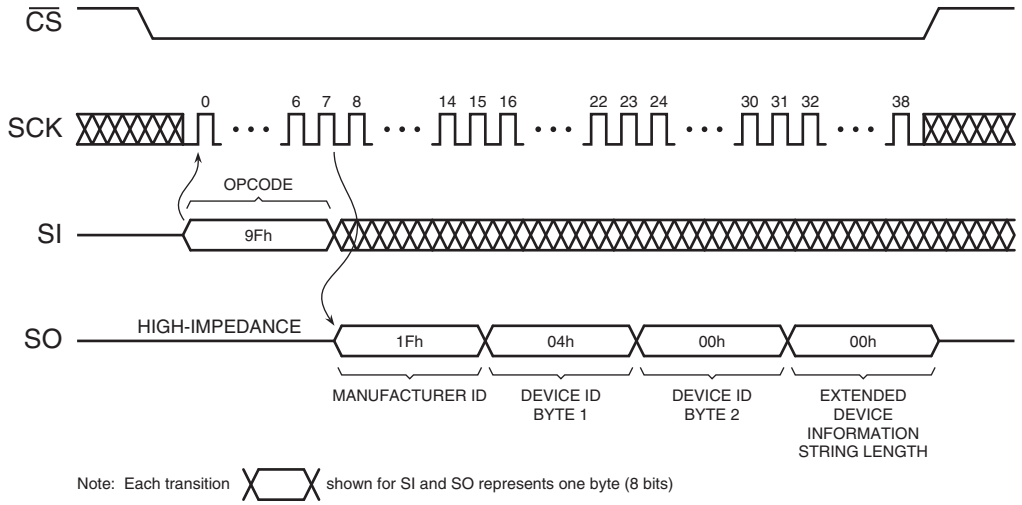
Table 11-1. Manufacturer and Device ID Information

Byte No.	Data Type	Value
1	Manufacturer ID	1FH
2	Device ID (Part 1)	04H
3	Device ID (Part 2)	00H
4	Extended Device Information String Length	00H

Table 11-2. Manufacturer and Device ID Details

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1FH	JEDEC Code: 0001 1111 (1FH for Atmel)
	0	0	0	1	1	1	1	1		
Device ID (Part 1)	Family Code			Density Code					04H	Family Code: 000 (AT26Fxxx series) Density Code: 00100 (4-Mbit)
	0	0	0	0	0	1	0	0		
Device ID (Part 2)	MLC Code			Product Version Code					00H	MLC Code: 000 (1-bit/cell technology) Product Version: 00000 (Initial version)
	0	0	0	0	0	0	0	0		

Figure 11-1. Read Manufacturer and Device ID



11.2 Deep Power-down

During normal operation, the device will be placed in the standby mode to consume less power as long as the $\overline{CS}$ pin remains deasserted and no internal operation is in progress. The Deep Power-down command offers the ability to place the device into an even lower power consumption state called the Deep Power-down mode.

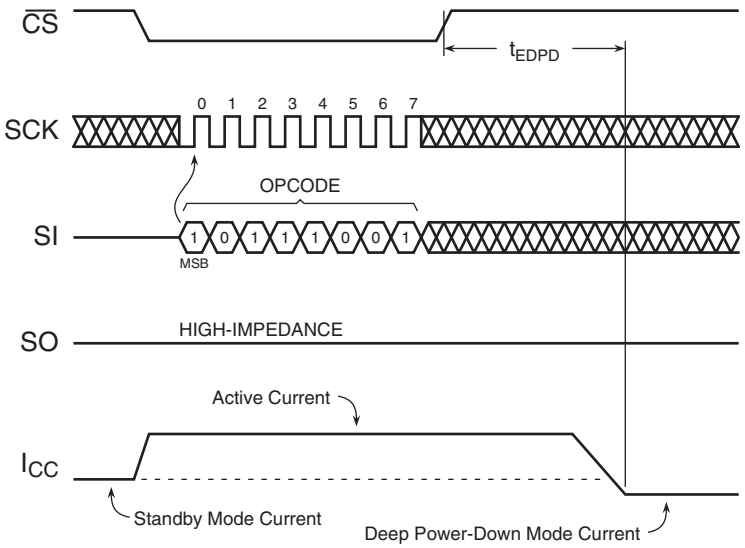
When the device is in the Deep Power-down mode, all commands including the Read Status Register command will be ignored with the exception of the Resume from Deep Power-down command. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode of B9h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Deep Power-down mode within the maximum time of t_{EDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power-cycle or a device reset.

The Deep Power-down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-down mode.

Figure 11-2. Deep Power-down



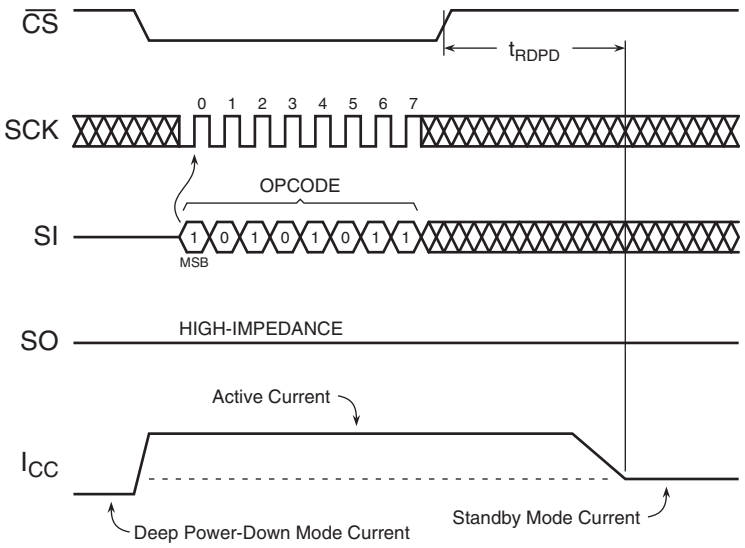
11.3 Resume from Deep Power-down

In order exit the Deep Power-down mode and resume normal device operation, the Resume from Deep Power-down command must be issued. The Resume from Deep Power-down command is the only command that the device will recognize while in the Deep Power-down mode.

To resume from the Deep Power-down mode, the $\overline{CS}$ pin must first be asserted and opcode of ABh must be clocked into the device. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will exit the Deep Power-down mode within the maximum time of t_{RDPD} and return to the standby mode. After the device has returned to the standby mode, normal command operations such as Read Array can be resumed.

If the complete opcode is not clocked in before the $\overline{CS}$ pin is deasserted, then the device will abort the operation and return to the Deep Power-down mode.

Figure 11-3. Resume from Deep Power-down



11.4 Hold

The $\overline{\text{HOLD}}$ pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an affect on any internally self-timed operations such as a program or erase cycle. Therefore, if an erase cycle is in progress, asserting the $\overline{\text{HOLD}}$ pin will not pause the operation, and the erase cycle will continue until it is finished.

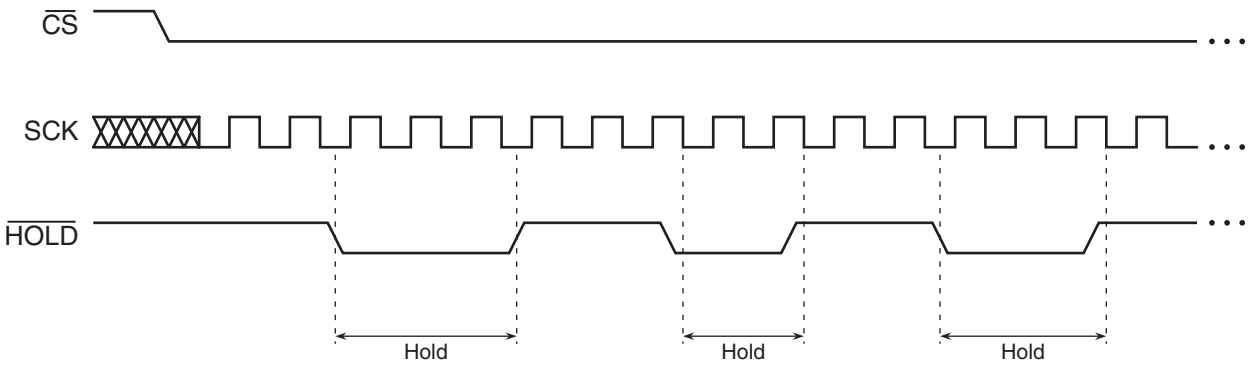
The Hold mode can only be entered while the $\overline{\text{CS}}$ pin is asserted. The Hold mode is activated simply by asserting the $\overline{\text{HOLD}}$ pin during the SCK low pulse. If the $\overline{\text{HOLD}}$ pin is asserted during the SCK high pulse, then the Hold mode won't be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the $\overline{\text{HOLD}}$ pin and $\overline{\text{CS}}$ pin are asserted.

While in the Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The $\overline{\text{WP}}$ pin, however, can still be asserted or deasserted while in the Hold mode.

To end the Hold mode and resume serial communication, the $\overline{\text{HOLD}}$ pin must be deasserted during the SCK low pulse. If the $\overline{\text{HOLD}}$ pin is deasserted during the SCK high pulse, then the Hold mode won't end until the beginning of the next SCK low pulse.

If the $\overline{\text{CS}}$ pin is deasserted while the $\overline{\text{HOLD}}$ pin is still asserted, then the Hold mode will abort and the device may abort the current operation depending on whether or not a complete opcode, address bytes, or data byte was already clocked into the device before the Hold mode was entered. The WEL bit in the Status Register will be reset back to a logical “0” if a program, erase, Protect Sector, Unprotect Sector, or Write Status Register operation aborts as a result of the Hold mode aborting.

Figure 11-4. Hold Mode



12. Electrical Specifications

12.1 Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +4.1V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.2 DC and AC Operating Range

		AT26F004
Operating Temperature (Case)	Industrial	-40° C to 85° C
V_{CC} Power Supply		2.7V to 3.6V

12.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$ = V_{CC}, all inputs at CMOS levels		25	35	µA
I_{DPD}	Deep Power-down Current	$\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$ = V_{CC}, all inputs at CMOS levels		20	25	µA
I_{CC1}	Active Current, Read Operation	f = 33 MHz; I_{OUT} = 0 mA; $\overline{CS}$ = V_{IL}, V_{CC} = Max		8	12	mA
		f = 20 MHz; I_{OUT} = 0 mA; $\overline{CS}$ = V_{IL}, V_{CC} = Max		7	10	
I_{CC2}	Active Current, Program Operation	$\overline{CS}$ = V_{CC}, V_{CC} = Max		9	12	mA
I_{CC3}	Active Current, Erase Operation	$\overline{CS}$ = V_{CC}, V_{CC} = Max		9	12	mA
I_{LI}	Input Leakage Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	V_{OUT} = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = Min			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

12.4 AC Characteristics

Symbol	Parameter	Min	Max	Units
f_{SCK}	Serial Clock (SCK) Frequency		33	MHz
f_{RDLF}	SCK Frequency for Read Array (Low Frequency – 03h opcode)		20	MHz
t_{SCKH}	SCK High Time	13 20[1]		ns
t_{SCKL}	SCK Low Time	13 20[1]		ns
t_{SCKR}[2]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1		V/ns
t_{SCKF}[2]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1		V/ns
t_{CSH}	Chip Select High Time	50		ns
t_{CSLS}	Chip Select Low Setup Time (relative to SCK)	5		ns
t_{CSLH}	Chip Select Low Hold Time (relative to SCK)	5 12[3]		ns
t_{CSHS}	Chip Select High Setup Time (relative to SCK)	5		ns
t_{CSHH}	Chip Select High Hold Time (relative to SCK)	5		ns
t_{DS}	Data In Setup Time	3		ns
t_{DH}	Data In Hold Time	3		ns
t_{OH}	Output Hold Time	0		ns
t_{DIS}[2]	Output Disable Time		10	ns
t_V	Output Valid Time		12 18[1]	ns
t_{HLS}	$\overline{HOLD}$ Low Setup Time (relative to SCK)	5		ns
t_{HLH}	$\overline{HOLD}$ Low Hold Time (relative to SCK)	5		ns
t_{HHS}	$\overline{HOLD}$ High Setup Time (relative to SCK)	5		ns
t_{HHH}	$\overline{HOLD}$ High Hold Time (relative to SCK)	5		ns
t_{HLQZ}[2]	$\overline{HOLD}$ Low to Output High-Z		9	ns
t_{HHQX}[2]	$\overline{HOLD}$ High to Output Low-Z		9	ns
t_{WPS}[2][4]	Write Protect Setup Time	20		ns
t_{WPH}[2][4]	Write Protect Hold Time	100		ns
t_{SECP}[2]	Sector Protect Time (from Chip Select High)		20	ns
t_{SECUP}[2]	Sector Unprotect Time (from Chip Select High)		20	ns
t_{EDPD}[2]	Chip Select High to Deep Power-down		3	µs
t_{RDPD}[2]	Chip Select High to Standby Mode		3	µs

Notes:
1. Specification only applies when using the 03h Read Array (Low Frequency) command.
2. Not 100% tested (value guaranteed by design and characterization).
3. Specification only applies when using the SPI Mode 3 timing.
4. Only applicable as a constraint for the Write Status Register command when SPRL = 1.

12.5 Program and Erase Characteristics

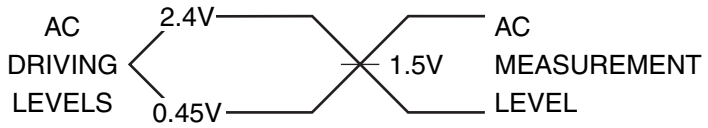
Symbol	Parameter		Min	Typ	Max	Units
t_{BP}	Byte Program Time			15		µs
t_{PP}	Page Program Time (256 Bytes Using Sequential Program Mode)				5	ms
t_{BLKE}	Block Erase Time	4-Kbyte		0.1	0.35	sec.
		32-Kbyte		0.38	0.65	
		64-Kbyte		0.75	1.0	
t_{CHPE}	Chip Erase Time			6	10	sec.
t_{WRSR} [1]	Write Status Register Time				200	ns

Note: 1. Not 100% tested (value guaranteed by design and characterization).

12.6 Power-Up Conditions

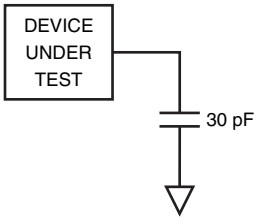
Parameter	Min	Max	Units
Minimum V_{CC} to Chip Select Low Time	50		µs
Power-up Device Delay Before Program or Erase Allowed		10	ms
Power-on Reset Voltage	1.5	2.5	V

12.7 Input Test Waveforms and Measurement Levels



t_R, t_F < 2 ns (10% to 90%)

12.8 Output Test Load



13. AC Waveforms

Figure 13-1. Serial Input Timing

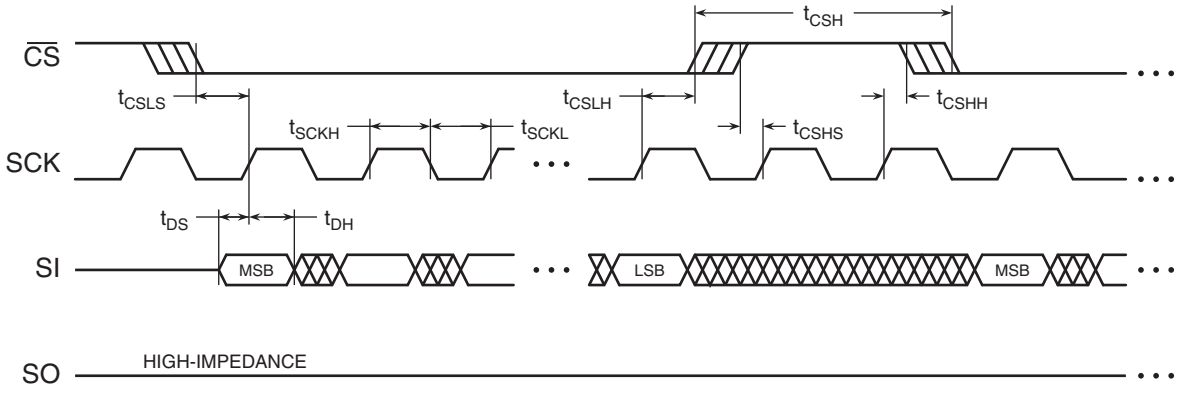


Figure 13-2. Serial Output Timing

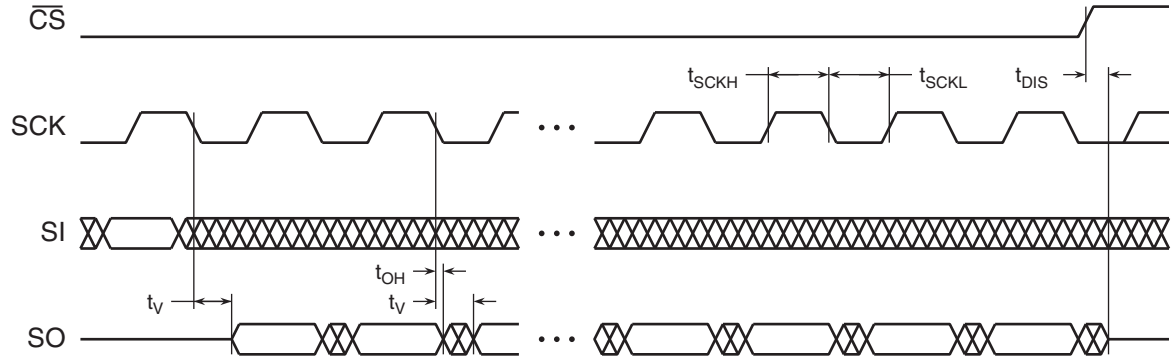


Figure 13-3. HOLD Timing – Serial Input

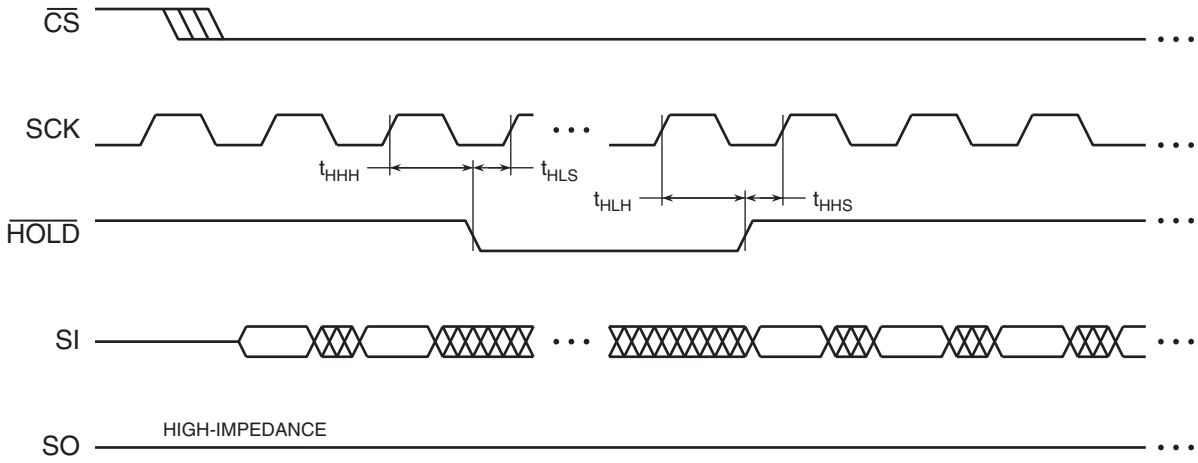


Figure 13-4. $\overline{\text{HOLD}}$ Timing – Serial Output

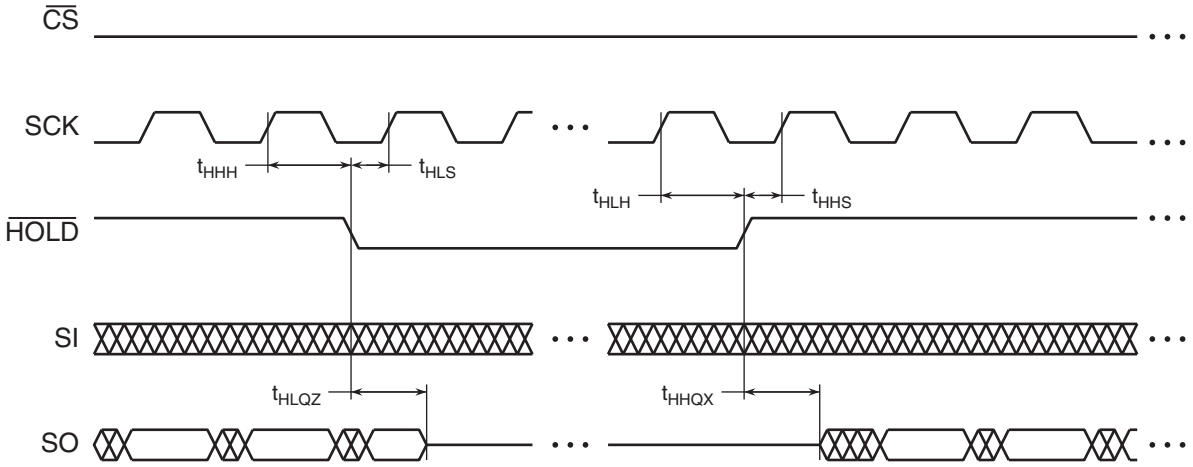
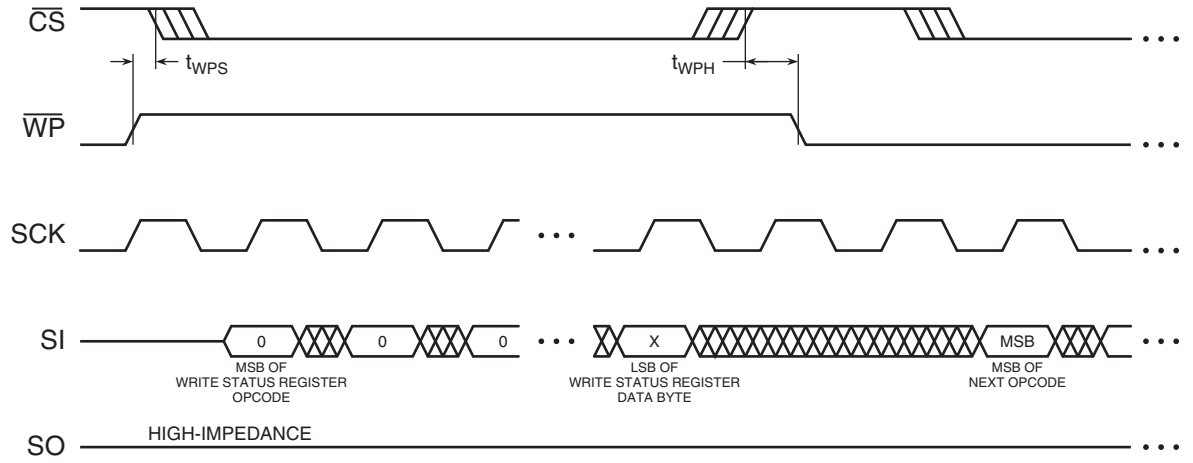


Figure 13-5. $\overline{\text{WP}}$ Timing for Write Status Register Command When SPRL = 1



14. Ordering Information

14.1 Green Package Options (Pb/Halide-free/RoHS Compliant)

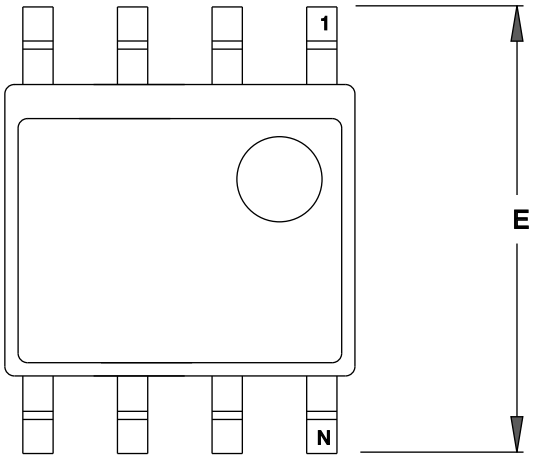
f_{SCK} (MHz)	Ordering Code	Package	Operation Range
33	AT26F004-SSU	8S1	Industrial (-40° C to 85° C)
	AT26F004-SU	8S2	
	AT26F004-MU[1]	8M1-A	

Note: 1. Contact Atmel for availability.

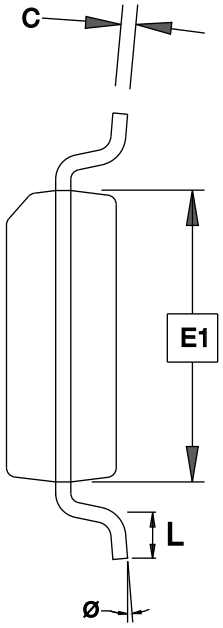
Package Type	
8S1	8-lead, 0.150” Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.208” Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8M1-A	8-pad, 6 x 5 x 1.00 mm Very Thin Micro Lead-frame Package (MLF)

15. Packaging Information

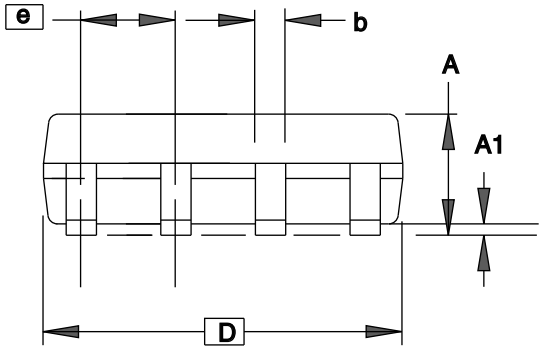
15.1 8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

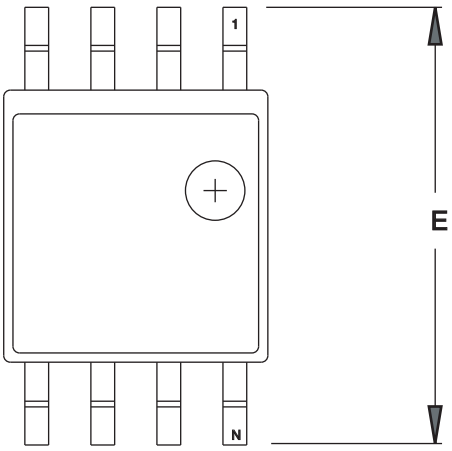
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

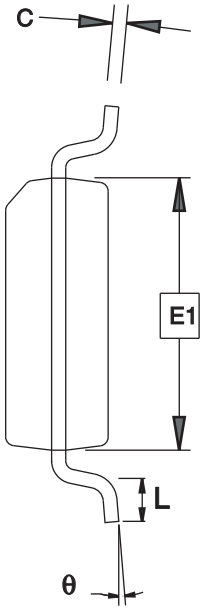
3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

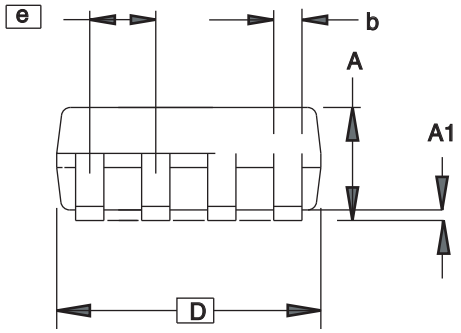
15.2 8S2 – EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

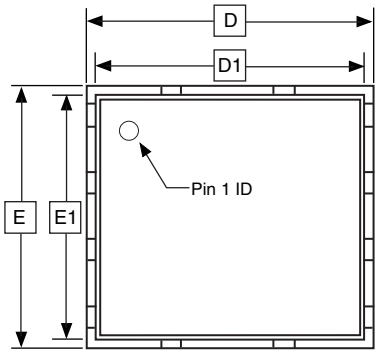
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			3

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

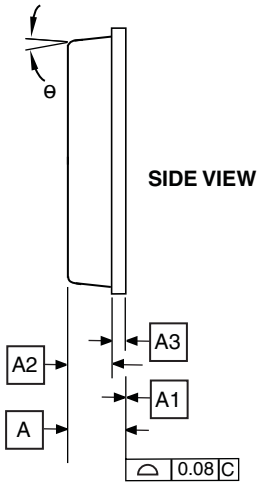
4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8S2,** 8-lead, 0.208” Body, Plastic Small Outline Package (EIAJ)	STN	8S2	F

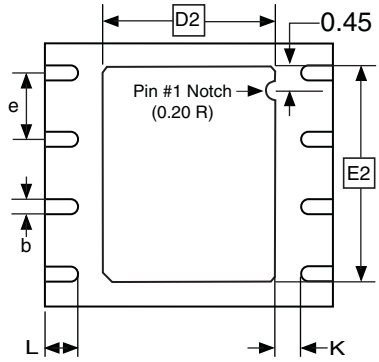
15.3 8M1-A – MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.85	1.00	
A1	–	–	0.05	
A2		0.65 TYP		
A3		0.20 TYP		
b	0.35	0.40	0.48	
D	5.90	6.00	6.10	
D1	5.70	5.75	5.80	
D2	3.20	3.40	3.60	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	3.80	4.00	4.20	
e		1.27		
L	0.50	0.60	0.75	
θ	–	–	12°	
K	0.25	–	–	

8/28/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8M1-A,** 8-pad, 6 x 5 x 1.00 mm Body, Thermally Enhanced Plastic Very Thin Dual Flat No Lead Package (VDFN)	YBR	8M1-A	D

16. Revision History

Revision Level – Release Date	History
A – October 2005	Initial release.
B – January 2006	Changed t_{CSLH} parameter for SPI Mode 3 timing
C – April 2006	Changed Note 5 of 8S2 package drawing to generalize terminal plating comment.
D – October 2008	No longer recommended for new designs. For new designs use AT25DF041A.

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