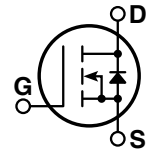
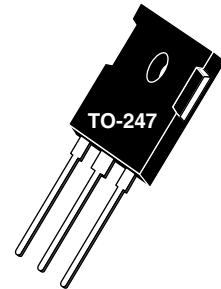


POWER MOS V®

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **Avalanche Energy Rated**
- **Lower Leakage**
- **Popular TO-247 Package**


MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT1201R5BVFR_SVFR	UNIT
V_{DSS}	Drain-Source Voltage	1200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	10	Amps
I_{DM}	Pulsed Drain Current ^①	40	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	370	Watts
	Linear Derating Factor	2.96	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	10	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	1200			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 5A$)			1.500	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1200V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1\text{mA}$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT1201R5BVFR_SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		3700	4440	pF
C _{oss}	Output Capacitance			320	450	
C _{riss}	Reverse Transfer Capacitance			150	225	
Q _g	Total Gate Charge ^③	V _{GS} = 10V V _{DD} = 600V I _D = 10A @ 25°C		190	285	nC
Q _{gs}	Gate-Source Charge			16	24	
Q _{gd}	Gate-Drain ("Miller") Charge			90	135	
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V V _{DD} = 600V I _D = 10A @ 25°C R _G = 1.6Ω		12	24	ns
t _r	Rise Time			10	20	
t _{d(off)}	Turn-off Delay Time			50	75	
t _f	Fall Time			14	28	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			10	Amps
I _{SM}	Pulsed Source Current ^① (Body Diode)			40	
V _{SD}	Diode Forward Voltage ^② (V _{GS} = 0V, I _S = -I _D 10A)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			18	V/ns
t _{rr}	Reverse Recovery Time (I _S = -I _D 10A, di/dt = 100A/μs)	T _j = 25°C		250	ns
		T _j = 125°C		430	
Q _{rr}	Reverse Recovery Charge (I _S = -I _D 10A, di/dt = 100A/μs)	T _j = 25°C		1.0	μC
		T _j = 125°C		2.5	
I _{RRM}	Peak Recovery Current (I _S = -I _D 10A, di/dt = 100A/μs)	T _j = 25°C		11	Amps
		T _j = 125°C		17	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.34	°C/W
R _{θJA}	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ SStarting T_j = +25°C, L = 26mH, R_G = 25Ω, Peak I_L = 10A

⑤ I_S ≤ I_D 10A, di/dt = 100A/μs, T_j ≤ 150°C, R_G = 2.0Ω V_R = 1200V.

APT Reserves the right to change, without notice, the specifications and information contained herein.

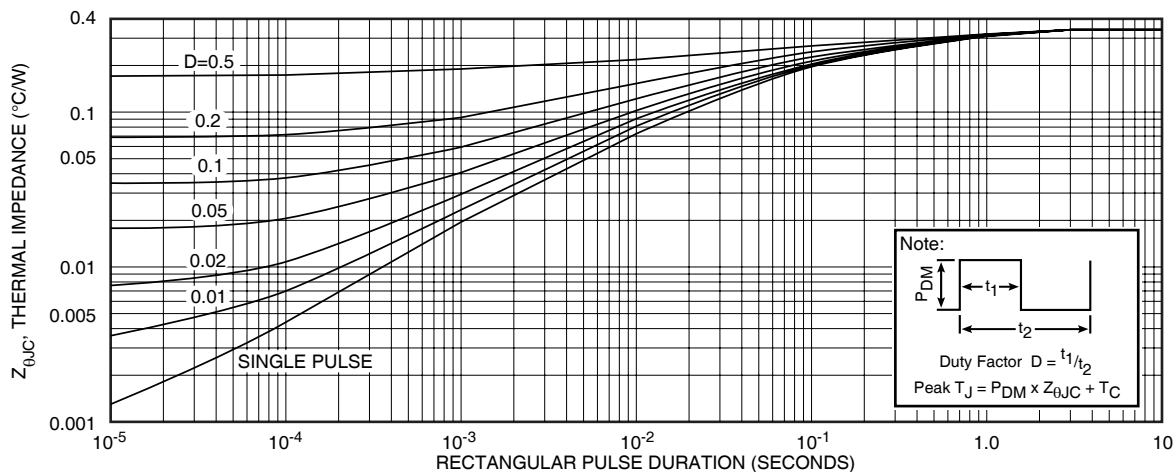


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

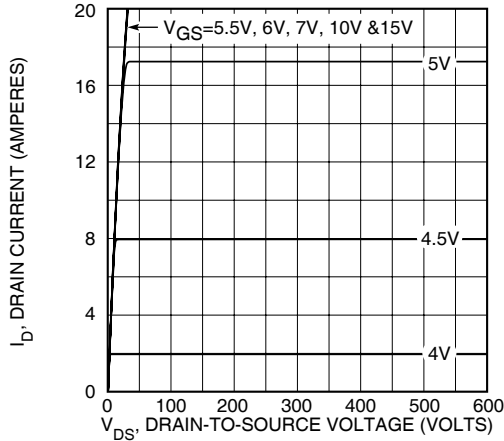


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

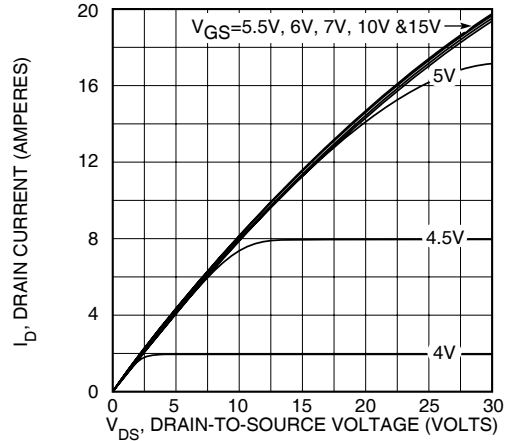


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

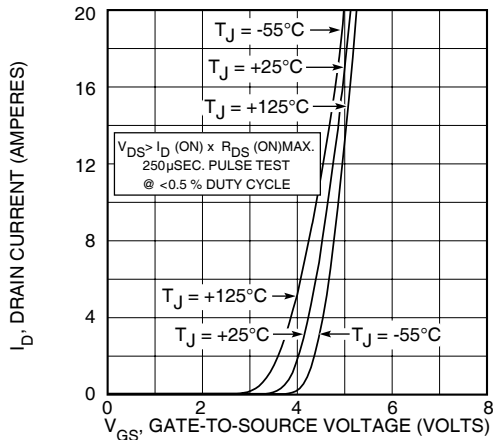


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

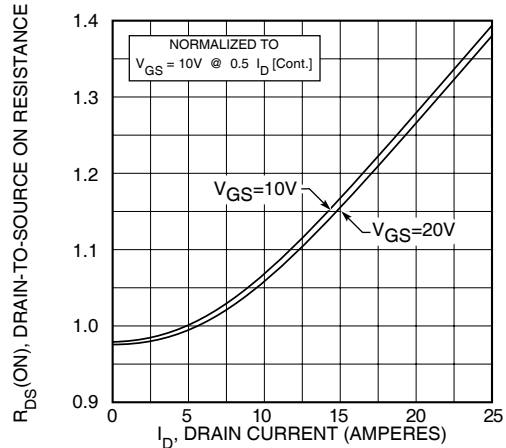


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

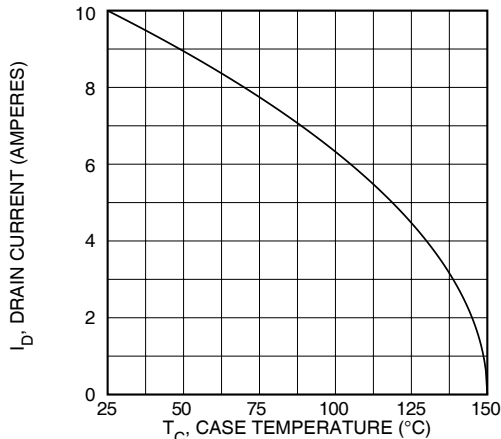


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

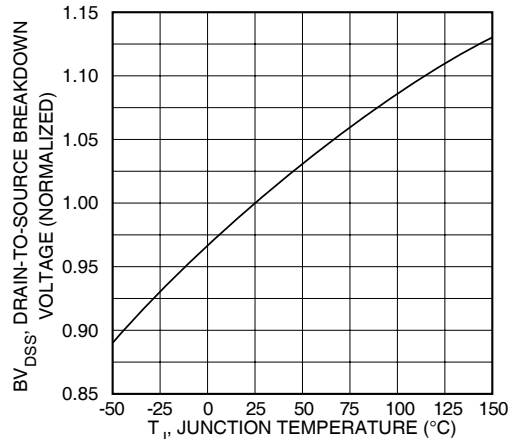


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

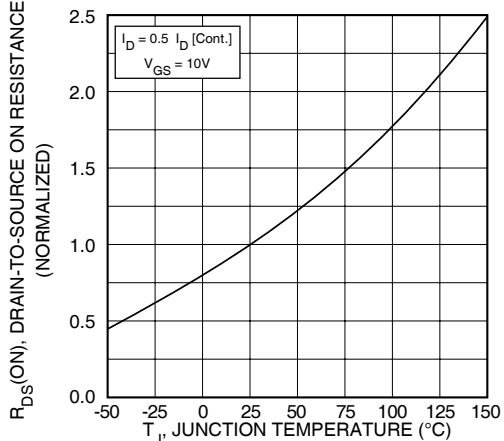


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

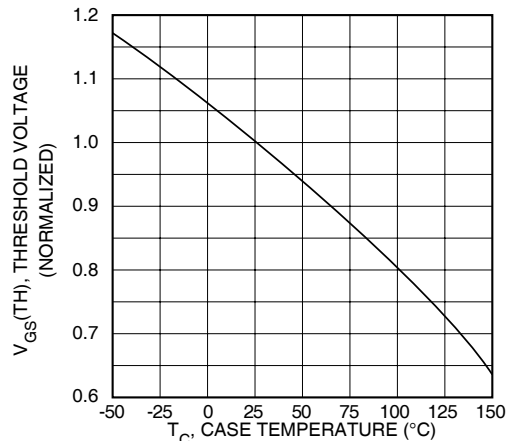


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

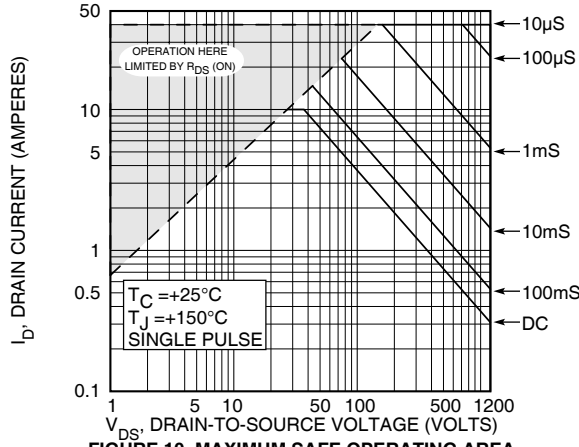


FIGURE 10, MAXIMUM SAFE OPERATING AREA

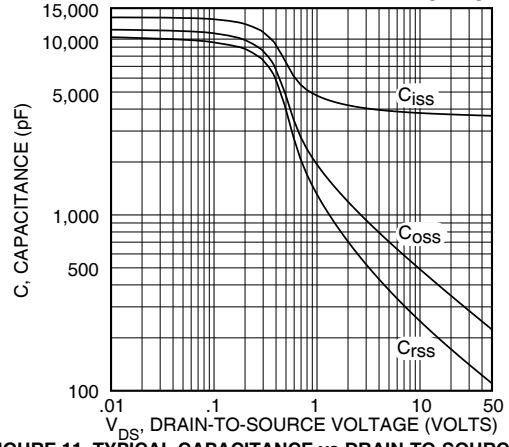


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

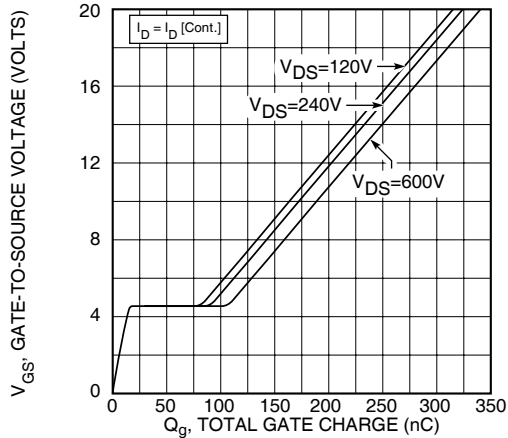


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

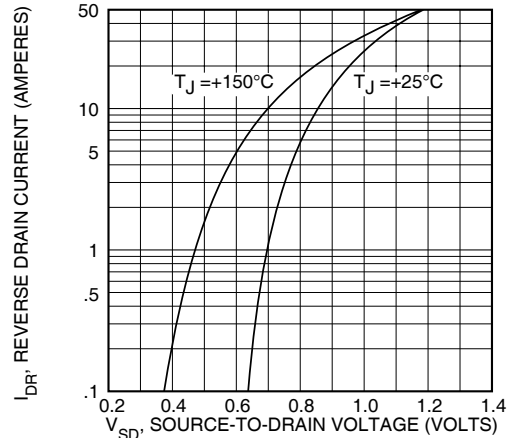
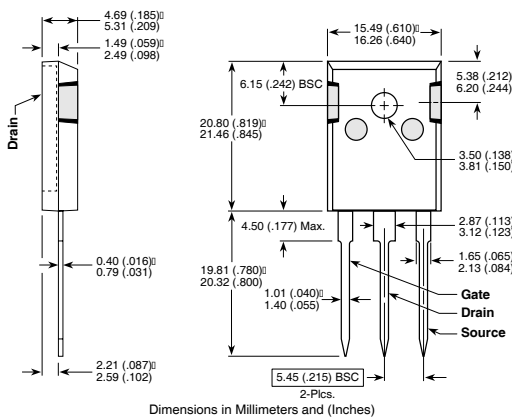


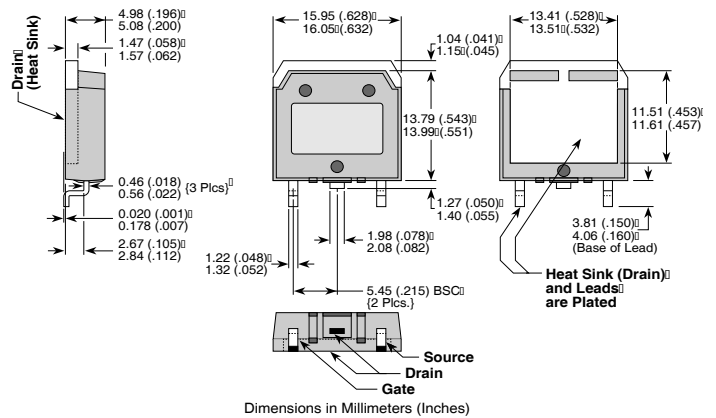
FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline



Dimensions in Millimeters and (Inches)

D³PAK Package Outline



Dimensions in Millimeters (Inches)

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522

5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.