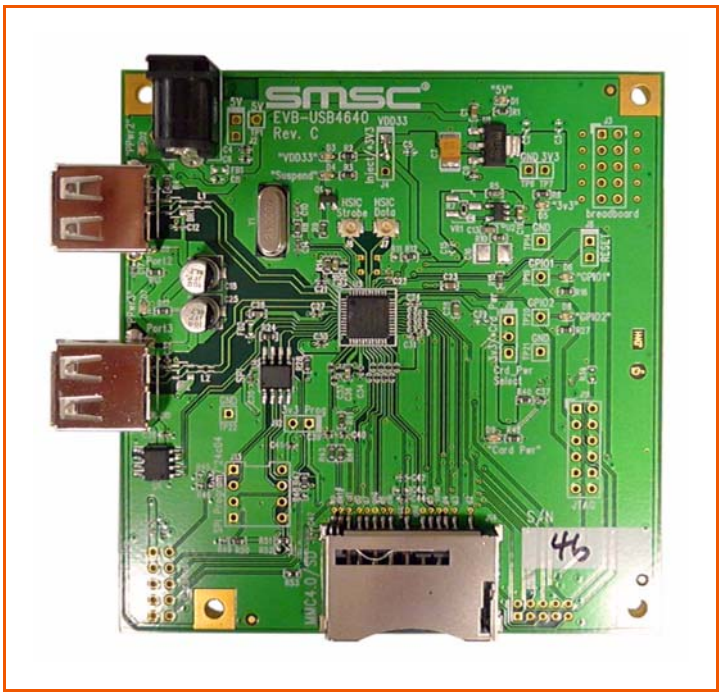
EVB-USB4640 Evaluation Board Revision C



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Chapter 1 Overview

EVB-USB4640 Revision C Evaluation Board is for the SMSC USB4640 Hi-Speed HSIC USB hub and card reader combo solution. It has an upstream port compliant to HSIC 1.0, a supplement to the USB 2.0 Specification. It also has two downstream ports that are compliant with the USB 2.0 Specification. The goal of the EVB-USB4640 is to provide an application platform for developers of the following applications: Flash Media Card Reader/Writer, printers, desktop and mobile PCs, consumer A/V, flat panel displays, and 3G/4G handsets, smartphones, cell phones, and other mobile devices. The EVB-USB4640 demonstrates driver compatibility with Microsoft Vista, Windows XP, Windows ME, Windows 2K SP4, Mac OSx, and Linux Mass Storage Class Drivers.

1.1 Features

- The USB4640 in a 48-Pin QFN RoHS compliant package
- Support for the following media types (sub-set of the USB4640):
  Secure Digital™ (SD)
  MultiMedia Card™ (MMC) 4 and 8 bit interfaces
- One HSIC 1.0 upstream hub port using dual UFL connectors
- Two USB 2.0 downstream hub ports with individual port power and over current sense
- External SPI FLASH for external downloadable firmware
- External I^2C EEPROM for configuration options
- Low-cost 4-layer space saving design
- Operates from a single voltage (+5.0 V, regulated) 'wall wart' external power supply
- Internal FET power switch for all media types
- Activity LED indicator
- Card power LED indicator
- Single crystal clock source
- Single onboard +3.3 V regulator
- Single onboard +1.2 V regulator
- +3.3 V and +5 V power LED indicators
- Suspend and port power LED indicators

1.2 General Description

The EVB-USB4640 is a demonstration and evaluation platform featuring the USB4640 Ultra Fast interface between an HSIC enabled host and current popular flash media formats on a 4-layer RoHS-compliant printed circuit board. The EVB-USB4640 should be connected to the upstream HSIC host via the HSIC Strobe and Data mini coax connectors, J6 and J7, through Male to Male, 50 Ω, shielded U.FL cables. It is designed to support internal default settings and either an external I^2C EEPROM for customized functionality or SPI FLASH for external firmware.

An 8-Mbit SPI FLASH device is populated on the evaluation board to provide firmware updates via an onboard programming socket J13.

The default configuration can be changed by adding an EEPROM into the provided socket. However, the SPI FLASH device must first be removed. Figure 1.1 shows the top and bottom level silk screen and copper layer.

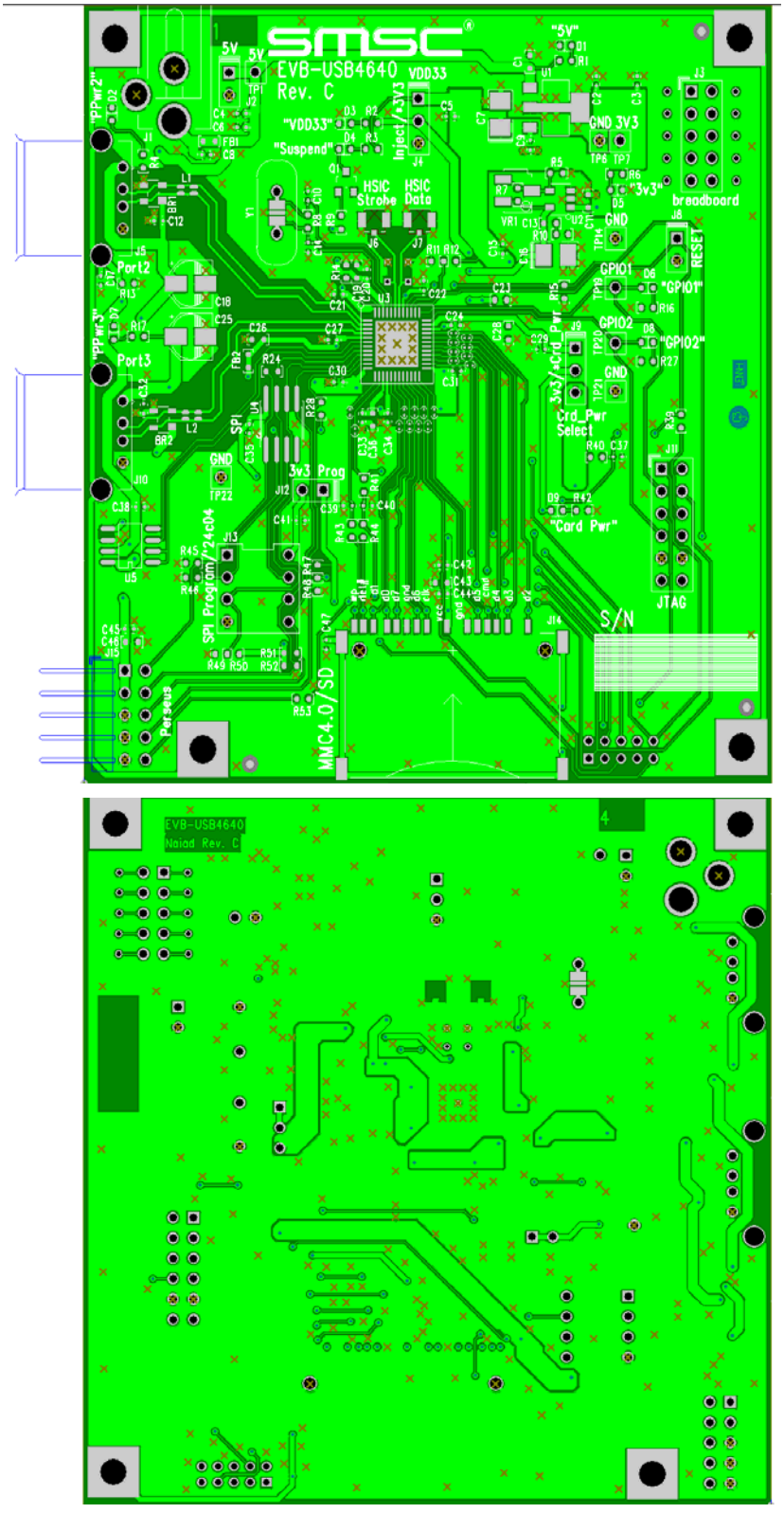

Figure 1.1 Top and Bottom Level Silk Screen and Copper Layers

Chapter 2 Getting Started

The EVB-USB4640 is configured by internal default registers. In the default configuration, it operates as a USB 2.0 combo device with a three port USB HUB (two external ports) and a Flash Media Controller with SMSC standard VID/PID/DID settings.

2.1 Configuration

The SMSC EVB-USB4640 is designed for flexible configuration solutions. It can operate with the default internal register settings, or may be programmed via USB host downloadable configuration EEPROM, or downloadable external firmware to a SPI FLASH via the onboard programming socket.

2.1.1 Configuration source - Internal default

When the USB4640 does not detect an EEPROM or a valid SPI FLASH image upon power-up, the EVB-USB4640 uses internal default register settings; it sets the Vendor ID, Product ID, Language ID, and Device ID, and a few other choices from internal ROM code.

2.1.2 Configuration source - External SMBus

Upon power-up, the USB4640 searches for an attached EEPROM on the I^2C interface. The EVB-USB4640 provides an 8-pin DIP socket J13 for an external EEPROM IC (U6) of type 24C04B to customize the Media Controller's settings. The EEPROM contains 512 bytes of user customizable settings. Among the settings are Vendor ID, Product ID, and Device ID numbers. See Table 2.1 for all SMBus component population options. To use EEPROM, the SPI FLASH components must first be removed. These include the SPI chip U4 and both 0 Ω series SPI resistors R24 and R28 which will isolate the SMBus. Also, the following SMBus components must be populated:

- SPI programming socket J13
- 10 kΩ pull-down resistors R45 and R46
- 0 Ω pull-down resistors R48 and R49
- 1 kΩ pull-up resistor R51
- 10 kΩ pull-up resistor R52.

Note: If the "3v3 Prog" header J12 has been installed, this header must be shorted. Install the EEPROM device U6 into socket J13 to use.

To use I^2C, the same setup above applies. However, the EEPROM device U6 must now be removed if installed. Instead, use the open socket J13 pins 5 (SI), 6 (SCK), 7 (GND through 0 Ω pull-down resistors), and 8 (VCC) for I^2C communication.

2.1.3 Configuration source - External SPI FLASH

The installed SPI FLASH is initially blank. In this scenario the internal firmware will execute. There are several SPI FLASH options. For all options, the SPI chip U4 must be populated as well as both 0 Ω series SPI resistors, R24 and R28. The following SMBus components must be removed:

- 10 kΩ pull-down resistors R45 and R46
- 10 kΩ pull-up resistor R52
- EEPROM device U6
- 0 Ω pull-down resistors R48 and R49

See Table 2.1 for all SPI FLASH component population options.

The default configuration is populated with a 60 MHz SPI on the EVB. This means that the 1 kΩ pull-up resistor R51 must also be populated. If a 30 MHz SPI chip is populated instead, then the 1 kΩ pull-up resistor R51 must be removed. This is the speed select resistor and it is internally pulled low in the USB4640 to set the 30 MHz mode. When using onboard SPI, make sure there is either a trace shorting pins 1 and 2 of the “3v3 Prog” header J12, or if this header is installed, make sure that it is shorted to supply 3.3 V to the onboard SPI chip.

The SPI FLASH can be programmed onboard using the J13 8-pin DIP socket. For SPI configuration, this socket only needs to be installed when programming SPI FLASH. In order to use this socket for programming, cut the trace shorting pins 1 and 2 on the “3v3 Prog” header J12. Then populate the 1x2 header (J12) and “RESET” header J8. To program the SPI, hold the board in reset by shorting the “RESET” jumper while programming the SPI through the J13 programming socket. This will tri-state the SPI pins on the USB while the onboard SPI is being programmed. The “3v3 Prog” header must be left open during programming to isolate the board power from the programmer power.

After programming is complete, the “RESET” header J8 must be left open and the “3v3 Prog” header must be shorted to supply 3.3 V to the onboard SPI chip. After downloading, the USB4640 will execute out of the SPI FLASH.

2.1.4 Configuration Source - Memory Component Configuration Table

Follow the population options in the table below for the various configuration sources described above.

Table 2.1 Memory Component Configuration

	SPI OPTIONS			SMBUS OPTIONS	
COMPONENTS	**60MHZ (DEFAULT)**	**30MHZ**	**PROGRAMMING SOCKET**	**EEPROM**	**I^2C**
U4	Populate	Populate	Populate	DNP	DNP
U6	DNP	DNP	DNP	Populate	DNP
J12	DNP	DNP	Populate	DNP	DNP
J13	DNP	DNP	Populate	Populate	Populate
R24	Populate	Populate	Populate	DNP	DNP
R28	Populate	Populate	Populate	DNP	DNP
R45	DNP	DNP	DNP	Populate	Populate
R46	DNP	DNP	DNP	Populate	Populate
R48	DNP	DNP	DNP	Populate	Populate
R49	DNP	DNP	DNP	Populate	Populate
R51	Populate	DNP	DNP	Populate	Populate
R52	DNP	DNP	DNP	Populate	Populate

2.1.5 Power Source - Self Powered

The EVB-USB4640 only supports self powered operation. The EVB-USB4640 is powered through a +5.0 V regulated 'wall wart' external power supply.

2.1.6 Configuration Source - USB Upstream

The EEPROM supporting the EVB-USB4640 is configured by connecting the upstream port to a qualified HSIC host or USB to HSIC bridge device. Once connected, the EEPROM can be configured with the SMSC configuration tool, USBDM. USBDM allows for modification of Vendor ID, Product ID, Language ID, Device ID, and configuration settings as shown in Figure 2.1.

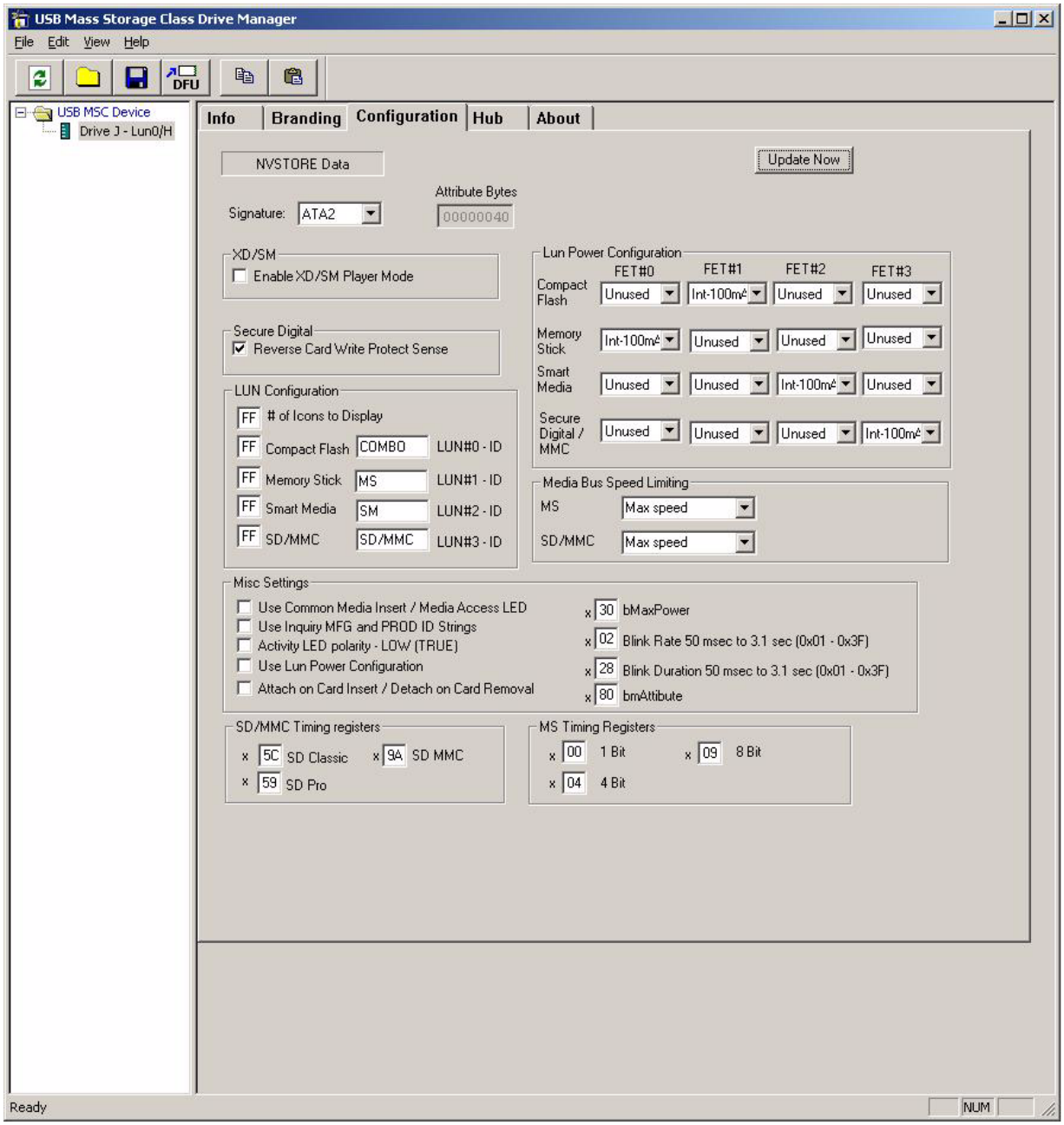

Figure 2.1 USBDM Configuration Interface