MCP14A0153/4/5

1.5A Dual MOSFET Driver with Low Threshold Input and Enable

Features

- High Peak Output Current: 1.5A (typical)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - 1000 pF in 11.5 ns (typical)
- Short Delay Times: 25 ns (t_{D1}), 24 ns (t_{D2}) (typical)
- Low Supply Current: 750 µA (typical)
- Low-Voltage Threshold Input and Enable with Hysteresis
- Latch-up Protected: Withstands 500 mA Reverse Current
- Space-Saving Packages:
  - 8-Lead MSOP
  - 8-Lead SOIC
  - 8-Lead 2x3 TDFN

Applications

- Switch-Mode Power Supplies (SMPS)
- Pulse Transformer Drive
- Line Drivers
- Level Translator
- Motor and Solenoid Drive

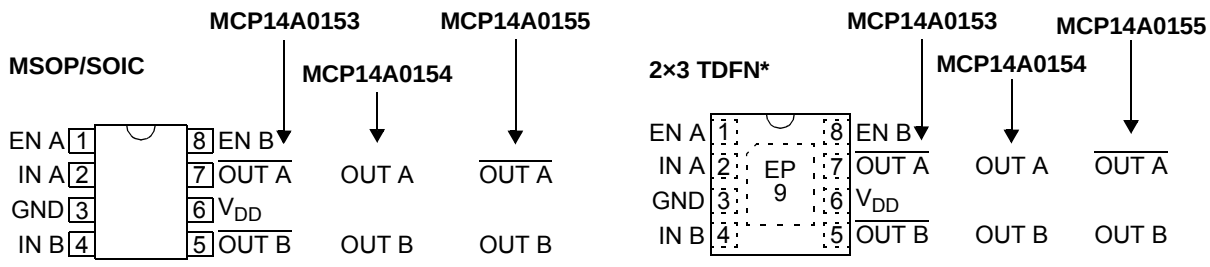
General Description

The MCP14A0153/4/5 devices are high-speed dual MOSFET drivers that are capable of providing up to 1.5A of peak current while operating from a single 4.5V to 18V supply. There are three output configurations available: dual inverting (MCP14A0153), dual non-inverting (MCP14A0154) and complementary (MCP14A0155). These devices feature low shoot-through current, matched rise and fall times and short propagation delays, which make them ideal for high switching frequency applications.

The MCP14A0153/4/5 family of devices offers enhanced control with enable functionality. The active-high enable pins can be driven low to drive the corresponding outputs of the MCP14A0153/4/5 low, regardless of the status of the input pin. An integrated pull-up resistor allows the user to leave the enable pins floating for standard operation.

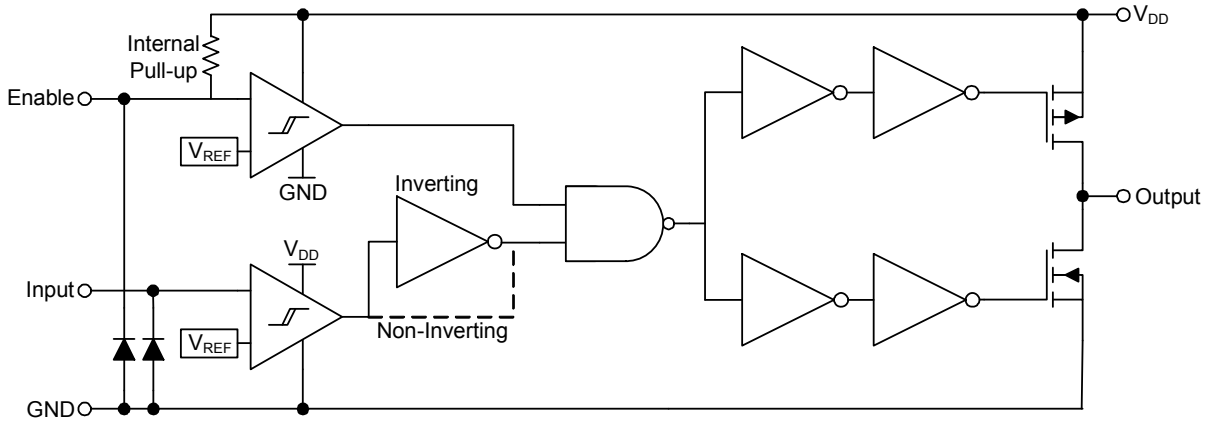
These devices are highly latch-up resistant under any condition within their power and voltage ratings. They can accept up to 500 mA of reverse current being forced back into their outputs without damage or logic upset. All terminals are fully protected against Electrostatic Discharge (ESD), up to 2 kV (HBM) and 200 V (MM).

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP14A0153 Dual Inverting
MCP14A0154 Dual Non-Inverting
MCP14A0155 One Inverting, One Non-Inverting

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}, Supply Voltage.....+20V
V_{IN}, Input Voltage..... (V_{DD} + 0.3V) to (GND – 0.3V)
V_{EN}, Enable Voltage..... (V_{DD} + 0.3V) to (GND – 0.3V)
Package Power Dissipation (T_A = +50°C)
8L MSOP 0.63W
8L SOIC 1.00W
8L 2 x 3 TDFN.....1.86W
ESD Protection on all Pins.....2 kV (HBM)
.....200V (MM)

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND – 0.3	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-1	—	+1	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Pin Pull-up Resistance	R_{ENBL}	—	1.8	—	MΩ	V_{DD} = 18V, EN = GND
Enable Input Current	I_{EN}	—	10	—	µA	V_{DD} = 18V, EN = GND
Propagation Delay	t_{D3}	—	25	32	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3 **(Note 1)**
Propagation Delay	t_{D4}	—	24	31	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3 **(Note 1)**
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	I_{OUT} = 0A
Low Output Voltage	V_{OL}	—	—	0.025	V	I_{OUT} = 0A
Output Resistance, High	R_{OH}	—	4.5	6.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	3.0	4.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V **(Note 1)**
Latch-up Protection Withstand Reverse Current	I_{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 µs **(Note 1)**

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switching Time(1)						
Rise Time	t_R	—	11.5	18.5	ns	V_{DD} = 18V, C_L = 1000 pF, see Figure 4-1 and Figure 4-2 **(Note 1)**
Fall Time	t_F	—	10	17	ns	V_{DD} = 18V, C_L = 1000 pF, see Figure 4-1 and Figure 4-2 **(Note 1)**
Delay Time	t_{D1}	—	25	32	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1 and Figure 4-2 **(Note 1)**
	t_{D2}	—	24	31	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1 and Figure 4-2 **(Note 1)**
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	675	1120	µA	$V_{INA/B}$ = 3V, $V_{ENA/B}$ = 3V
	I_{DD}	—	715	1160	µA	$V_{INA/B}$ = 0V, $V_{ENA/B}$ = 3V
	I_{DD}	—	715	1160	µA	$V_{INA/B}$ = 3V, $V_{ENA/B}$ = 0V
	I_{DD}	—	750	1200	µA	$V_{INA/B}$ = 0V, $V_{ENA/B}$ = 0V

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)(1)

Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	1.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	1.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Input Current	I_{EN}	—	12	—	µA	V_{DD} = 18V, EN = GND
Propagation Delay	t_{D3}	—	28	35	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3
Propagation Delay	t_{D4}	—	27	34	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)(1) (CONTINUED)

Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	9	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	—	6.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	14	21	ns	V_{DD} = 18V, C_L = 1000 pF, T_A = +125°C, see Figure 4-1 and Figure 4-2
Fall Time	t_F	—	13	20	ns	V_{DD} = 18V, C_L = 1000 pF, T_A = +125°C, see Figure 4-1 and Figure 4-2
Delay Time	t_{D1}	—	28	35	ns	V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1 and Figure 4-2
	t_{D2}	—	27	34	ns	V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1 and Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	—	1520	µA	V_{IN} = 3V, V_{EN} = 3V
	I_{DD}	—	—	1560	µA	V_{IN} = 0V, V_{EN} = 3V
	I_{DD}	—	—	1560	µA	V_{IN} = 3V, V_{EN} = 0V
	I_{DD}	—	—	1600	µA	V_{IN} = 0V, V_{EN} = 0V

Note 1: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Comments
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Information						
Junction-to-Ambient Thermal Resistance, 8LD MSOP	θ_{JA}	—	158	—	°C/W	**(Note 1)**
Junction-to-Ambient Thermal Resistance, 8LD SOIC	θ_{JA}	—	99.8	—	°C/W	**(Note 1)**
Junction-to-Ambient Thermal Resistance, 8LD TDFN	θ_{JA}	—	53.7	—	°C/W	**(Note 1)**
Junction-to-Top Characterization Parameter, 8LD MSOP	Ψ_{JT}	—	2.4	—	°C/W	**(Note 1)**
Junction-to-Top Characterization Parameter, 8LD SOIC	Ψ_{JT}	—	5.9	—	°C/W	**(Note 1)**
Junction-to-Top Characterization Parameter, 8LD TDFN	Ψ_{JT}	—	0.5	—	°C/W	**(Note 1)**
Junction-to-Board Characterization Parameter, 8LD MSOP	Ψ_{JB}	—	115.2	—	°C/W	**(Note 1)**
Junction-to-Board Characterization Parameter, 8LD SOIC	Ψ_{JB}	—	64.8	—	°C/W	**(Note 1)**
Junction-to-Board Characterization Parameter, 8L TDFN	Ψ_{JB}	—	24.4	—	°C/W	**(Note 1)**

Note 1: Parameter is determined using a High K 2S2P 4-layer board, as described in JESD 51-7, as well as JESD 51-5 for packages with exposed pads.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

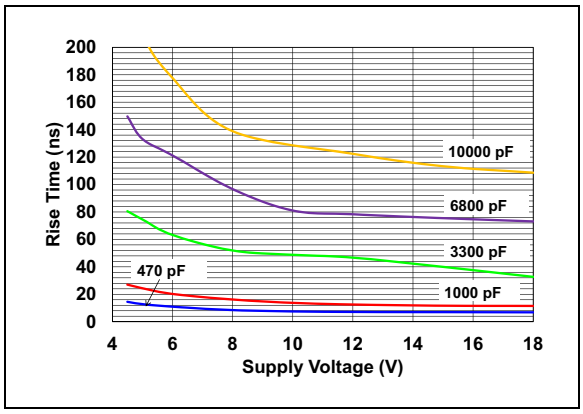


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

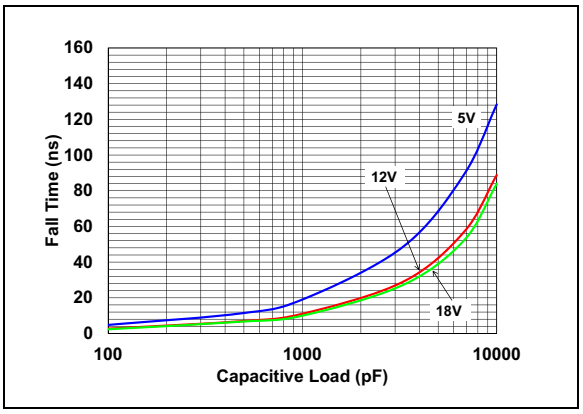


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

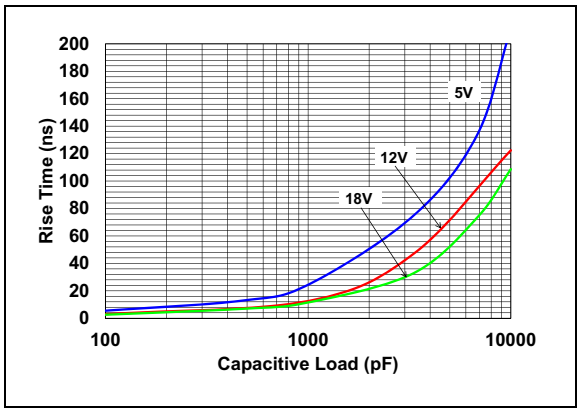


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

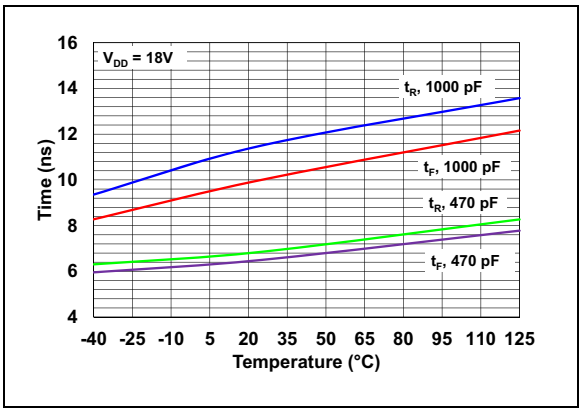


FIGURE 2-5: *Rise and Fall Time vs. Temperature.*

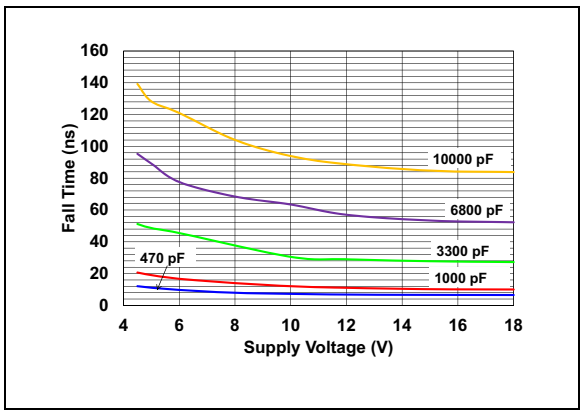


FIGURE 2-3: *Fall Time vs. Supply Voltage.*

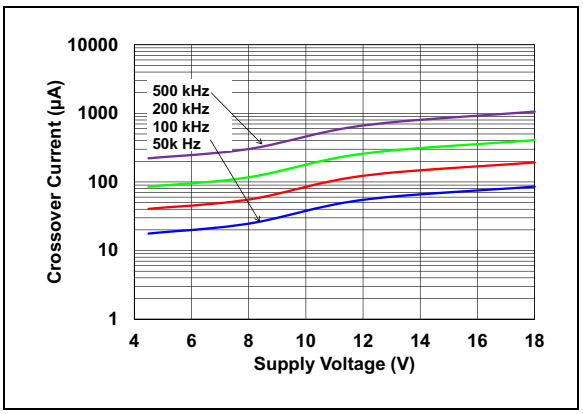


FIGURE 2-6: *Crossover Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

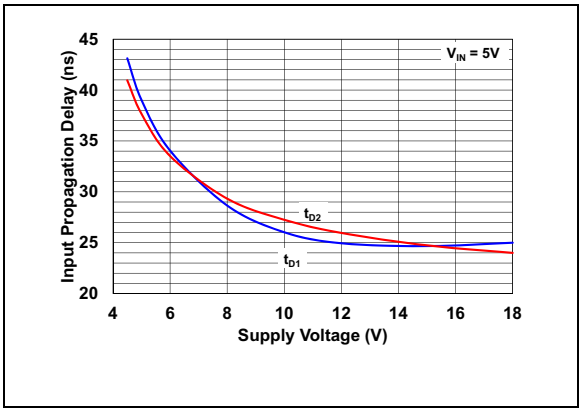


FIGURE 2-7: *Input Propagation Delay vs. Supply Voltage.*

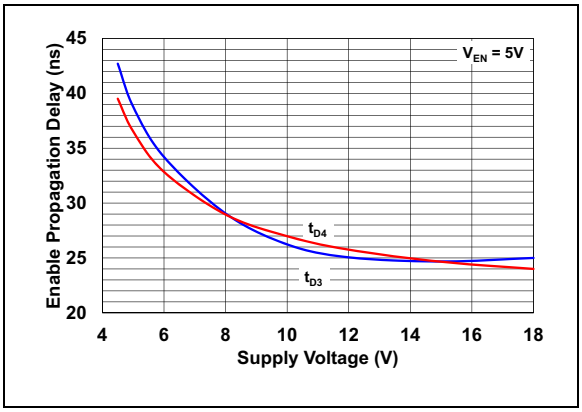


FIGURE 2-10: *Enable Propagation Delay vs. Supply Voltage.*

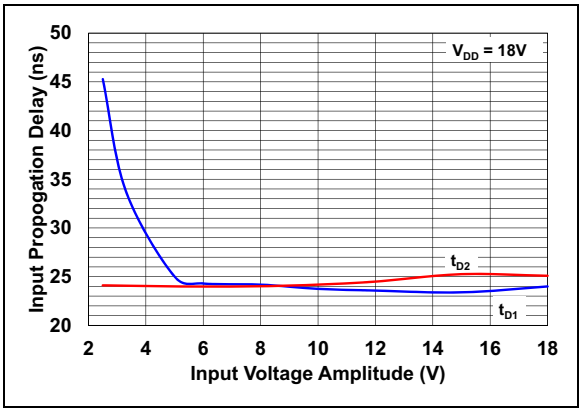


FIGURE 2-8: *Input Propagation Delay Time vs. Input Amplitude.*

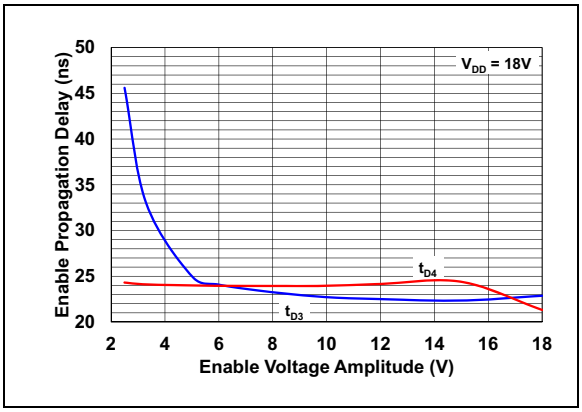


FIGURE 2-11: *Enable Propagation Delay Time vs. Enable Voltage Amplitude.*

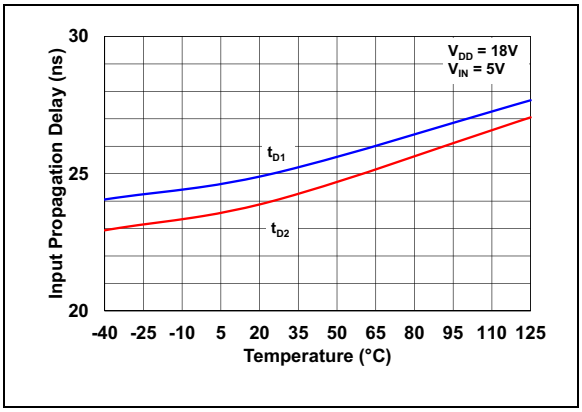


FIGURE 2-9: *Input Propagation Delay vs. Temperature.*

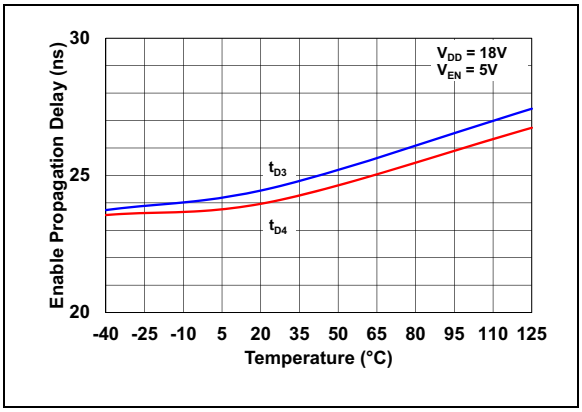


FIGURE 2-12: *Enable Propagation Delay vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

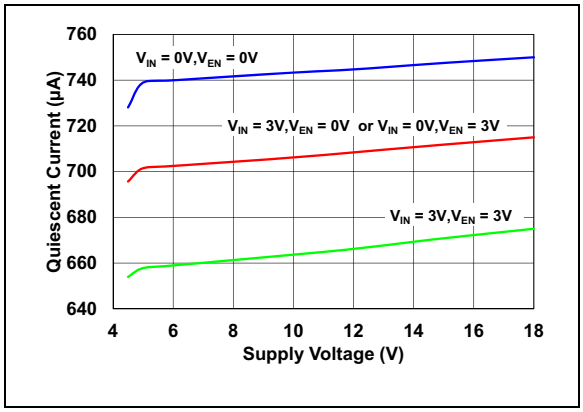


FIGURE 2-13: *Quiescent Supply Current vs. Supply Voltage.*

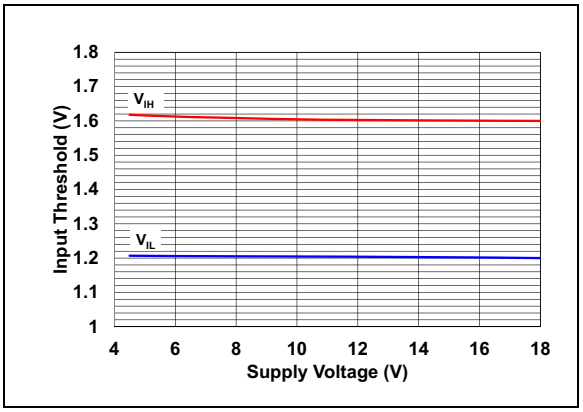


FIGURE 2-16: *Input Threshold vs. Supply Voltage.*

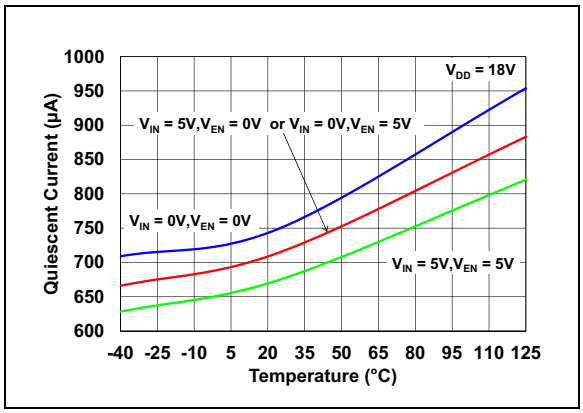


FIGURE 2-14: *Quiescent Supply Current vs. Temperature.*

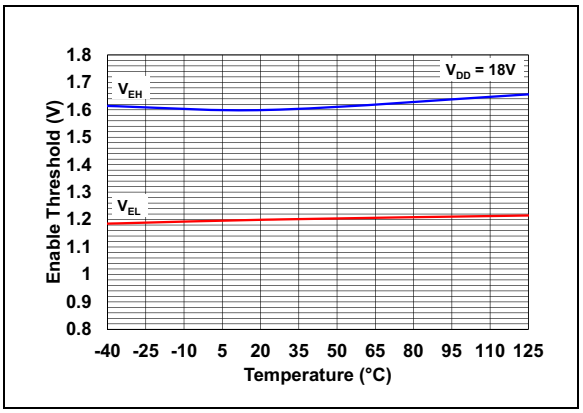


FIGURE 2-17: *Enable Threshold vs. Temperature.*

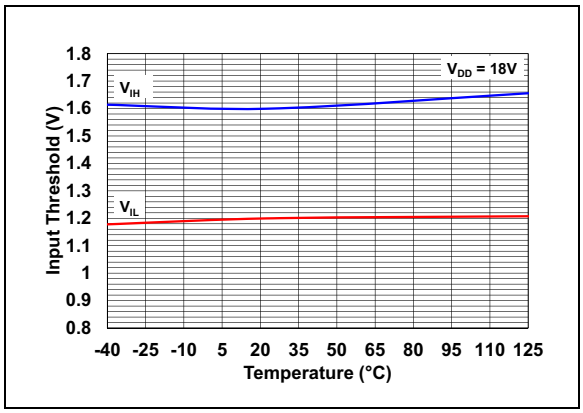


FIGURE 2-15: *Input Threshold vs. Temperature.*

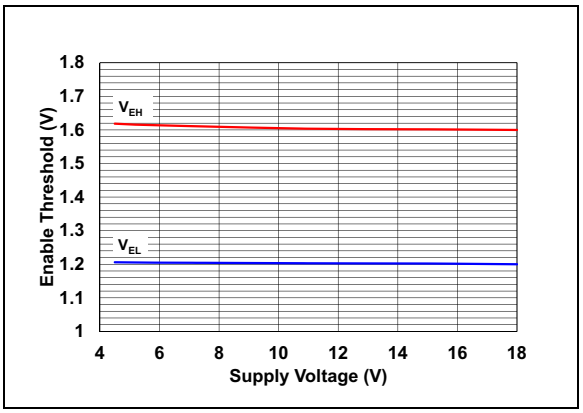


FIGURE 2-18: *Enable Threshold vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

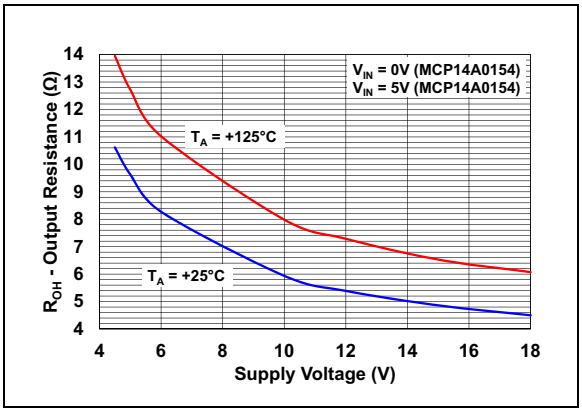


FIGURE 2-19: *Output Resistance (Output High) vs. Supply Voltage.*

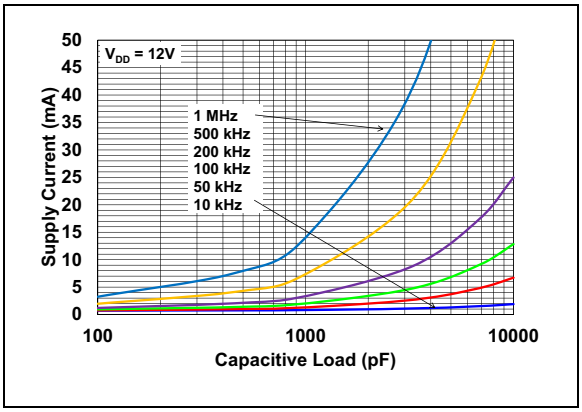


FIGURE 2-22: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

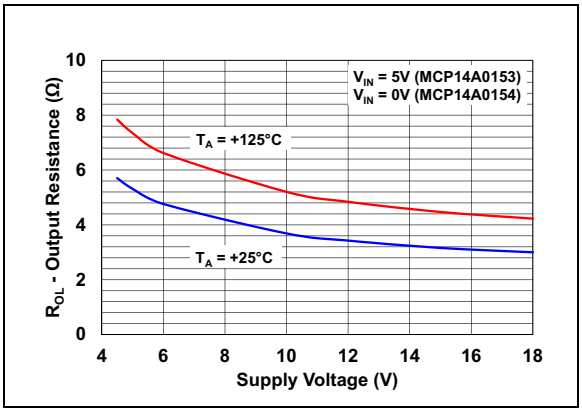


FIGURE 2-20: *Output Resistance (Output Low) vs. Supply Voltage.*

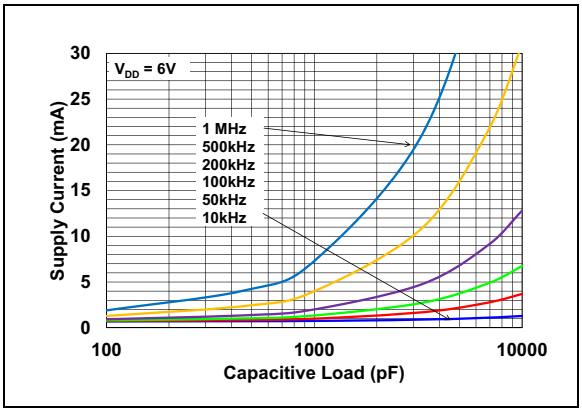


FIGURE 2-23: *Supply Current vs. Capacitive Load (V_{DD} = 6V).*

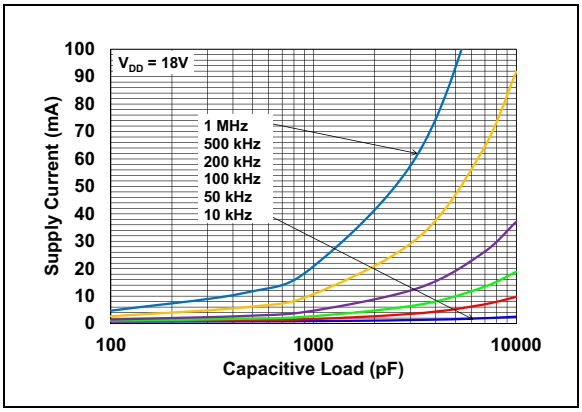


FIGURE 2-21: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

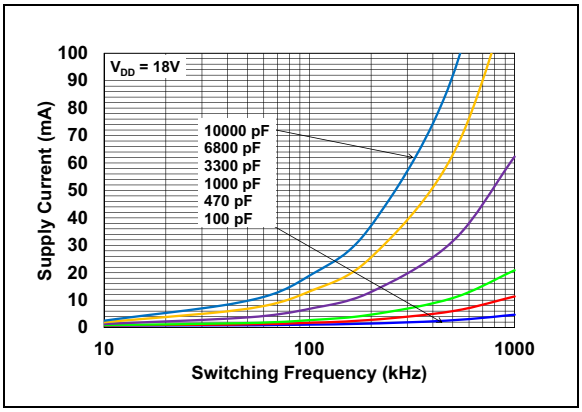


FIGURE 2-24: *Supply Current vs. Frequency (V_{DD} = 18V).*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

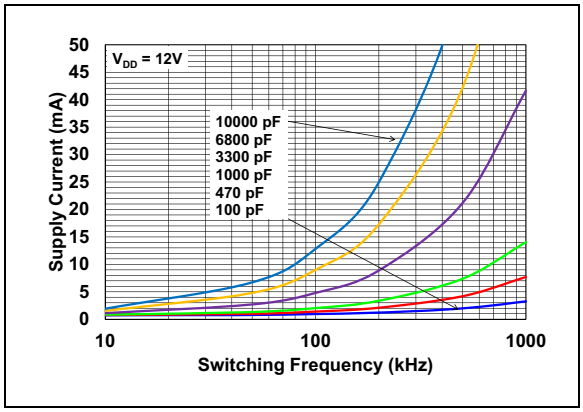


FIGURE 2-25: *Supply Current vs. Frequency (V_{DD} = 12V).*

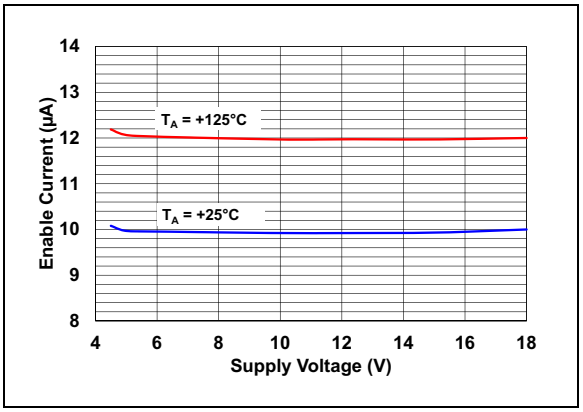


FIGURE 2-27: *Enable Current vs. Supply Voltage.*

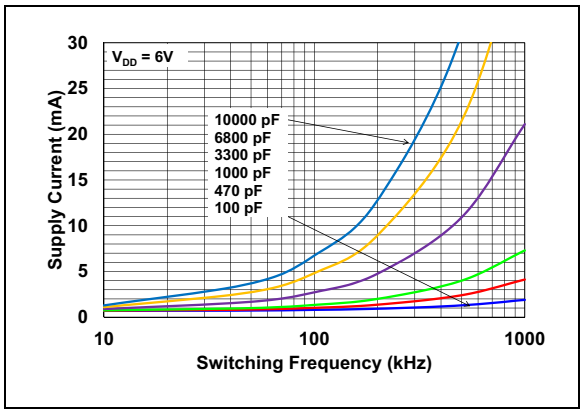


FIGURE 2-26: *Supply Current vs. Frequency (V_{DD} = 6V).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP14A0153, MCP14A0154, MCP14A0155		Symbol	Description
2x3 TDFN	MSOP/SOIC		
1	1	EN A	Enable – Channel A
2	2	IN A	Input – Channel A
3	3	GND	Device Ground
4	4	IN B	Input – Channel B
5	5	$\overline{\text{OUT B}}$/OUT B	Output – Channel B
6	6	V_{DD}	Supply Input
7	7	$\overline{\text{OUT A}}$/OUT A	Output – Channel A
8	8	EN B	Enable – Channel B
EP	—	EP	Exposed Thermal Pad (GND)

3.1 Output Pins ($\overline{\text{OUT A}}$/OUT A, $\overline{\text{OUT B}}$/OUT B)

The outputs are CMOS push-pull circuits that are capable of sourcing and sinking 1.5A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET stays in the intended state, even during large transients. This output also has a reverse current latch-up rating of 500 mA.

3.2 Device Ground Pin (GND)

GND is the device return pin for the input and output stages. The GND pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow through the ground pin.

3.3 Device Enable Pins (EN A,EN B)

The MOSFET driver device enable pins are high-impedance inputs featuring low threshold levels. The enable inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity. Driving the enable pins below the threshold will disable the corresponding output of the device, pulling $\overline{\text{OUT}}$/OUT low, regardless of the status of the input pin. Driving the enable pins above the threshold allows normal operation of the $\overline{\text{OUT}}$/OUT pin based on the status of the input pin. The enable pins utilize internal pull-up resistors, allowing the pins to be left floating for standard driver operation.

3.4 Control Input Pins (IN A,IN B)

The MOSFET driver control inputs are high-impedance inputs featuring low threshold levels. The inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

3.5 Supply Input Pin (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.6 Exposed Metal Pad Pin (EP)

The exposed metal pad of the TDFN package is internally connected to GND. Therefore, this pad should be connected to a Ground plane to aid in heat removal from the package.

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver, such as the MCP14A0153/4/5 family devices, can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully OFF state to a fully ON state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14A0153/4/5 timing.

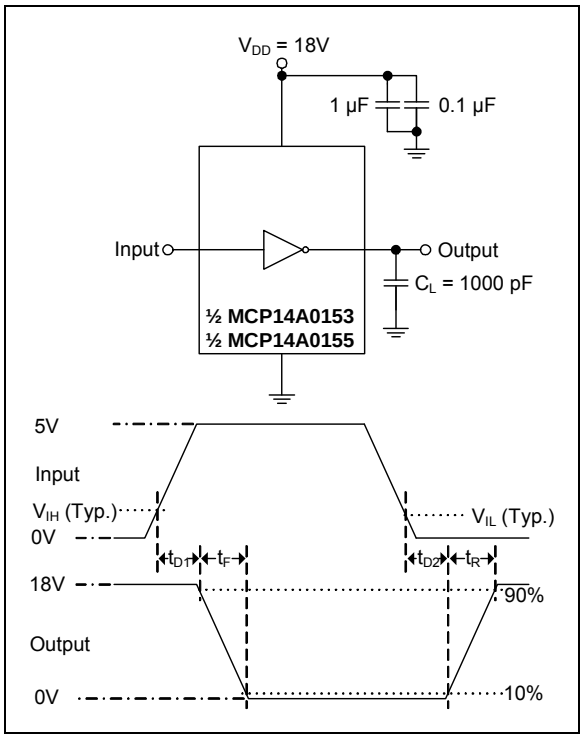


FIGURE 4-1: *Inverting Driver Timing Waveform.*

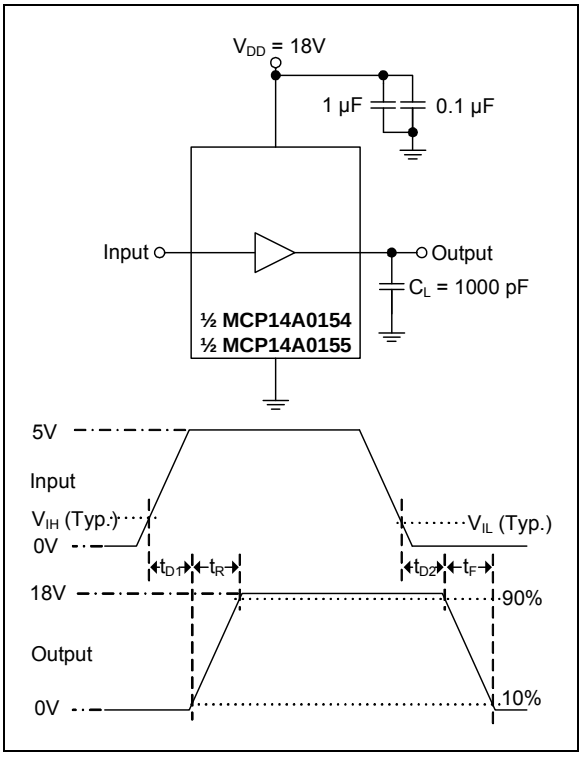


FIGURE 4-2: *Non-Inverting Driver Timing Waveform.*

4.3 Enable Function

The enable pins (EN A, EN B) provide additional control of the output pins (OUT). These pins are active-high and are internally pulled up to V_{DD} so that the pins can be left floating to provide standard MOSFET driver operation.

When the enable pin input voltages are above the enable pin high-voltage threshold (V_{EN_H}), the corresponding output is enabled and allowed to react to the status of the input pin. However, when the voltage applied to the enable pins falls below the low threshold voltage (V_{EN_L}), the driver's corresponding output is disabled and doesn't respond to changes in the status of the input pins. When the driver is disabled, the output is pulled down to a low state. Refer to Table 4-1 for the enable pin logic. The threshold voltage levels for the enable pin are similar to the threshold voltage levels of the input pin and are TTL compatible. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4}, are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

EN	IN	$\overline{OUT}$	OUT
H	H	L	H
H	L	H	L
L	X	L	L

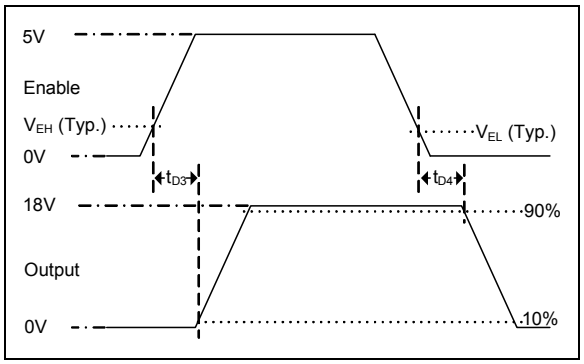


FIGURE 4-3: *Enable Timing Waveform.*

4.4 Decoupling Capacitors

Careful PCB layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place 1.0 µF and 0.1 µF low-ESR ceramic capacitors in parallel between the driver V_{DD} and GND. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper Printed Circuit Board (PCB) layout is important in high-current, fast switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. The PCB trace loop length and inductance should be minimized by the use of ground planes or traces under the MOSFET gate drive signal. Separate analog and power grounds, and local driver decoupling should also be used.

Placing a ground plane beneath the MCP14A0153/4/5 devices will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements, as shown in Equation 4-1.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

P_T = Total Power Dissipation
P_L = Load Power Dissipation
P_Q = Quiescent Power Dissipation
P_{CC} = Operating Power Dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

f = Switching Frequency
C_T = Total Load Capacitance
V_{DD} = MOSFET Driver Supply Voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the input and enable pins. See **Section 1.0 "Electrical Characteristics"** for typical quiescent current draw values in different operating states. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

I_{QH} = Quiescent Current in the High State
D = Duty Cycle
I_{QL} = Quiescent Current in the Low State
V_{DD} = MOSFET Driver Supply Voltage

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions, because for a very short period of time, both MOSFETs in the output stage are on simultaneously. This crossover current leads to a power dissipation described in Equation 4-4.

EQUATION 4-4:

$$P_{CC} = V_{DD} \times I_{CO}$$

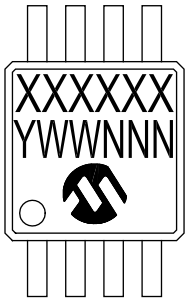
Where:

I_{CO} = Crossover Current
V_{DD} = MOSFET Driver Supply Voltage

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead MSOP (3x3 mm)

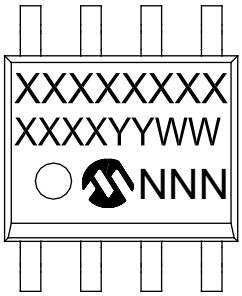


Device	Code
MCP14A0153T-E/MS	A0153
MCP14A0154T-E/MS	A0154
MCP14A0155T-E/MS	A0155

Note: Applies to 8-Lead MSOP.

Example

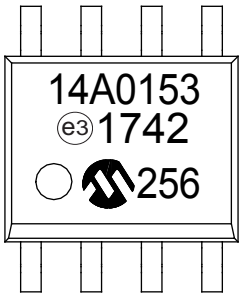
8-Lead SOIC (3.90 mm)



Device	Code
MCP14A0153T-E/SN	14A0153
MCP14A0154T-E/SN	14A0154
MCP14A0155T-E/SN	14A0155

Note: Applies to 8-Lead SOIC.

Example



8-Lead TDFN (2x3x0.75 mm)

Device	Code
MCP14A0153T-E/MNY	ACU
MCP14A0154T-E/MNY	ACM
MCP14A0155T-E/MNY	ACV

Note: Applies to 8-Lead TDFN.

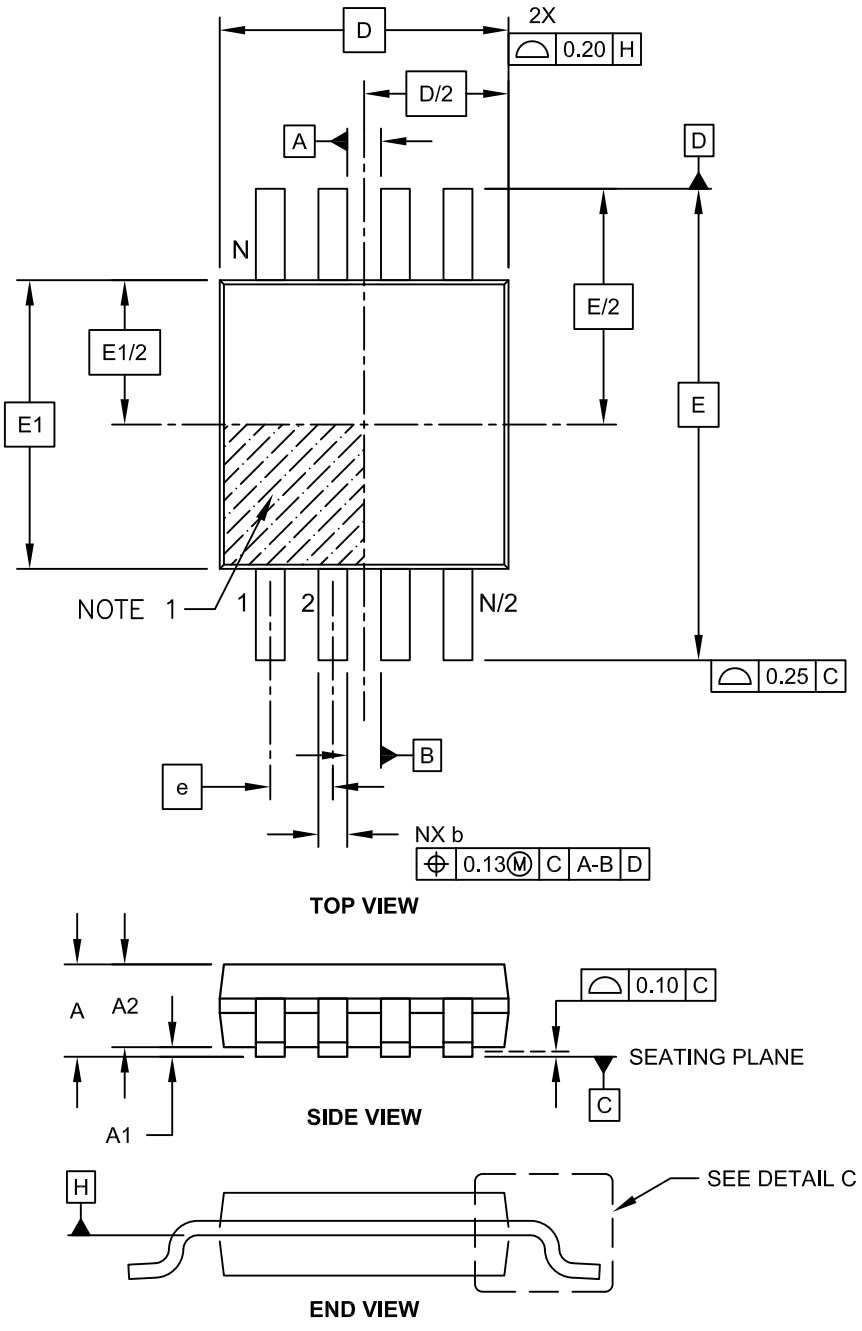
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

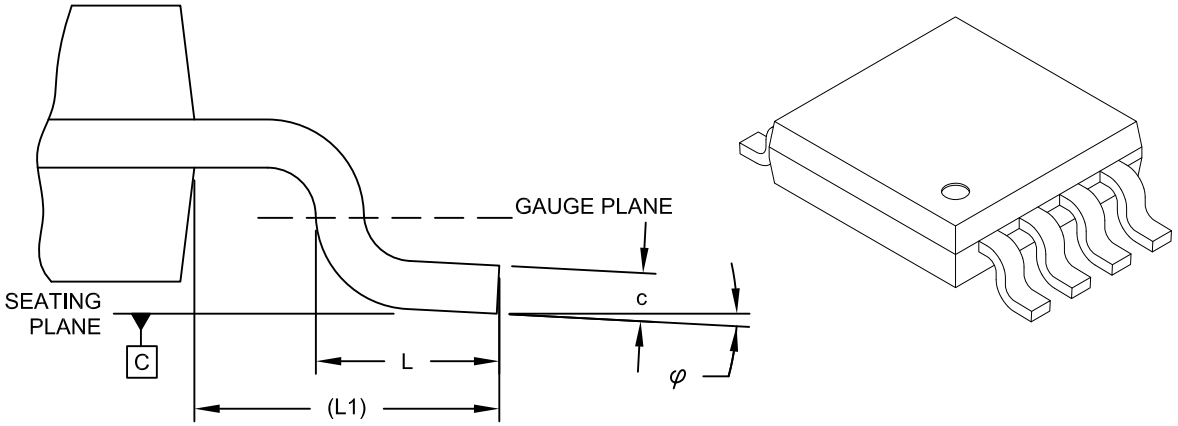
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

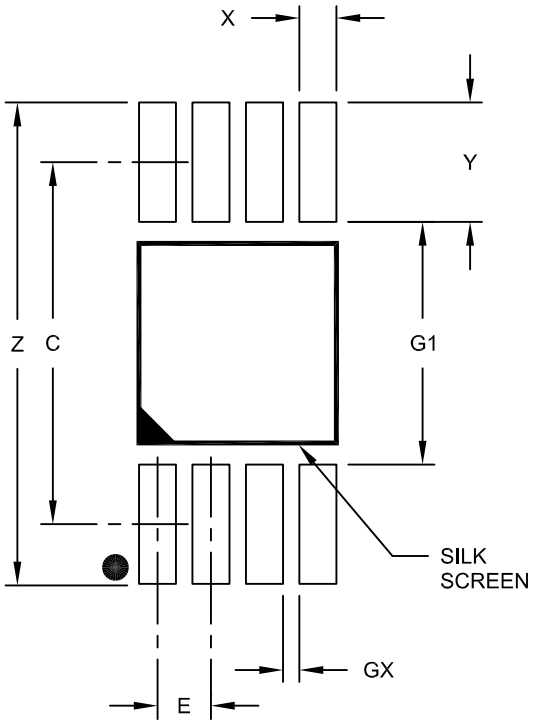
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

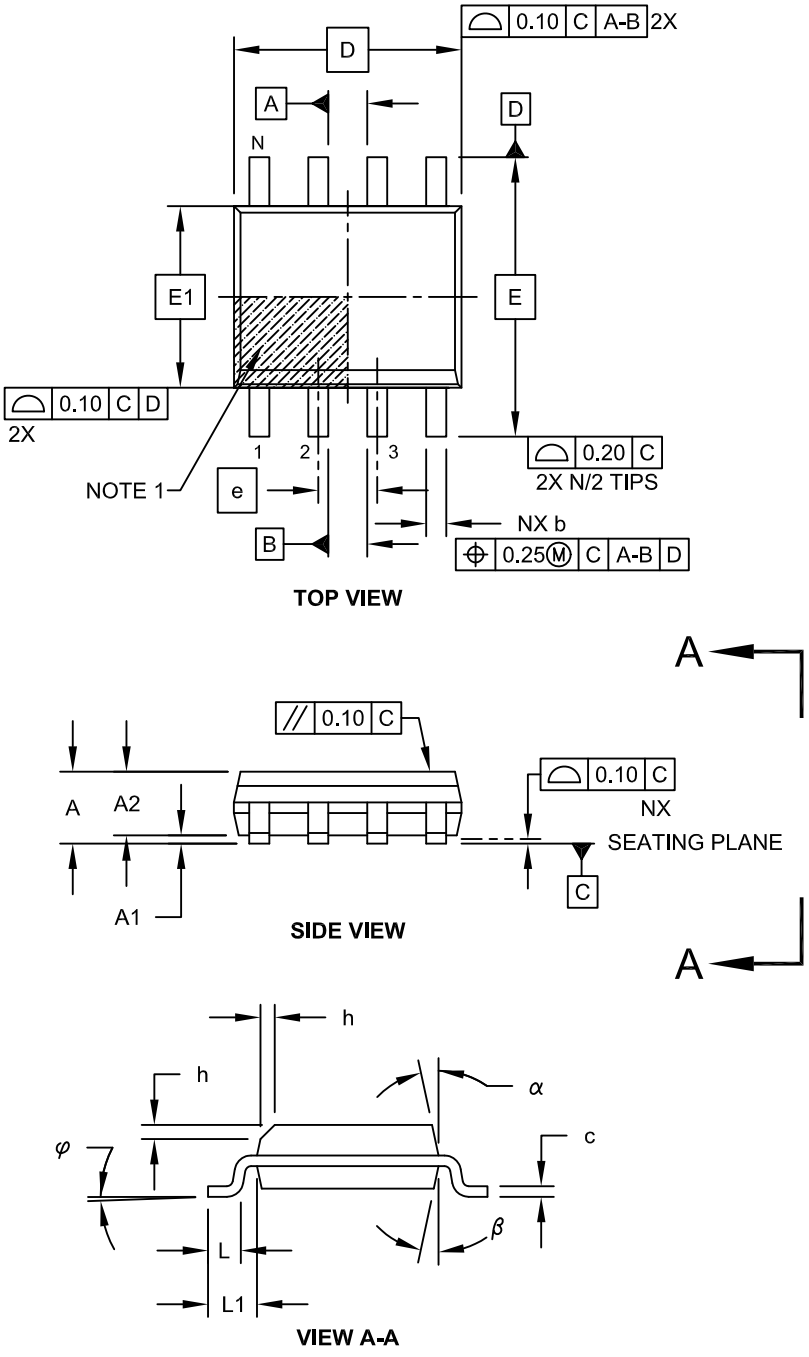
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

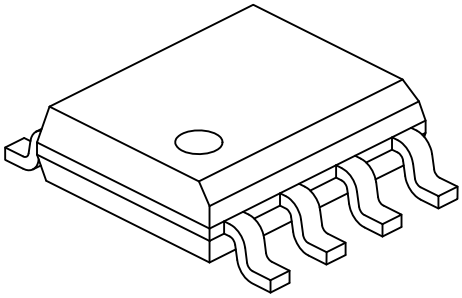
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

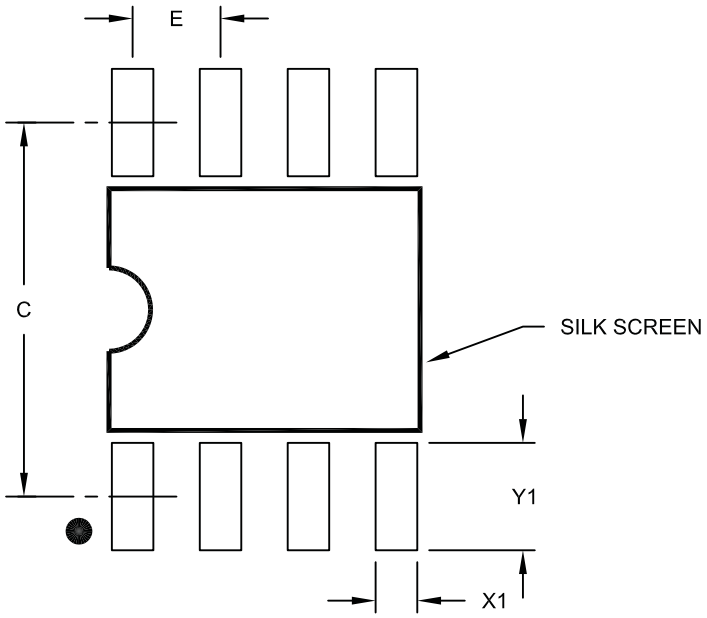
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

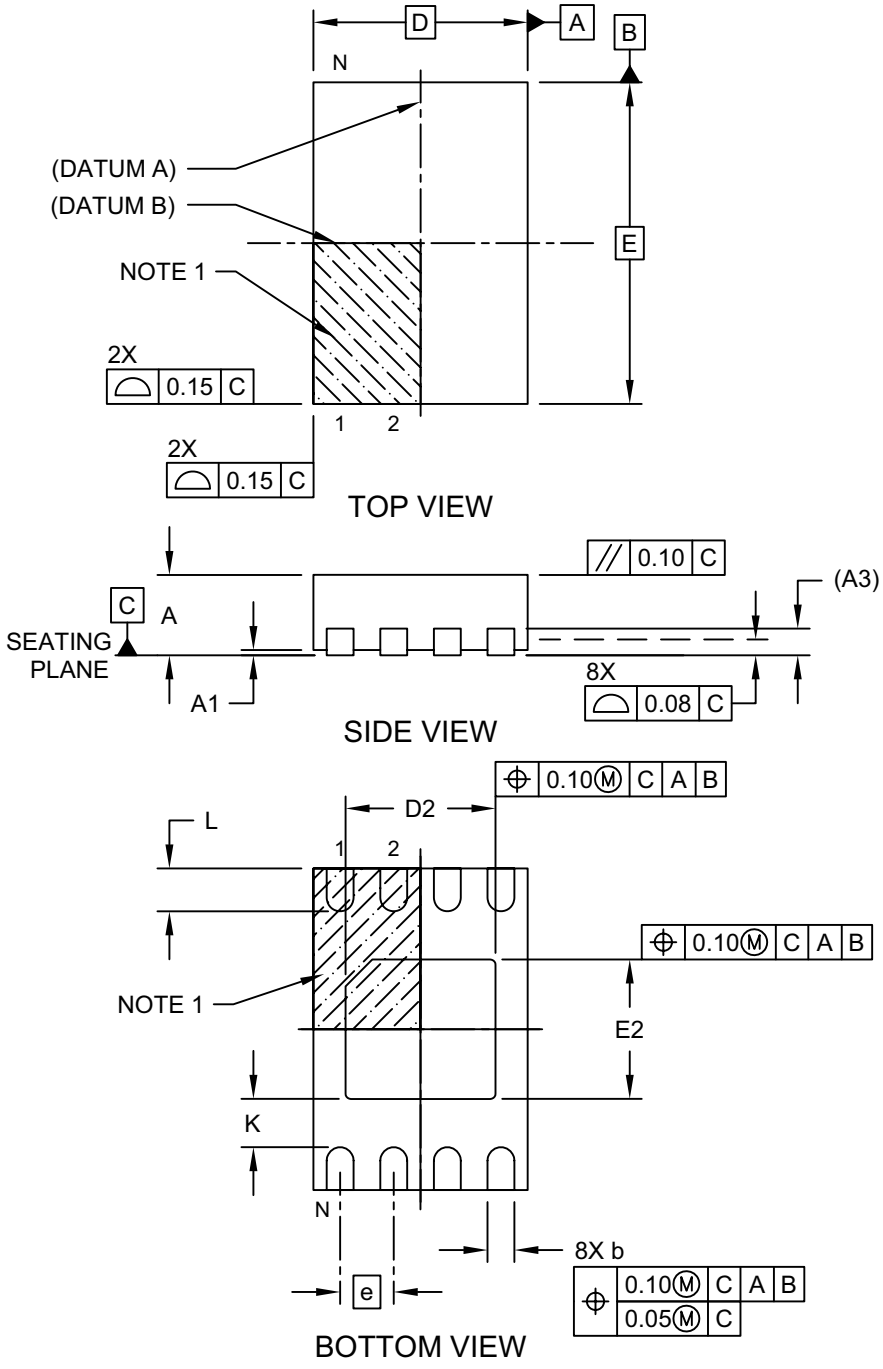
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

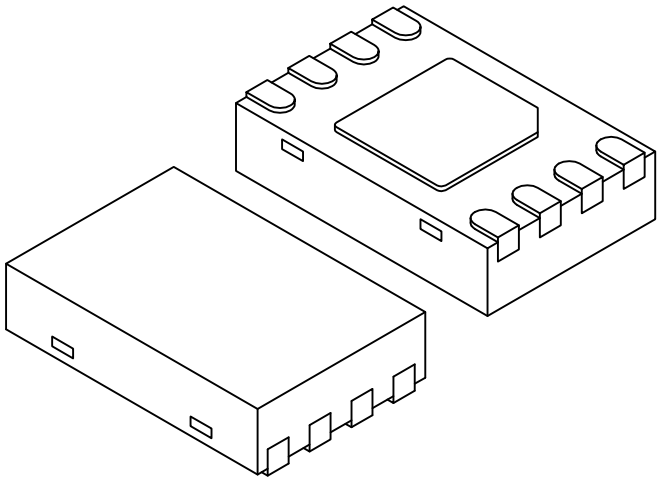
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

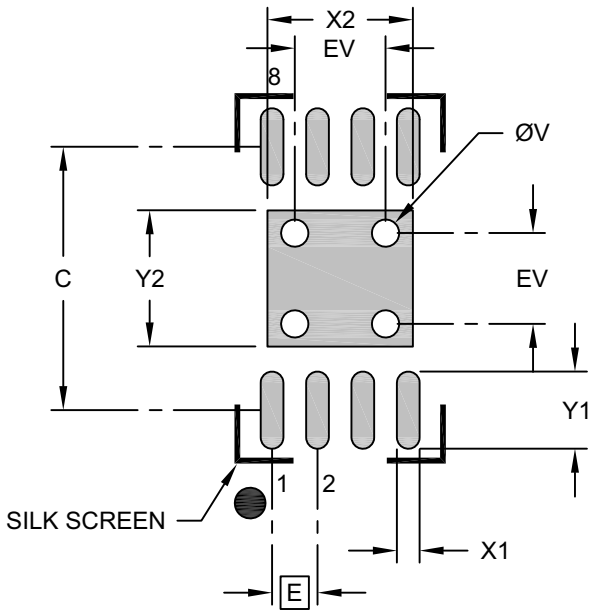
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

APPENDIX A: REVISION HISTORY

Revision B (July 2017)

The following is the list of modifications:

- Updated the Typical Performance Curves.
- Updated the Packaging Information.
- Various typographical edits.

Revision A (December 2015)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	–X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP14A0153:	High-Speed MOSFET Driver
	MCP14A0154:	High-Speed MOSFET Driver
	MCP14A0155:	High-Speed MOSFET Driver
	MCP14A0153T:	High-Speed MOSFET Driver (Tape and Reel)
	MCP14A0154T:	High-Speed MOSFET Driver (Tape and Reel)
	MCP14A0155T:	High-Speed MOSFET Driver (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MS =	8-Lead Plastic Micro Small Outline Package (MSOP)
	SN =	8-Lead Plastic Small Outline Package (SOIC)
	MNY* =	8-Lead Plastic Dual Flat, No Lead Package - 2x3x0.8 mm Body (TDFN)
	*Y =	Nickel Palladium Gold Manufacturing Designator. Only available on the TDFN package.

Examples:

a) MCP14A0153T-E/MS: Tape and Reel, Extended Temperature, 8-Lead MSOP Package

b) MCP14A0153-E/MS: Extended Temperature, 8-Lead MSOP Package

c) MCP14A0154T-E/SN: Tape and Reel, Extended Temperature, 8-Lead SOIC Package

d) MCP14A0154-E/SN: Extended Temperature, 8-Lead SOIC Package

e) MCP14A0155T-E/MNY: Tape and Reel, Extended Temperature, 8-Lead TDFN Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-1930-3

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820