

3.3V Differential LVPECL-to-LVTTL Translator

Features

- 3.3V Power Supply
- 2.0 ns Typical Propagation Delay
- Low Power
- Differential LVPECL Inputs
- 24 mA TTL Outputs
- Flow-Through Pinouts
- Available in 8-Lead SOIC Package

General Description

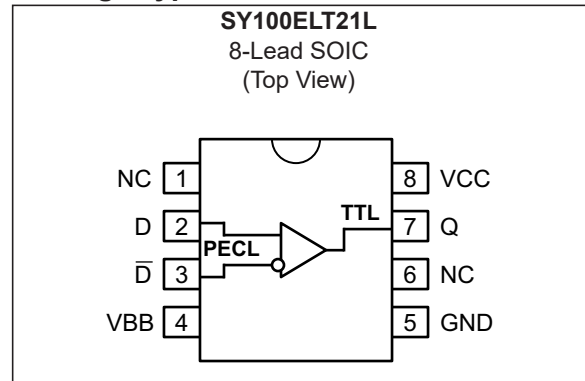
The SY100ELT21L is a single differential LVPECL-to-LVTTL translator that uses a single +3.3V power supply. Because LVPECL (low voltage positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the ELT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

VBB allows a differential, single-ended, or AC-coupled interface to the device. If used, the VBB output should be bypassed to VCC with a 0.01 μ F capacitor.

Under open input conditions, the \bar{D} will be biased at a $V_{CC}/2$ voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

The ELT21L is compatible with positive ECL 100K logic levels.

Package Type



SY100ELT21L

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC})	-0.5V to +3.8V
PECL Input Voltage (V_{IN})	0V to $V_{CC}+0.5V$
Voltage Applied to Output at High State (V_{OUT})	-0.5V to V_{CC}
Current Applied to Output at Low State (I_{OUT})	Twice the Rated I_{OL} in mA

† **Notice:** Permanent device damage can occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TTL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted.						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Short Circuit Current	I_{OS}	-275	—	-80	mA	$V_{OUT} = 0V$
Power Supply Current	I_{CC}	—	—	20	mA	Valid for $-40^{\circ}C$, $0^{\circ}C$, and $+85^{\circ}C$
		—	14	20		Valid for $+25^{\circ}C$
Output High Voltage	V_{OH}	2.0	—	—	V	$I_{OH} = -3.0$ mA
Output Low Voltage	V_{OL}	—	—	0.5	V	$I_{OL} = 24$ mA

PECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted.						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current	I_{IL}	0.5	—	—	μA	—
Input High Voltage	V_{IH}	2135	—	2420	mV	Note 1
Input Low Voltage	V_{IL}	1490	—	1825	mV	Note 1
Common Mode Range	V_{CMR}	1.2	—	V_{CC}	V	—
Reference Output	V_{BB}	1920	—	2040	mV	Note 1, Valid for $-40^{\circ}C$, $0^{\circ}C$, and $+85^{\circ}C$
		1920	1980	2040		Note 1, Valid for $+25^{\circ}C$

Note 1: These values are for $V_{CC} = 3.3V$. Level specifications will vary 1:1 V_{CC} .

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Propagation Delay	t_{PLH}	1.5	—	2.5	ns	$C_L = 20$ pF, Valid for $-40^{\circ}C$, $0^{\circ}C$, & $+85^{\circ}C$
	t_{PHL}	1.5	2.0	2.5		$C_L = 20$ pF, Valid for $+25^{\circ}C$
Part-to-Part Skew	t_{SKPP}	—	—	0.5	ns	$C_L = 20$ pF, Note 1 , Note 2
Maximum Input Frequency	f_{MAX}	275	—	—	MHz	$C_L = 20$ pF, Note 2 , Note 3 , Note 4
Input Swing	V_{PP}	200	—	1000	mV	Note 5
Output Rise/Fall Time (1.0V to 2.0V)	t_r/t_f	0.5	—	1.0	ns	$C_L = 20$ pF

- Note 1:** Part-to-part skew considering high-to-high transitions at common V_{CC} level.
- 2:** These parameters are guaranteed, but not tested.
- 3:** Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
- 4:** The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
- 5:** Input swing for which AC parameters are guaranteed. Minimum input swing guarantees full logic at output.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Lead Temperature	—	—	—	+260	$^{\circ}C$	Soldering, 20 sec.
Ambient Operating Temperature	T_A	-40	—	+85	$^{\circ}C$	—
Storage Temperature	T_S	-65	—	+150	$^{\circ}C$	—

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

SY100ELT21L

2.0 PIN DESCRIPTIONS

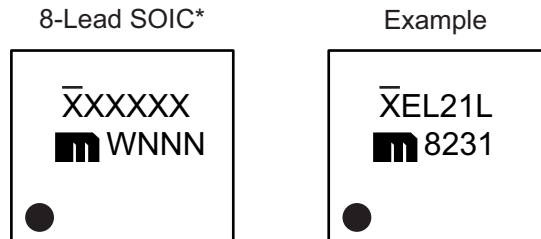
The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 6	NC	No connect.
2, 3	D, /D	Differential LVPECL inputs.
4	VBB	Reference output.
5	GND	Ground.
7	Q	TTL output.
8	VCC	+3.3V supply.

3.0 PACKAGING INFORMATION

3.1 Package Marking Information



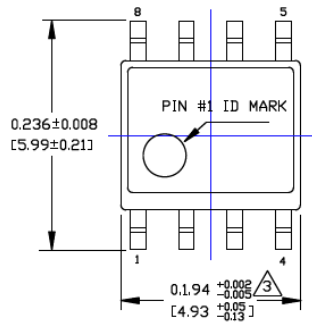
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

SY100ELT21L

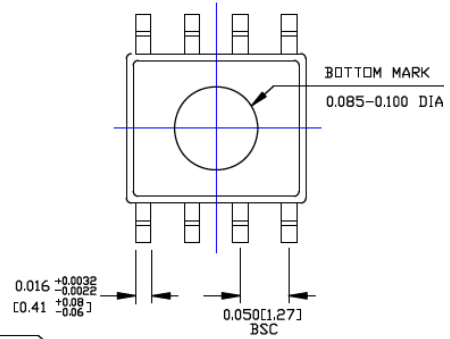
TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

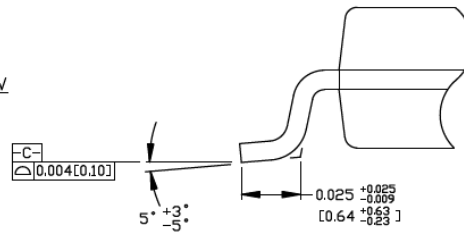
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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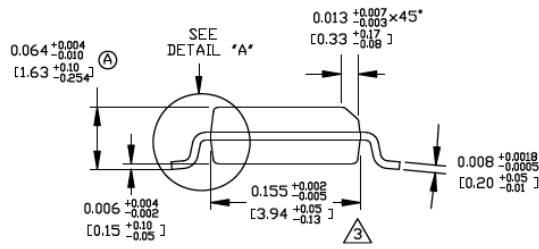
TOP VIEW



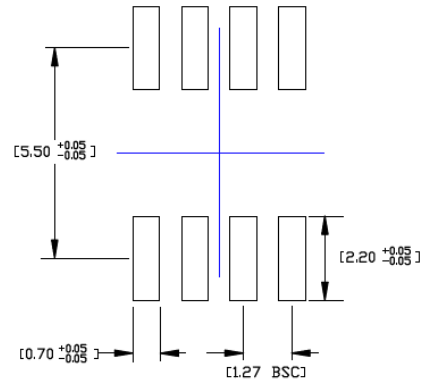
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Converted Micrel document SY100ELT21L to Microchip data sheet DS20006213A.
- Minor text changes throughout.
- Removal of all reference to the discontinued SY100ELT21L.
- Updated V_{PP} values and associated note in [AC Electrical Characteristics](#).

SY100ELT21L

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part No.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Device	Supply Voltage	Package	Temp. Range	Packing
Device:	SY100ELT21: Differential LVPECL-to-LVTTL Translator			
Supply Voltage:	L	=	3.3V	
Package:	Z	=	8-Lead SOIC	
Temperature Range:	G	=	-40°C to +85°C (NiPdAu Lead-Free)	
Tape and Reel:	<blank>	=	95/Tube	
	TR	=	1,000/Reel	

Examples:

a) SY100ELT21LZG:
SY100ELT21, 3.3V Supply Voltage,
8-Lead SOIC, -40°C to +85°C Temperature Range,
95/Tube

b) SY100ELT21LZG-TR:
SY100ELT21, 3.3V Supply Voltage,
8-Lead SOIC, -40°C to +85°C Temperature Range,
1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

SY100ELT21L

NOTES:

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