REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38	39	40														
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

Phu H. Nguyen

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Phu H. Nguyen

APPROVED BY

Thomas M. Hess

DRAWING APPROVAL DATE

15-02-09

REVISION LEVEL

MICROCIRCUIT, DIGITAL, 32-BIT SPARC V8 RECONFIGURABLE PROCESSOR, MULTIPLE CHIP MODULE

SIZE	CAGE CODE	
A	**67268**	**5962-14229**

SHEET 1 OF 40

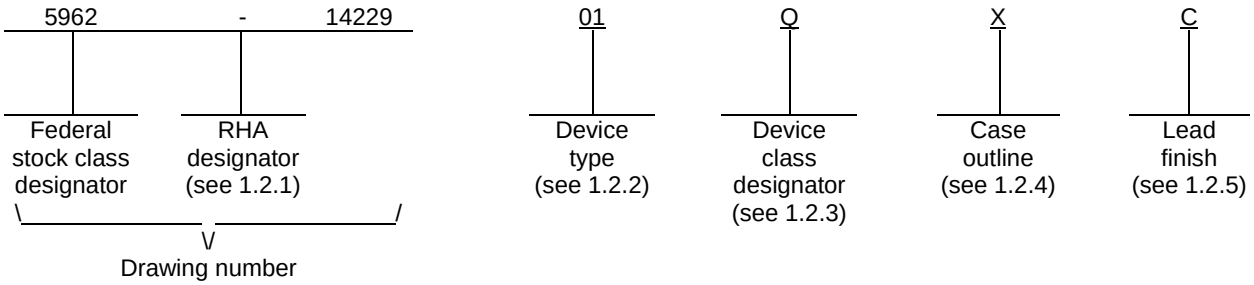
DSCC FORM 2233
APR 97

5962-E362-14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ATF697FF	32-bit SPARC V8 reconfigurable processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	352	Quad Flatpack unformed Leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (PROC_V_{DD18}, FPGA_V_{DD18}, PROG_V_{DDPLL}) ..... -0.3 V to 2.0 V 3/
Supply voltage range (PROC_V_{CC33}, FPGA_V_{CC33}) ..... -0.3 V to 4.0 V 4/
All output voltages with respect to ground ..... -0.3 V to 4.0 V
Maximum power dissipation (P_D) ..... 4.5 W
Processor power dissipation ..... 1.2 W
Reconfigurable unit power dissipation ..... 3.3 W
Case temperature range, (T_C) ..... -55ºC to +125ºC
Thermal resistance, junction to case X. 4ºC/W 5/
Storage temperature range (T_S) ..... -65°C to + 150°C
Maximum junction temperature (T_J)..... +175°C
Lead temperature (soldering 10sec) Case outline X ..... +300°C 6/

1.4 Recommended operating conditions. 2/ 7/ 8/:

Supply voltage range (PROC_V_{DD18}, FPGA_V_{DD18}, PROG_V_{DDPLL}) ..... 1.65 V to 1.95 V 3/
Supply voltage range (PROC_V_{CC33}, FPGA_V_{CC33}) ..... 3.0 V to 3.6 V 4/
Ambient temperature (T_A) ..... -55°C to 125°C
IO Power Supply (PROC_V_{CC33}, FPGA_V_{CC33}) ..... 3.3 V ± 0.3 V
LVDS Reference Voltage (LVDS_REF_A, LVDS_REF_B) ..... 1.25 V± 0.1 V
IO Power Supply (PROC_V_{DD18}, FPGA_V_{DD18}, PROG_V_{DDPLL}) ..... 1.8 V ± 0.15 V

1.5 Digital logic testing for device classes Q and V.

Lead temperature (soldering 10sec) Case outline X ..... +300°C 6/
Fault coverage measurement (MIL-STD-883, method 5012) :
Processor. ..... 92 percent
Reconfigurable unit ..... 95 percent 9/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to ground unless otherwise specified.
3/ For core.
4/ For interface I/O's.
5/ Based on thermal simulation
6/ For Multilayer Quad Flat Package case, duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed; else, during reflow.
7/ When the device needs to be powered "on/off" while other circuits in the application are still powered, the recommended "power on/off" sequences are:
Power-up:
First power PROC_VCC33 (I/O) & FPGA_VCC33 (I/O)
Then power PROC_VDD18 (Core) & FPGA_VDD18 (Core).
Power-down:
First power PROC_VDD18 (Core) & FPGA_VDD18 (Core).
Then power PROC_VCC33 (I/O) & FPGA_VCC33 (I/O)
is also recommended to stop all activity during these phases as a bi-directional could be in an undetermined state (input or output mode) and create bus contention
8/ Cold sparing capability of the IOs allows to be electrically connected to a bus while its power supply remains in the range [VSS-300mV/VSS+300mV], this without any risk of damage for the device. Cold-sparing allows a redundant spare to be electrically connected but unpowered until needed.
For applications requiring high reliability, the capability to use of a redundant device is a key feature. Cold sparing availability on the ATF697FF makes the reconfigurable processor especially suitable for high reliability systems. The cold sparing feature is available for all the IOs:
All the General Purpose IOs
All the LVDS IOs
They present a high input impedance when unpowered [VSS-300mV / VSS+300mV] and exhibit a negligible leakage current if exposed to a non-null input voltage at that time.
9/ 95 percent test coverage of blank programmable logic devices.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://www.quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD78 – Standardized Test Procedure for Characterization of Latch-up in CMOS Integrated Circuits.

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

TELECOMMUNICATIONS INDUSTRY ASSOCIATION 2001

TIA/EIA-644 - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.

(Copies of this document are from TELECOMMUNICATIONS INDUSTRY ASSOCIATION 2001, Standards and Technology Department, 2500 Wilson Boulevard, Arlington, VA 22201).

IEEE - THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at http://www.ieee.org or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331).

(Non-Government standards and other publications are normally available from the organizations that prepare of distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block or logic diagram(s) shall be as specified on figure 3.

3.2.3.1 LVDS Interface. The LVDS basic interface and bidirectional communication shall be as specified on figure 4.

3.2.3.2 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.4 Truth table(s).

3.2.4.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 90 percent of the total number of logic modules shall be utilized.

3.2.4.2 Programmed devices. Prior to submitting altered item drawing the truth table or test vectors for programmed devices should be agreed upon by acquiring activity and the manufacturer.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.8.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA.

3.8.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery. Manufacturer shall verify design checksum after programming

TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}	V_{CC} = PROC_V_{CC33} = FPGA_V_{CC33}	1, 2, 3	All	$0.7V_{CC}$	4	V
Low Level Input Voltage	V_{IL}	V_{CC} = PROC_V_{CC33} = FPGA_V_{CC33}	1, 2, 3	All	-0.3	$0.3V_{CC}$	V
Low level input current 4/	I_{IL}	V_{IN} = PROC_V_{SS33} = FPGA_V_{SS33}	1,2,3	All	-1	1	µA
Low level input current with Pull up 5/ 6/	I_{ILPU}	V_{IN} = PROC_V_{SS33} = FPGA_V_{SS33}	1,2,3	All	-600	-20	µA
High level input current 4/	I_{IH}	V_{IN} = PROC_V_{CC33} (max) = FPGA_V_{CC33} (max)	1,2,3	All	-1	1	µA
High level input current With Pull-down 5/ 7/	I_{IHPD}	V_{IN} = PROC_V_{CC33} (max) = FPGA_V_{CC33} (max)	1,2,3	All	20	600	µA
High impedance state low level output current 8/	I_{OZL}	V_{IN} = PROC_V_{SS33} = FPGA_V_{SS33}	1,2,3	All	-1	1	µA
High impedance state low level output current With Pull up 5/ 9/	I_{OZLPU}	V_{IN} = PROC_V_{SS33} = FPGA_V_{SS33}	1,2,3	All	-600	-20	µA
High impedance state high level output current 8/	I_{OZH}	V_{IN} = PROC_V_{CC33} (max) = FPGA_V_{CC33} (max)	1,2,3	All	-1	1	µA
High impedance state high level output current With Pull down 5/	I_{OZHPD}	V_{IN} = PROC_V_{CC33} (max) = FPGA_V_{CC33} (max)	1,2,3	All	20	600	µA
Cold Sparing input leakage current	I_{ICS}	$PROC\_V_{DD18}$ = $FPGA\_V_{DD18}$ = 0V $PROC\_V_{CC33}$= $FPGA\_V_{CC33}$ = 0V V_{IN} = PROC_V_{SS33} to PROC_V_{CC33} (max) = FPGA_V_{SS33} to FPGA_V_{CC33} (max)	1,2,3	All	-1	1	µA
Cold Sparing output leakage current	I_{OCS}	$PROC\_V_{DD18}$ = $FPGA\_V_{DD18}$ = 0V $PROC\_V_{CC33}$= $FPGA\_V_{CC33}$ = 0V V_{IN} = PROC_V_{SS33} to PROC_V_{CC33} (max) = FPGA_V_{SS33} to FPGA_V_{CC33} (max	1,2,3	All	-1	1	µA
Supply threshold of cold sparing Buffers 10/	V_{CSTH}	$I_{ICS} < 4$ µA		All	0.5 Typ		V

See notes at the end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level output voltage 11/	V_{OL}	V_{CC} = PROC_V_{CC33} (min) = FPGA_V_{CC33} (min) IOL = 2, 4, 8, 10 & 14 mA	1, 2, 3	All		0.4	V
High level output voltage12/	V_{OH}	V_{CC} = PROC_V_{CC33} (min) = FPGA_V_{CC33} (min) IOH = -2, -4, -8, -10 & -14 mA	1, 2, 3	All	V_{CC} -0.4		V
Processor Stand by current	I_{CCSB}	Reconfigurable unit not powered FPGA_V_{DD18} = FPGA_V_{CC33} =0V V_{cc} = PROC_V_{CC33} (max) V_{DD} = PROC_V_{DD18} (max) No clock active	1, 2, 3	All		5	mA
Reconfigurable Unit Array Standby current	I_{CCSB1}	V_{CC} = FPGA_V_{CC33} max After reset, cells not configured	1, 2, 3	All		50	mA
	I_{CCSB2}	V_{CC} = FPGA_V_{CC33} max All cells configured, no floating nodes	1, 2, 3	All		200	mA
Input capacitance 13/ 14/	C_{IN}	See 4.4.1c	4	All		10	pF
Functional test		See 4.4.1b	7, 8	All			
LVDS Drivers DC characteristics							
Differential output voltage	$\|V_{OD}\|$	Rload = 100 Ω See figure 4	1, 2, 3	All	247	454	mV
Output offset voltage	V_{OS}		1, 2, 3	All	1125	1375	mV
Change in VOD between "0" and "1"	$\|\Delta V_{OD}\|$	Rload = 100 Ω	1, 2, 3	All	0	50	mV
Change in VOS between "0" and "1"	$\|\Delta V_{OS}\|$		1, 2, 3	All	0	50	mV
Output current 14/	ISA, ISB	Drivers shorted to FPGA_V_{SS33} or FPGA_V_{CC33}	9, 10, 11	All	1	6.2	mA
Output current 14/	ISAB	Drivers shorted together	9, 10, 11	All	2.6	4.8	mA
LVDS Receiver DC characteristics							
Input differential Voltage 14/	V_{ID}		9, 10, 11	All	200	600	mV
Input offset range 14/	V_{CM}		9, 10, 11	All	400	2000	mV

See notes at the end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reconfigurable Unit AC parameters		**14/**					
IO Propagation Delay pad → q 14/	t_{PD}	Input I/O= 3.3V, propagation delay from **pad** to **q**, no extra delay	9, 10, 11	All		3.6	ns
		Input I/O = 3.3V, propagation delay from **pad** to **q**, extra delay 1	9, 10, 11	All		3.7	ns
		Input I/O = 3.3V, propagation delay from **pad** to **q**, extra delay 3	9, 10, 11	All		4.1	ns
		Input I/O = 3.3V, propagation delay from **pad** to **q**, extra delay 5	9, 10, 11	All		4.6	ns
IO Propagation Delay a → pad 14/		Output , 3.3V, slow, propagation delay from **a** to **pad**, 40 pF load	9, 10, 11	All		7.1	ns
		Output , 3.3V, medium, propagation delay from **a** to **pad**, 40 pF load	9, 10, 11	All		6.2	ns
		Output , 3.3V, fast , propagation delay from **a** to **pad**, 40 pF load	9, 10, 11	All		6.0	ns
IO Propagation Delay oe → pad 14/		Output , 3.3V, slow, propagation delay from **oe** to **pad**, 40 pF load	9, 10, 11	All		8.2	ns
		Output , 3.3V, medium, propagation delay from **oe** to **pad**, 40 pF load	9, 10, 11	All		7.4	ns
		Output , 3.3V, fast , propagation delay from **oe** to **pad**, 40 pF load	9, 10, 11	All		7.1	ns
Clocks Pad → clk 14/		GCK Input pad at 3.3V delay from GCKx global clock pad to flop onthe rising edge clock	9, 10, 11	All		9.5	ns
		FCK Input pad at 3.3V delay from FCKx fast clock pad to flop on the rising edge clock. **Warning:** Flops must be placed on first or last column of the matrix	9, 10, 11	All		8	ns
Set/Reset pad → sn | rn 14/		Reset Input pad at 3.3V delay from any pad to the set/reset flop pin	9, 10, 11	All		10	ns

See notes at the end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clocks 14/ pad → pad	t_{PD}	GCK input pad to output pad (3.3V, fast), delay from GCKx global clock pad to an output pad loaded at 40pF **Warning:** flop is placed close to the output pad	9, 10, 11	All		22	ns
		FCK input pad to output pad (3.3V,fast), delay from FCKx fast clock pad to an output pad loaded at 40pF **Warning:** Flops must be placed on first or last column of the matrix	9, 10, 11	All		20	ns
Reconfigurable Unit Freeram Timing – Asynchronous mode 14/							
Write : **we** min pulse width high or low 14/	TWEL, TWEH	See Figure 5.	9, 10, 11	All		1.7	ns
Write, we → ain | a, setup time of address input before **low** transition at the **we i**nput 14/	t_{AWS}		9, 10, 11	All		4.2	ns
Write, we → ain | a, hold time of address input before **high** transition at the **we** input 14/	t_{AWH}		9, 10, 11	All		1.7	ns
Write, we → din | d, setup time of data input before **rising** transition at the **we** input 14/	t_{DS}		9, 10, 11	All		0	ns
Write, we → din | d, hold time of data input before rising transition at the we input 14/	t_{DH}		9, 10, 11	All		0	ns
Write /Read, din → dout, propagation delay between **din** and **dout** on double port ram when **ain** = **aout** 14/	t_{DD}		9, 10, 11	All		6.4	ns
Read, ain → dout,propagation delay from **ain** to **dout** 14/	t_{AD}		9, 10, 11	All		4.9	ns
Read, oe → dout, propagation delay from **oe** to **dout** for a transition from z to 0|1 14/	t_{OZX}		9, 10, 11	All		2.9	ns
Read, oe → dout, propagation delay from **oe** to **dout** for a transition from 0|1 to z 14/	t_{OXZ}		9, 10, 11	All		2.9	ns

See notes at the end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reconfigurable Unit Freeram Timing – Synchronous mode 14/							
Write - **clk** min pulse width high or low 14/	t_{CLKL}, t_{CLKH}	See Figure 5.	9, 10, 11	All		1.2	ns
Write - setup time of **we** input before active transition at the clk input 14/	t_{WCS}		9, 10, 11	All		2.7	ns
Write- hold time of **we** input before active transition at the clk input 14/	t_{WCH}		9, 10, 11	All	0		ns
Write - setup time of adress input before active transition at the **clk** input 14/	t_{ACS}		9, 10, 11	All		3.2	ns
Write - hold time of adress input before active transition at the **clk** input 14/	t_{ACH}		9, 10, 11	All	3.3		ns
Write - setup time of data input before active transition at the **clk** input 14/	t_{DCS}		9, 10, 11	All		1.5	ns
Write - hold time of data input before active transition at the **clk** input 14/	t_{DCH}		9, 10, 11	All	0		ns
Write/ Read - propagation delay from **clk** to **dout** 14/	t_{CD}		9, 10, 11	All		5.8	ns
Read - propagation delay from **aout** to **dout** 14/	t_{AD}		9, 10, 11	All		4.9	ns
Read - propagation delay from **oe** to **dout** for a transition from z to 0|1 14/	t_{OZX}		9, 10, 11	All		2.9	ns
Read - propagation delay from **oe** to **dout** for a transition from 0|1 to z or z to 0|1 14/	t_{OXZ}		9, 10, 11	All		2.9	ns

See notes at the end of Table IA.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ -55°C ≤ T_A ≤ +125°C 1.65V <PROC_V_{DD18} < 1.95V 1.65V <FPGA_V_{DD18} < 1.95V 3.0V <PROC_V_{CC33} < 3.6V 3.0V <FPGA_V_{CC33} < 3.6V Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVDS Drivers AC characteristics 14/							
Maximum operating frequency	F_{MAX}	FPGA_V_{CC33} = 3.3V ± 0.3V	9, 10, 11	All	-	200	MHz
Clock signal duty cycle	Clock	Max. frequency	9, 10, 11	All	45	55	%
Fall time 80-20%	t_{fall}	Rload = 100 Ω	9, 10, 11	All	445	838	ps
Rise time 20-80%	t_{rise}		9, 10, 11	All	445	841	ps
Propagation delay	Tp		9, 10, 11	All	1120	2120	ps
Duty cycle skew	t_{sk1}		9, 10, 11	All	0	80	ps
Channel to channel skew (same edge)	t_{sk2}		9, 10, 11	All	0	50	ps
LVDS Receiver AC characteristics with Cout = 50 pF 14/							
Propagation delay	t_p	FPGA_V_{CC33} = 3.3V ± 0.3V	9, 10, 11	All	0.7	2.4	ns
Duty cycle distortion	t_{skew}		9, 10, 11	All	-	500	ps

See notes at the end of Table .

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Processor AC Timing - Natural skew SKEW[1:0]='00'							
CLK period with PLL disabled 15/	t1	See Figure 5.	9, 10, 11	All	10		ns
CLK period with PLL enable 14/	t1_p		9, 10, 11	All	40	50	ns
CLK low or high pulse width PLL disabled	t2		9, 10, 11	All	4.5		ns
CLK low or high pulse width PLL enable 14/	t2_p		9, 10, 11	All	18		ns
SDCLK period 15/	t3		9, 10, 11	All	10		ns
SDCLK output delay - PLL disabled 16/	t4		9, 10, 11	All	3	8	ns
PLL setup time 15/ 20/	t5		9, 10, 11	All		10^7	ns
Reset pulse width 15/	t6		9, 10, 11	All	1*t3		ns
A[27:0] output delay 17/	t10		9, 10, 11	All	1.5	8	ns
D[31:0] and CB[7:0] Output delay 17/	t11		9, 10, 11	All	2	8.5	ns
D[31:0] and CB[7:0] Setup time 17/	t12		9, 10, 11	All	4		ns
D[31:0] and CB[7:0] hold time during load/fetch 17/ 18/	t13		9, 10, 11	All	0		ns
D[31:0] and CB[7:0] hold time during write 14/ 17/ 19/	t14		9, 10, 11	All	0	9	ns
OE*, READ and WRITE* output delay 17/	t15		9, 10, 11	All	1	7	ns
ROMS*[1:0] output delay 17/	t16		9, 10, 11	All	2	5.5	ns
RAMS*[4:0], RAMOE*[4:0] and RWE*[3:0] output delay 17/	t17		9, 10, 11	All	1.5	6	ns
IOS* output delay 17/ 18/	t18		9, 10, 11	All	2	5.5	ns
BRDY* setup time 14/ 17/	t19		9, 10, 11	All	5		ns
BRDY* hold time 14/ 17/	t20		9, 10, 11	All	0		ns
SDCAS* output delay 17/	t21		9, 10, 11	All	2	8	ns
SDCS*[1:0], SDRAS*, SDWE* and SDDQM*[3:0] output delay 17/	t22		9, 10, 11	All	1.5	8.5	ns
BEXC* setup time 14/ 17/	t23		9, 10, 11	All	4.5		ns
BEXC* hold time 14/ 17/	t24		9, 10, 11	All	0		ns
PIO[15:0] output delay 17/ 18/	t25		9, 10, 11	All	1.5	10	ns
PIO[15:0] setup time 14/ 15/	t26		9, 10, 11	All	5		ns
PIO[15:0] hold time during load 14/ 17/	t27		9, 10, 11	All	0		ns
PIO[15:0] hold time during write 14/ 17/ 19/	t28		9, 10, 11	All	2.5		ns

See notes at the end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Processor AC Timing - Maximum skew SKEW[1:0]='10'							
CLK period with PLL disabled 15/	t1	See Figure 5.	9, 10, 11	All	12		ns
CLK period with PLL enable 14/	t1_p		9, 10, 11	All	48	50	ns
CLK low or high pulse width PLL disabled	t2		9, 10, 11	All	5.4		ns
CLK low or high pulse width PLL enable 14/	t2_p		9, 10, 11	All	21		ns
SDCLK period 14/	t3		9, 10, 11	All	10		ns
SDCLK output delay - PLL disabled 16/	t4		9, 10, 11	All	3	8	ns
PLL setup time 15/ 20/	t5		9, 10, 11	All		10^7	ns
Reset pulse width 15/	t6		9, 10, 11	All	1*t3		ns
A[27:0] output delay 17/	t10		9, 10, 11	All	1.5	9	ns
D[31:0] and CB[7:0] Output delay 17/	t11		9, 10, 11	All	2	9.5	ns
D[31:0] and CB[7:0] Setup time 17/	t12		9, 10, 11	All	4		ns
D[31:0] and CB[7:0] hold time during load/fetch 17/ 18/	t13		9, 10, 11	All	0		ns
D[31:0] and CB[7:0] hold time during write 14/ 17/ 19/	t14		9, 10, 11	All	1	11	ns
OE*, READ and WRITE* output delay 17/	t15		9, 10, 11	All	1	7.5	ns
ROMS*[1:0] output delay 17/	t16		9, 10, 11	All	2	8	ns
RAMS*[4:0], RAMOE*[4:0] and RWE*[3:0] output delay 17/	t17		9, 10, 11	All	1.5	7	ns
IOS* output delay 17/ 18/	t18		9, 10, 11	All	2	7	ns
BRDY* setup time 14/ 17/	t19		9, 10, 11	All	5		ns
BRDY* hold time 14/ 17/	t20		9, 10, 11	All	0		ns
SDCAS* output delay 17/	t21		9, 10, 11	All	2	10	ns
SDCS*[1:0], SDRAS*, SDWE* and SDDQM*[3:0] output delay 17/	t22		9, 10, 11	All	1.5	9.5	ns

See notes at the end of table.

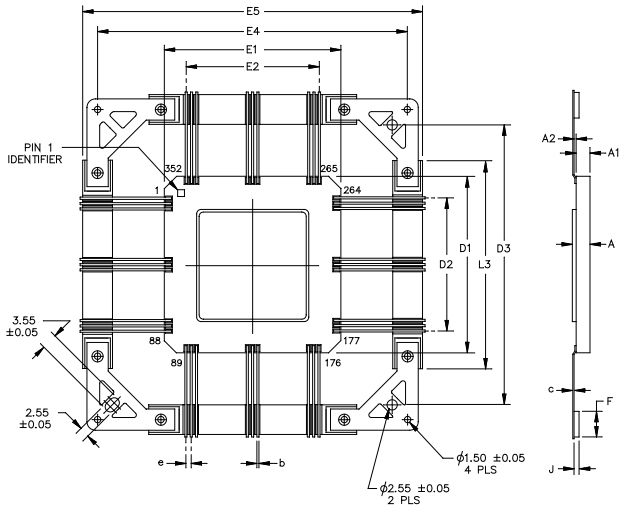
TABLE I. Electrical performance characteristics – Continued. 1/ 2/

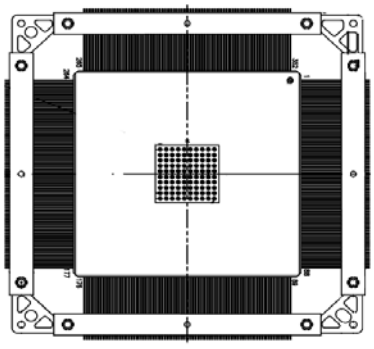
Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ $1.65V < PROC\_V_{DD18} < 1.95V$ $1.65V < FPGA\_V_{DD18} < 1.95V$ $3.0V < PROC\_V_{CC33} < 3.6V$ $3.0V < FPGA\_V_{CC33} < 3.6V$ Output load: 50 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Processor AC Timing - Maximum skew SKEW[1:0]='10' – Continued.							
BEXC* setup time 14/ 17/	t23		9, 10, 11	All	4.5		ns
BEXC* hold time 14/ 17/	t24		9, 10, 11	All	0		ns
PIO[15:0] output delay 17/ 18/	t25		9, 10, 11	All	1.5	11	ns
PIO[15:0] setup time 14/ 15/	t26		9, 10, 11	All	5		ns
PIO[15:0] hold time during load 14/ 17/	t27		9, 10, 11	All	0		ns
PIO[15:0] hold time during write 13/ 16/ 19/	t28		9, 10, 11	All	2.5		ns

1/ AC/Timing parameters (subgroup 9, 10, 11) are not directly tested but fully characterized (see note 2/), which are published on device manufacturer's data sheet and implemented in manufacturer's software (Table IIA note 8/ herein). All the timings are given at the worst case corner.
- All input I/O characteristics measured from V_{IH} of 50% of V_{CC2} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC2}.
- All output I/O characteristics are measured as the average of T_{PDLH} and T_{PDHL} to the pad V_{IH} of 50% of V_{CC2}.
- Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC2}.
- Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

2/ Characterization data is taken at initial device introduction and repeated after any design or process changes that may affect the related parameters.
3/ All tests shall be performed under the worst-case condition unless otherwise specified.
4/ Applies to DSUBRE, DSURX, DSUEN, BEXC*, BRDY*, CLK, RESET* and reconfigurable unit IOx (if not programmed with pull)
5/ Applies to reconfigurable unit I/Ox pins (if programmed with pull)
6/ Applies to TDI, TMS, TRST.
7/ Applies to TCK, BYPASS, and SKEW [0:1].
8/ Applies to CB[7:0], D[31:0], PIO[15:0] and reconfigurable unit IOs (if not programmed with pull)
9/ Applies to WDOG*, ERROR*.
10/ This value is not tested and for information only
11/ Applies to CLKDIV4, SDCLK, DSUACT, A[27:0], SDCS*[1:0], SDRAS*, SDWEN, OE*, ROM*[1:0], SDCAS* , RAMOE*[4:0], RAMS* [4:0], READ, CB [7:0], D [31:0], RWE* [3:0], WRITE*, IOS*, WDOG*, PIO [15:0], SDDQM [3:0], DSUTX and reconfigurable unit I/Ox pins.
12/ Applies to SDCLK, DSUACT, A [27:0], SDCS*[1:0], SDRAS*, SDWEN, OE*, ROM*[1:0], SDCAS*, RAMOE*[4:0], RWE*[3:0] , RAMS*[4:0], READ, CB [6:0], D [31:0], WRITE*, IOS*, PIO [15:0], SDDQM [3:0], DSUTX and reconfigurable unit I/Ox pins.
13/ Tested at initial design and after major process changes, otherwise guaranteed.
14/ Parameters are guaranteed by simulation, but not tested
15/ Not recorded – tested go/nogo during functional test.
16/ Delay given with reference to CLK.
17/ Delay given with reference to SDCLK (rising edge).
18/ Not recorded – tested during AC tests.
19/ The given timing indicate when the buffer is not driving any level on the bus. This timing is independent of the capacitive load.
20/ Although the processor is being reset asynchronously, this timing is a minimum requirement to guarantee a proper reset of the processor: a glitch of any shorter duration may lead to an unpredictable behavior.

Case outline X





Bottom 2/

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	3.09	3.14	D3	65.89 REF.	
A1	2.40	2.94	E4	70.00 REF.	
B	0.15	0.25	E5	74.87	76.01
C	0.10	0.20	E	0.45	0.55
D1/E1	47.67 SQ.	48.33 SQ.	F	4.5	5.5
D2/E2	43.37	43.63	J	0.75	1.05

NOTES:

1/ Lid is connected to ground

2/ The bottom pads are used only for manufacturing purpose, and must be left unconnected for end user application. It is recommended not to have routing under the pad area.

FIGURE 1. Case outline.

Case outline X

Pin Number	Pin name	Pin Number	Pin name	Pin Number	Pin name	Pin Number	Pin name
1	IO482_GCK5	45	LVDS_REF_B	89	IO705	133	V_{SS}
2	IO487	46	IO599_OLVDSB1	90	IO707	134	V_{SS}
3	IO493	47	IO600_OLVDSB1N	91	IO711	135	BEXC*
4	IO497	48	IO603_OLVDSB2	92	IO713_D0	136	SKEW [0]
5	IO503	49	IO604_OLVDSB2N	93	IO717	137	SKEW [1]
6	IO505	50	V_{SS}	94	V_{SS}	138	DSURX
7	IO507	51	IO605	95	IO720_GCK6_CSOUT	139	DSUTX
8	IO511	52	IO607	96	IO722_GCK7	140	DSUEN
9	IO513	53	IO611	97	FPGA_V_{DD18}	141	DSUBRE
10	IO517	54	IO613	98	V_{SS}	142	DSUACT
11	IO519	55	IO617	99	IO725	143	BYPASS
12	IO523	56	IO619	100	CCLK	144	CLK
13	IO525	57	IO623	101	IO727	145	PROC_V_{CC33}
14	IO527	58	IO625	102	IO731	146	V_{SS}
15	IO531	59	IO627	103	IO733	147	LOCK
16	IO533	60	IO633	104	IO737	148	PROC_RESET*
17	FPGA_V_{DD18}	61	IO637	105	IO739	149	ERROR*
18	V_{SS}	62	IO639	106	IO743	150	WDOG*
19	IO537	63	IO643	107	IO745	151	M1
20	IO539	64	IO645	108	IO747	152	M0
21	IO543_FCK3	65	FPGA_V_{CC33}	109	IO751	153	M2
22	IO545	66	V_{SS}	110	IO753	154	WRITE*
23	IO547_CS0*	67	IO647	111	IO757	155	READ
24	IO551	68	IO651	112	IO759	156	ROMS*[0]
25	IO553	69	IO653	113	FPGA_V_{CC33}	157	ROMS*[1]
26	IO557	70	IO655_CHECK*	114	V_{SS}	158	BRDY*
27	IO559	71	IO658_FCK4	115	IO763	159	OE*
28	IO563	72	IO661	116	IO765	160	IOS*
29	IO565	73	IO665	117	IO767	161	FPGA_V_{DD18}
30	IO567	74	IO667	118	IO771	162	V_{SS}
31	IO571	75	IO673	119	IO773	163	RWE*[0]
32	IO573	76	IO679	120	IO777	164	RWE*[1]
33	FPGA_V_{CC33}	77	IO685	121	IO779	165	RWE*[2]
34	V_{SS}	78	IO671	122	IO783	166	RWE*[3]
35	IO577	79	IO677	123	IO785	167	RAMOE*[0]
36	FPGA_V_{DD18}	80	IO683	124	IO787	168	RAMOE*[1]
37	IO579	81	FPGA_V_{DD18}	125	IO791	169	RAMOE*[2]
38	IO583	82	V_{SS}	126	IO793	170	RAMOE*[3]
39	IO585	83	IO687	127	IO1_GCK1	171	RAMOE*[4]
40	IO591	84	IO693	128	IO960_GCK8	172	RAMS*[0]
41	IO593_ILVDSB1	85	IO691	129	FPGA_V_{DD18}	173	RAMS*[1]
42	IO594_ILVDSB1N	86	IO697	130	V_{SS}	174	RAMS*[2]
43	IO597_ILVDSB2	87	IO699	131	V_{SS}	175	RAMS*[3]
44	IO598_ILVDSB2N	88	IO703	132	V_{SS}	176	RAMS*[4]

FIGURE 2. Terminal connections.

Pin Number	Pin name	Pin Number	Pin name	Pin Number	Pin name	Pin Number	Pin name
177	FPGA_V_{DD18}	221	D[30]	265	A[26]	309	IO373
178	V_{SS}	222	D[31]	266	A[27]	310	IO377
179	CB[0]	223	SDCAS*	267	GPIO[0]	311	IO379
180	CB[1]	224	SDCLK	268	GPIO[1]	312	IO383
181	CB[2]	225	PROC_V_{CC33}	269	GPIO[2]	313	IO385
182	CB[3]	226	V_{SS}	270	GPIO[3]	314	IO387
183	CB[4]	227	SDCS*[0]	271	GPIO[4]	315	IO397
184	CB[5]	228	SDCS*[1]	272	GPIO[5]	316	IO393
185	CB [6]	229	SDDQM[0]	273	FPGA_V_{DD18}	317	IO399
186	CB[7]	230	SDDQM[1]	274	V_{SS}	318	IO403
187	D[0]	231	SDDQM[2]	275	GPIO[6]	319	IO405
188	D[1]	232	SDDQM[3]	276	GPIO[7]	320	IO407
189	D[2]	233	SDRAS*	277	GPIO[8]	321	FPGA_V_{CC33}
190	D[3]	234	SDWE*	278	GPIO[9]	322	V_{SS}
191	D[4]	235	A[0]	279	GPIO[10]	323	IO411
192	D[5]	236	A[1]	280	GPIO[11]	324	IO413
193	PROC_V_{DD18}	237	A[2]	281	GPIO[12]	325	IO417
194	V_{SS}	238	A[3]	282	GPIO[13]	326	IO419
195	D[6]	339	A[4]	283	GPIO[14]	327	IO423
196	D[7]	240	A[5]	284	GPIO [15]	328	IO425
197	D[8]	241	PROC_V_{DD18}	285	PROC_V_{DD_PLL}	329	IO427
198	D[9]	242	V_{SS}	286	PROC_V_{SS_PLL}	330	IO431
199	D[10]	243	A[6]	287	IO225_OTS	331	IO433
200	D[11]	244	A[7]	288	IO240_GCK2	332	IO437
201	D[12]	245	A[8]	289	PROC_V_{CC33}	333	IO439
202	D[13]	246	A[9]	290	V_{SS}	334	IO443
203	D[14]	247	A[10]	291	IO241_GCK3	335	IO445
204	D[15]	248	A[11]	292	IO259_LDC	336	IO447
205	D[16]	249	A[12]	293	IO265_HDC	337	FPGA_V_{DD18}
206	D[17]	250	A[13]	294	IO303_INIT	338	V_{SS}
207	D[18]	251	A[14]	295	IO353_ILVDSA1	339	IO453
208	D[19]	252	A[15]	296	IO354_ILVDSA1N	340	IO457
209	PROC_V_{DD18}	253	A[16]	297	IO357_ILVDSA2	341	IO459
210	V_{SS}	254	A[17]	298	IO358_ILVDSA2N	342	IO463
211	D[20]	255	A[18]	299	LVDS_REF_A	343	IO465
212	D[21]	256	A[19]	300	IO359_OLVDSA1	344	IO467
213	D[22]	257	PROC_V_{DD18}	301	IO360_OLVDSA1N	345	IO471
214	D[23]	258	V_{SS}	302	IO363_OLVDSA2	346	IO473
215	D[24]	259	A[20]	303	IO364_OLVDSA2N	347	IO477
216	D[25]	260	A[21]	304	IO365	348	CON
217	D[26]	261	A[22]	305	FPGA_V_{DD18}	349	IO480_GCK4
218	D[27]	262	A[23]	306	V_{SS}	350	IO485
219	D[28]	263	A[24]	307	IO367	351	IO491
220	D[29]	264	A[25]	308	IO371	352	FPGA_RESET*

FIGURE 2. Terminal connections. – continued

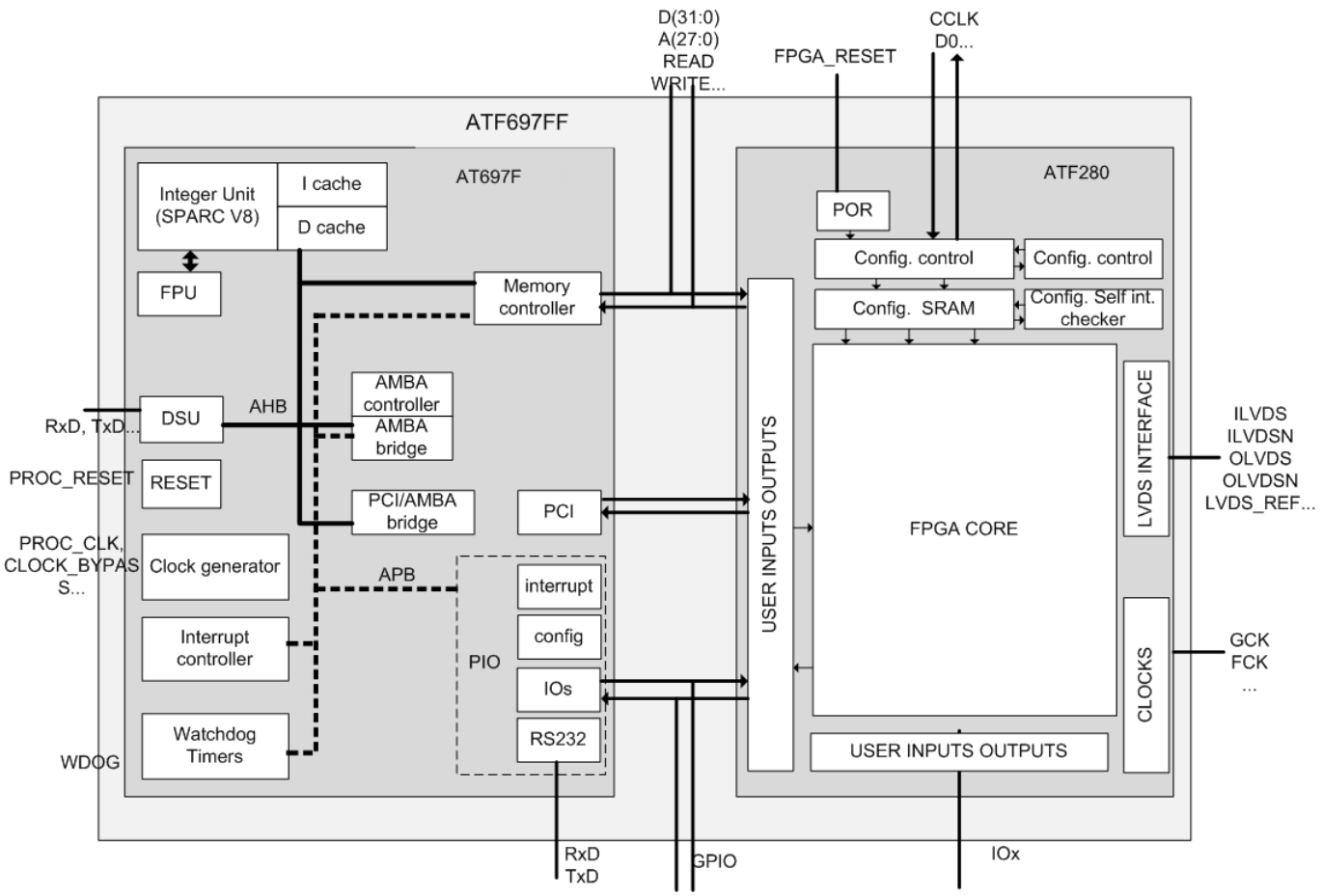
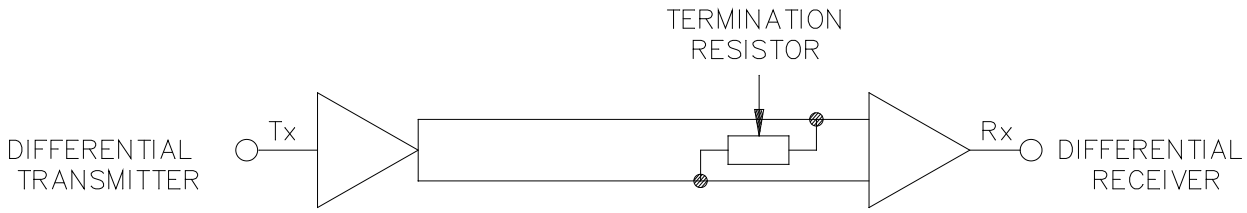


FIGURE 3. Block diagram.

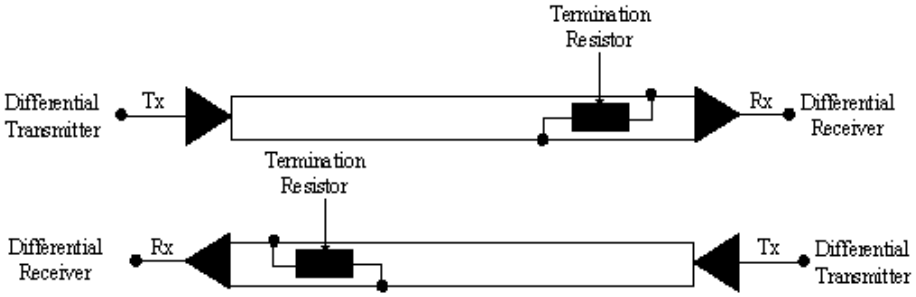
LVDS basic interface



The LVDS I/Os embedded on the ATF697FF are composed of 4 LVDS transceiver (Tx) pairs, 4 receivers (Rx) pairs together with the reference voltages (LVDS_REF_A and LVDS_REF_B). That must be connected to an accurate 1.25V voltage to give references to the transceivers and to the receivers. They are spread in 2 clusters, each one consisting in

- 2x transceivers
- 2x receivers
- 1x reference voltage.

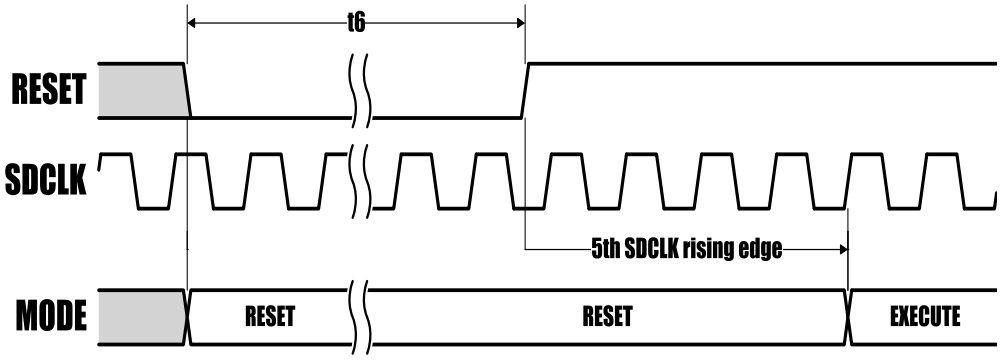
LVDS bidirectional communication principle



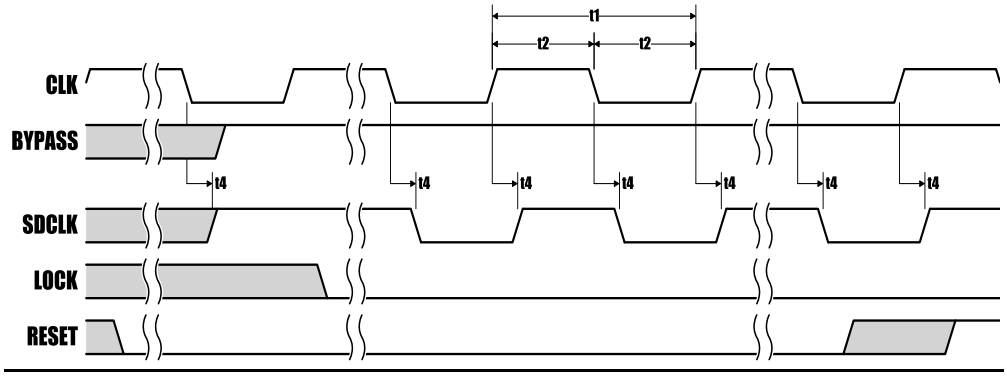
The LVDS_REF_B is the reference voltage for LVDSB1 and LVDSB2.
The LVDS_REF_A is the reference voltage for LVDSA1 and LVDSA2.

FIGURE4. LVDS interface.

Processor: Reset sequence:



Processor: Clock input without PLL



Processor: Clock input with PLL

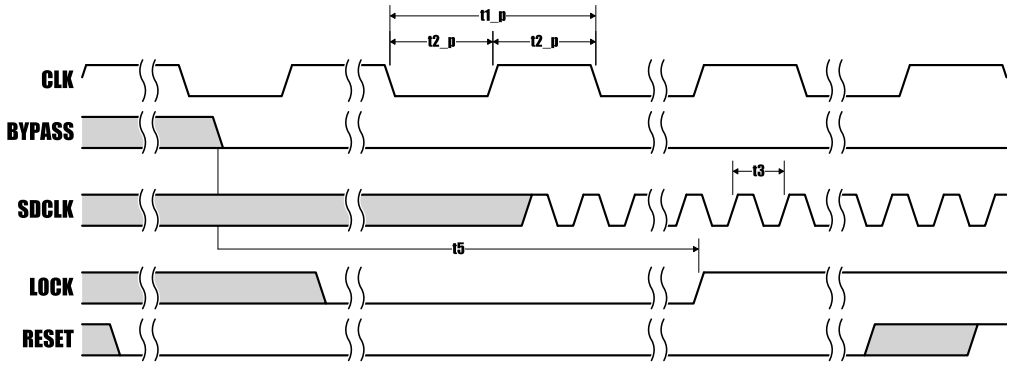
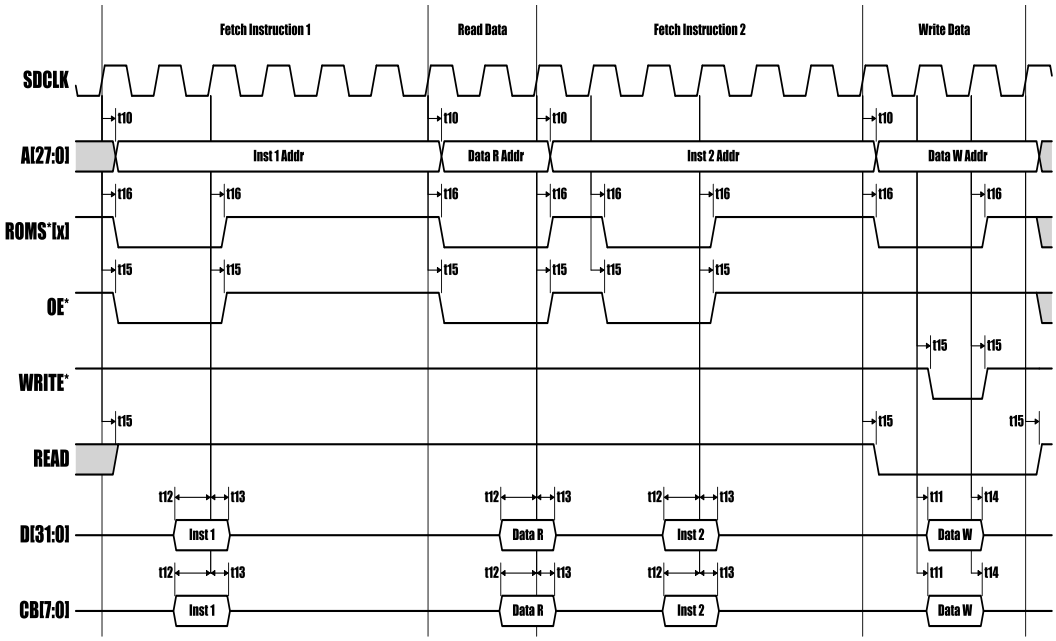


FIGURE 5. Timing waveforms

Processor: Fetch, Read and Write from 32-bit PROM 0 wait-states



Processor: Fetch, Read and Write from 32-bit PROM 2n wait-states

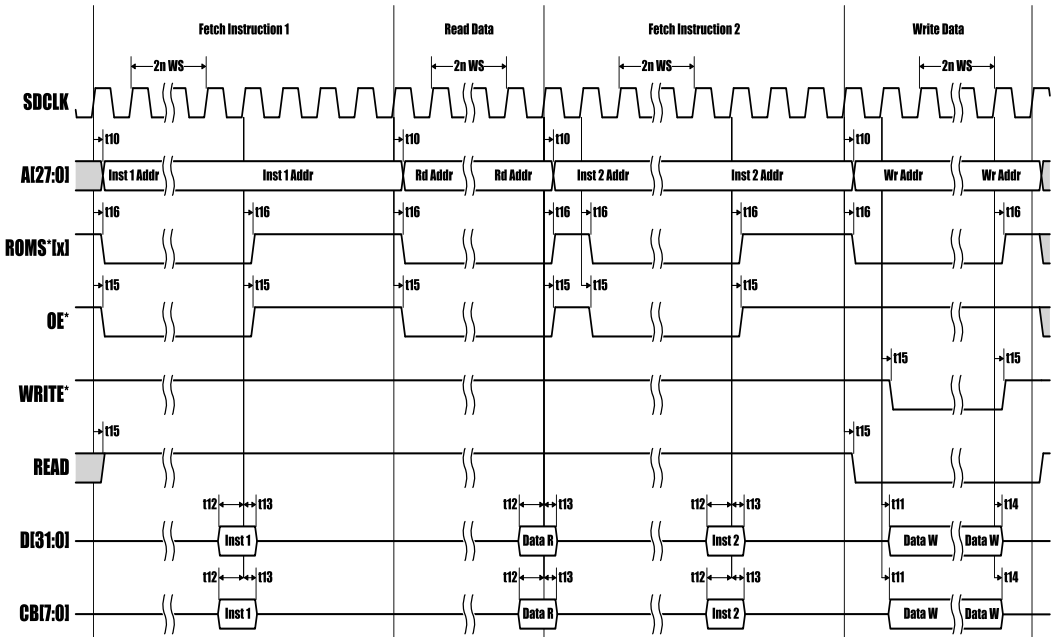


FIGURE 5. Timing waveforms – continued.

Processor: Fetch, Read and Write from 32-bit PROM 2n wait-states + BRDY*

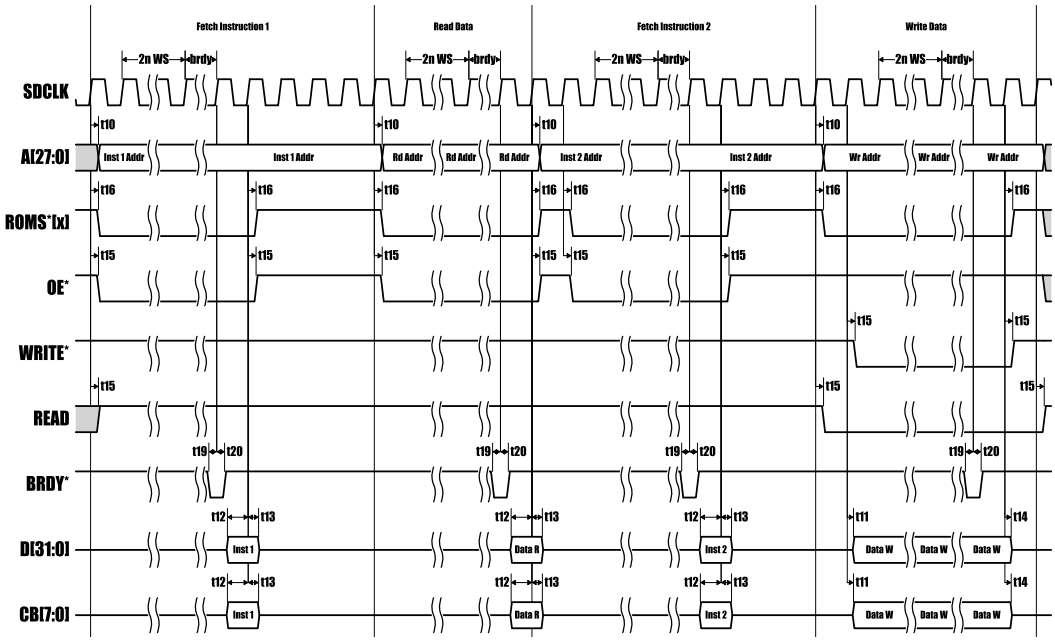
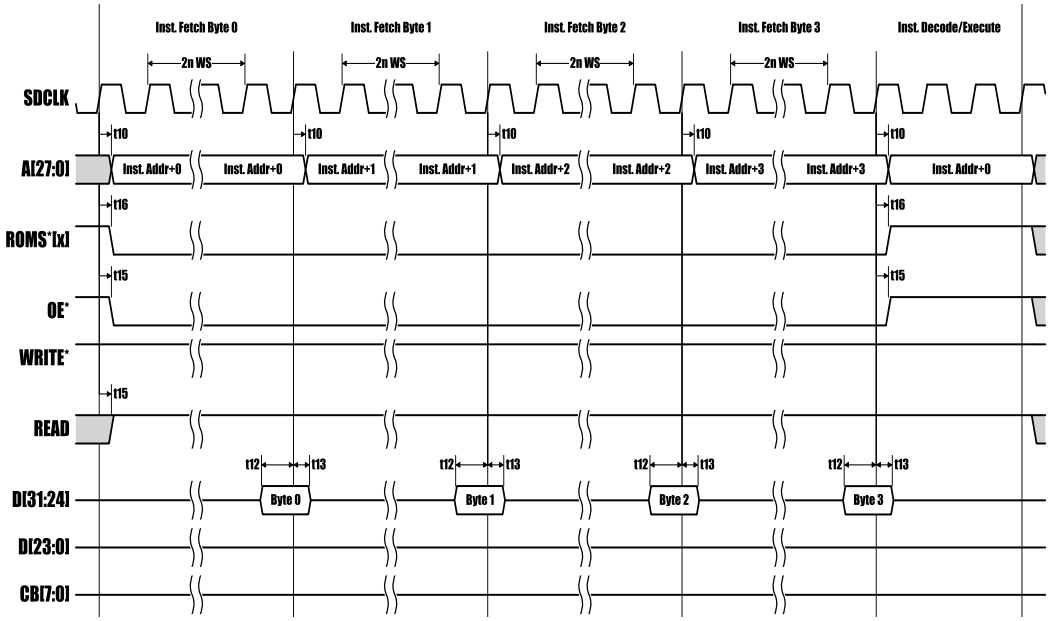


FIGURE 5. Timing waveforms – continued.

Processor: Fetch from 8-bit PROM with EDAC disabled 2n wait-states



Processor: Word Write to 8-bit PROM with EDAC disabled 2n wait-states

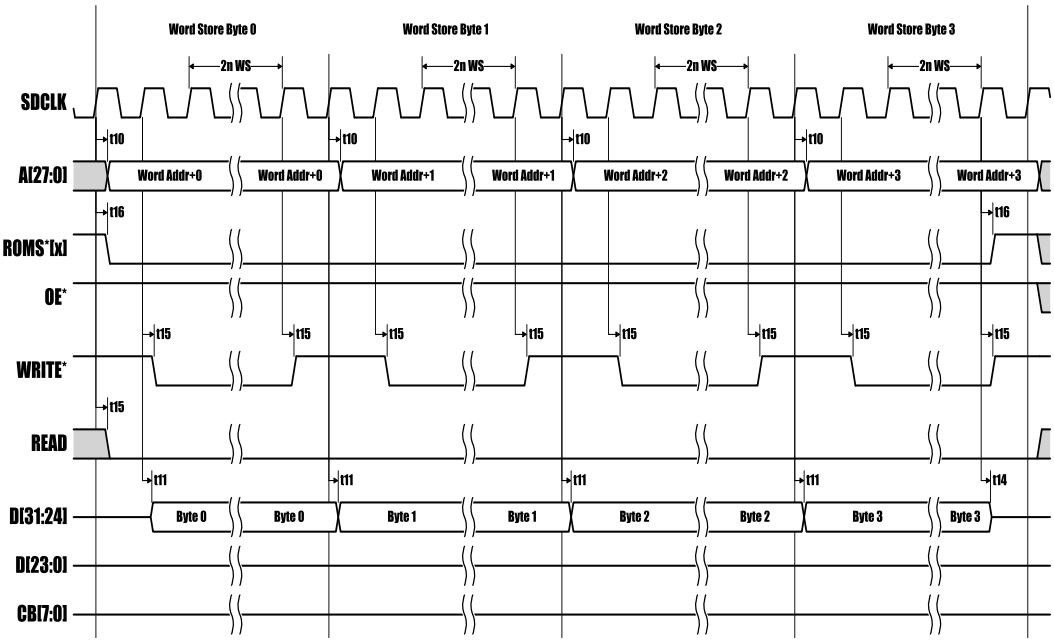
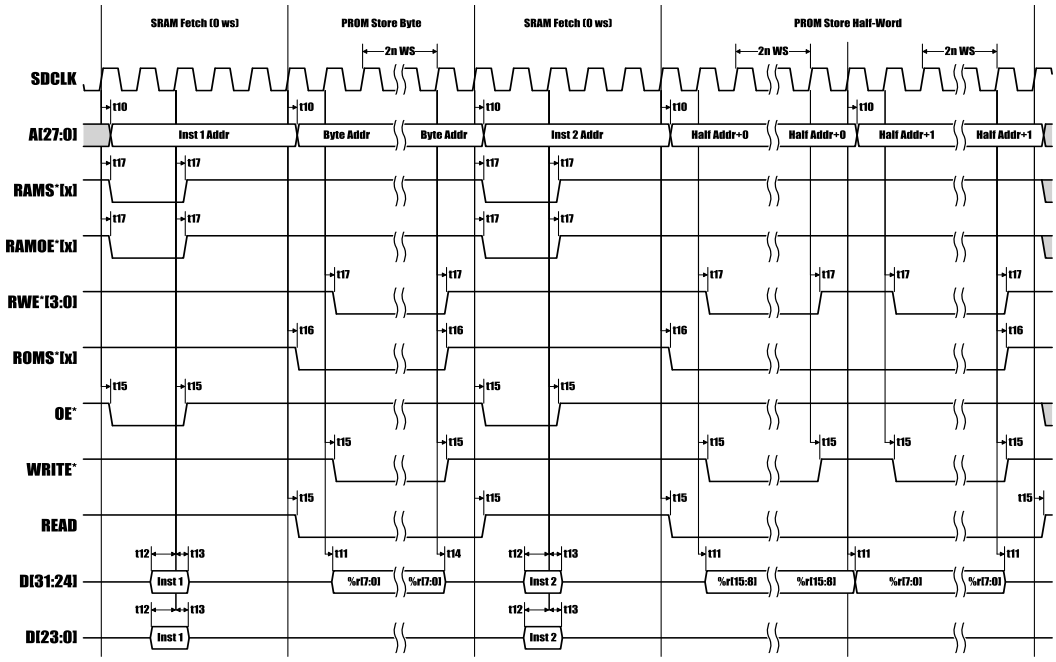


FIGURE 5. Timing waveforms – continued.

Processor: Byte and Half-Word Write to 8-bit PROM with EDAC disabled 2n wait-states



Processor: Fetch from 8-bit PROM with EDAC enabled 2n wait-states

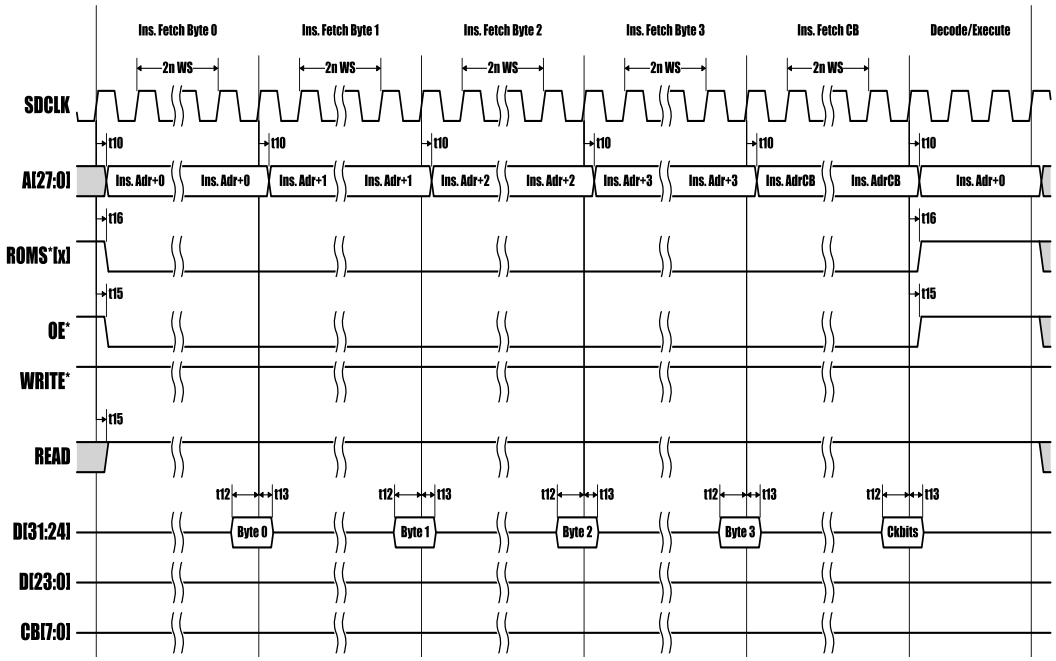
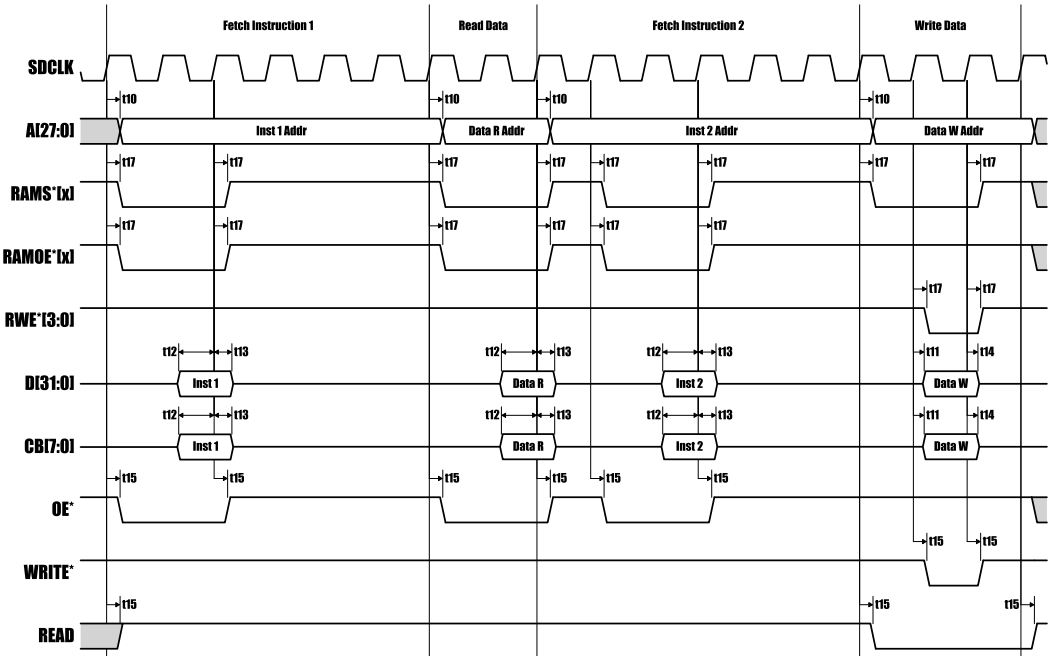


FIGURE 5. Timing waveforms – continued.

Processor: Fetch, Read and Write from/to 32-bit SRAM 0 wait-states



Processor: Fetch, Read and Write from/to 32-bit SRAM n wait-states

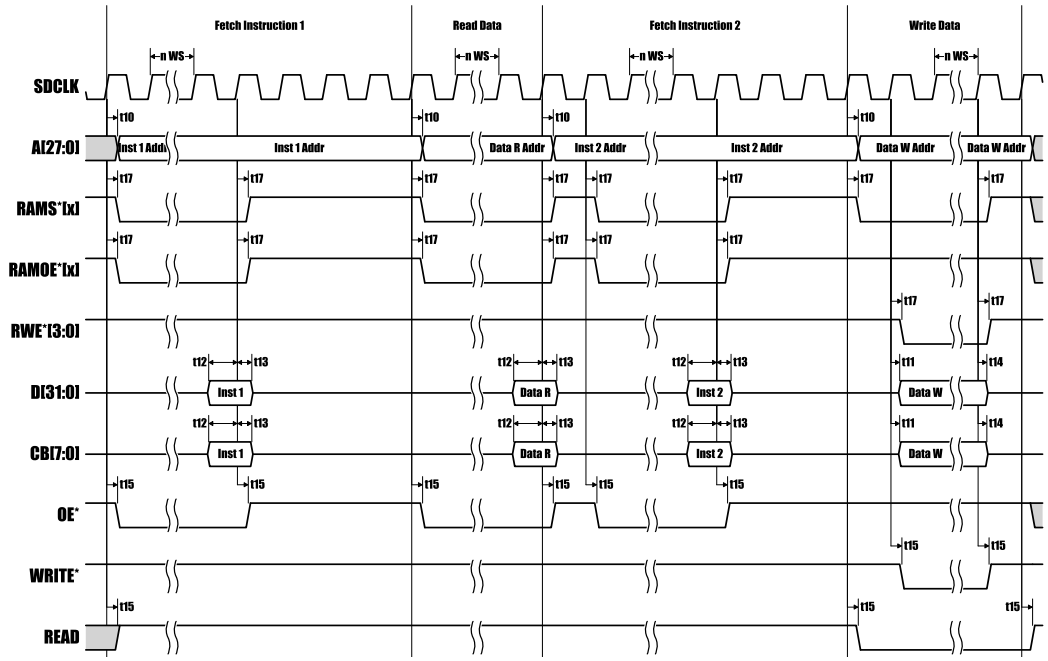
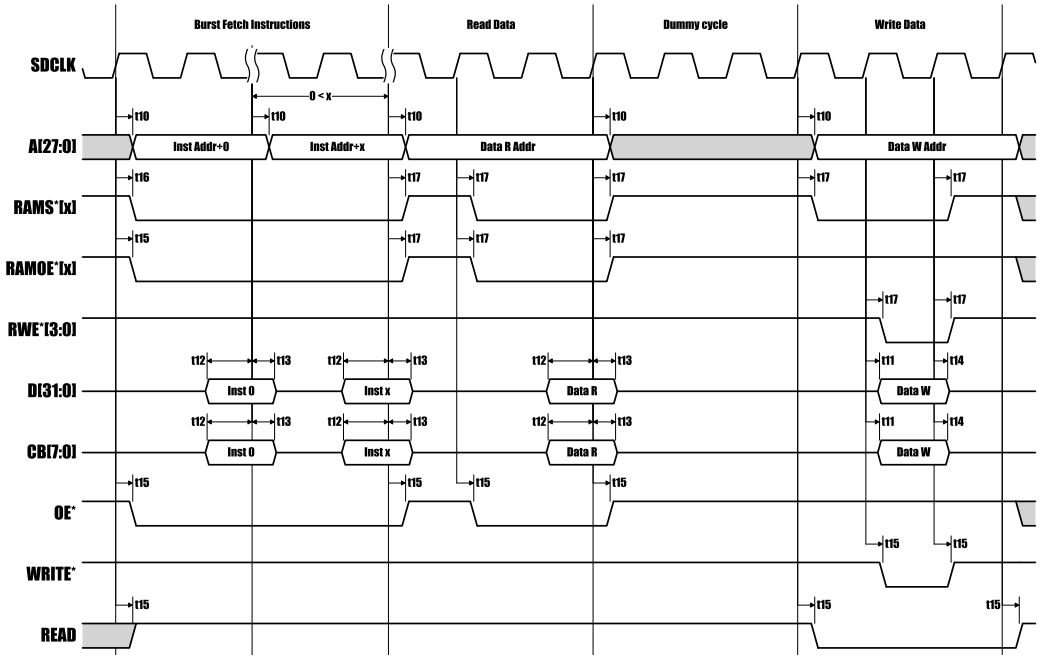


FIGURE 5. Timing waveforms – continued.

Processor: Fetch, Read and Write from/to 32-bit SRAM with Instruction Burst 0 wait-states



Processor: Fetch, Read and Write from/to 32-bit SRAM with Instruction Burst n wait-states

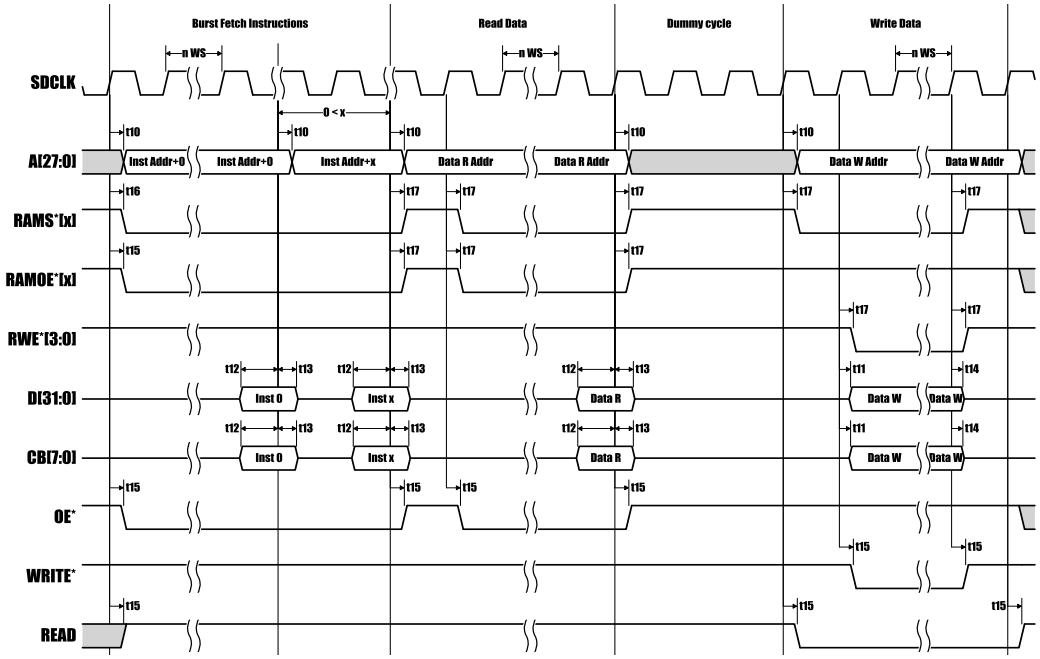
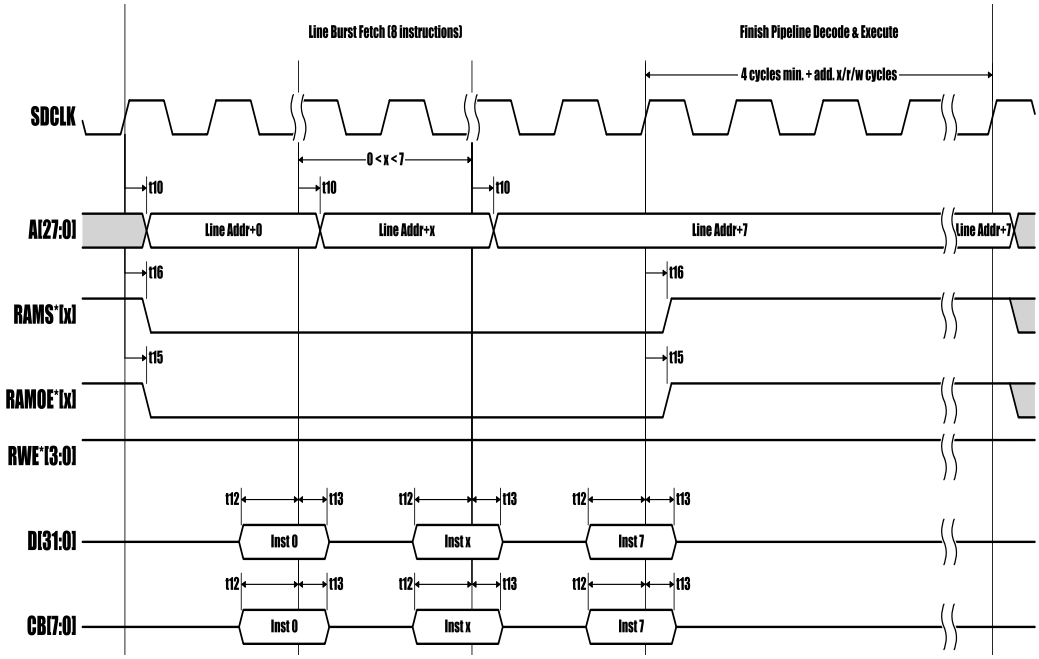


FIGURE 5. Timing waveforms – continued.

Processor: Burst of SRAM Fetches with Instruction Cache and Burst enabled 0 wait-states



Processor: Burst of SRAM Fetches with Instruction Cache and Burst enabled n wait-states

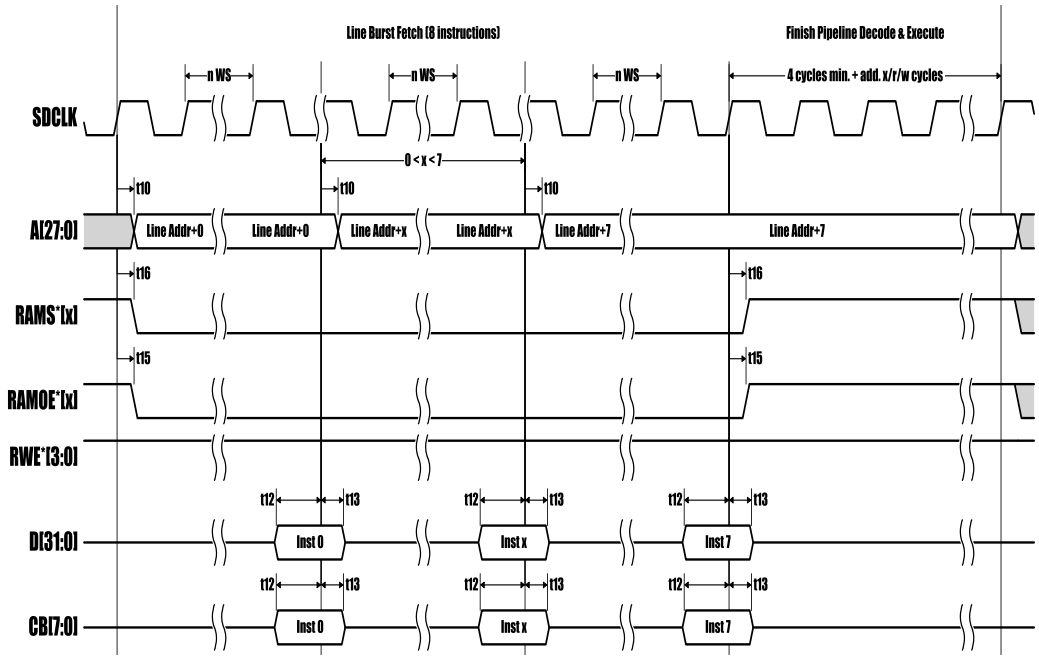
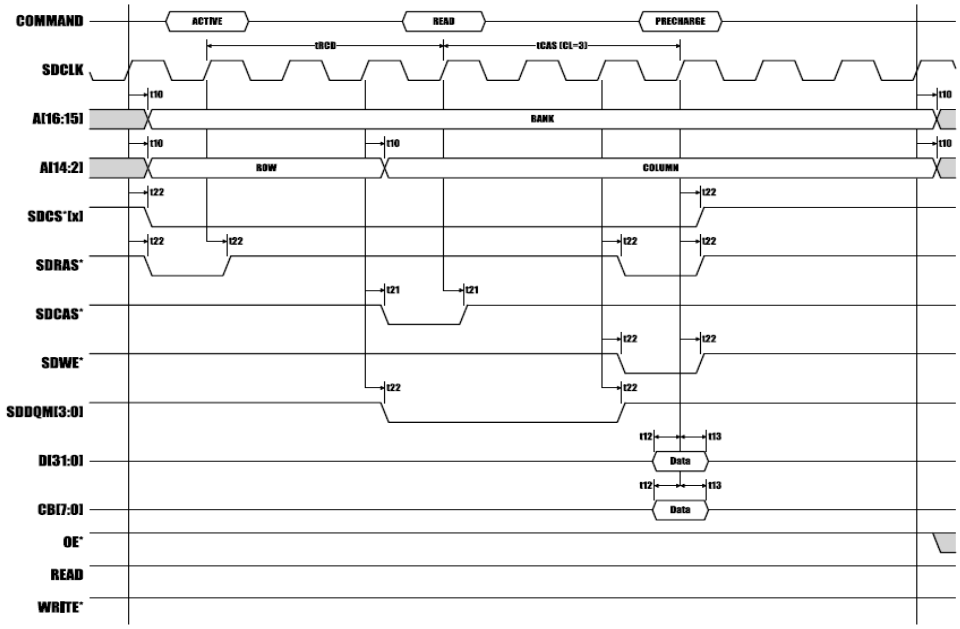


FIGURE 5. Timing waveforms – continued.

Processor: SDRAM read (or Fetch) with Precharge Burst length = 1; CL = 3



Processor: SDRAM write with Precharge Burst length = 1; CL = 3

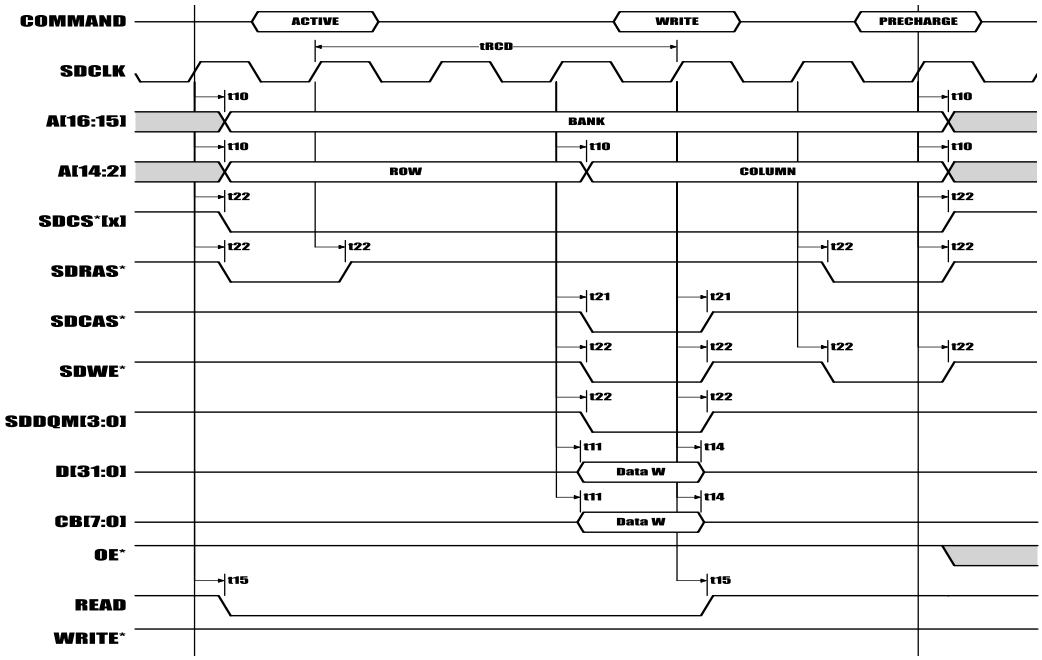
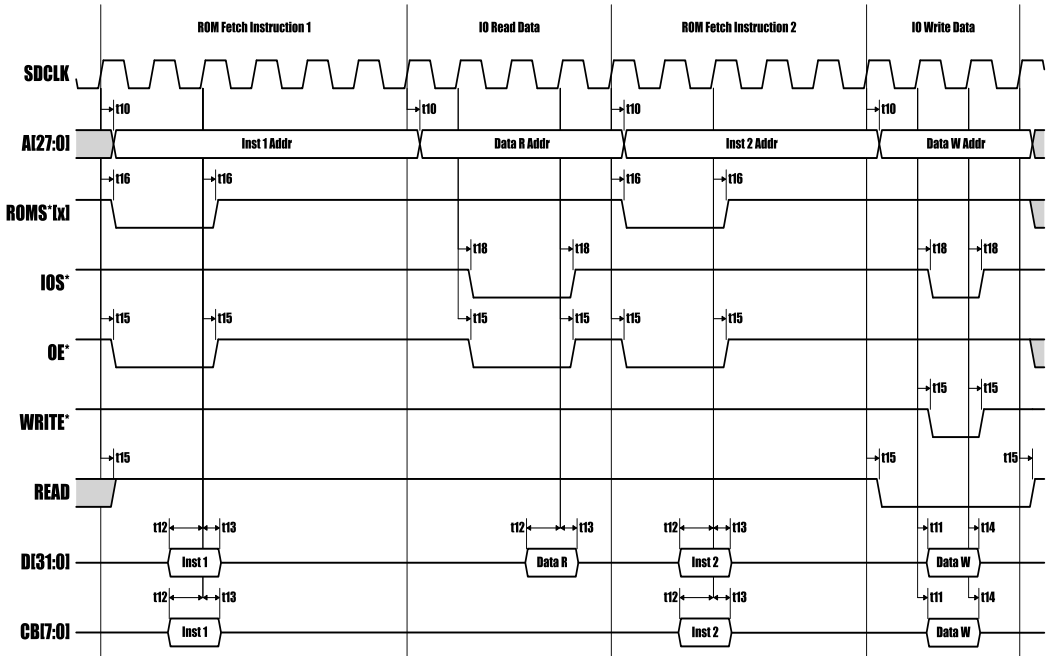


FIGURE 5. Timing waveforms – continued.

Processor: Fetch from ROM, Read and Write from/to 32-bit I/O 0 wait-states



Processor: Fetch from ROM, Read and Write from/to 32-bit I/O n wait-states

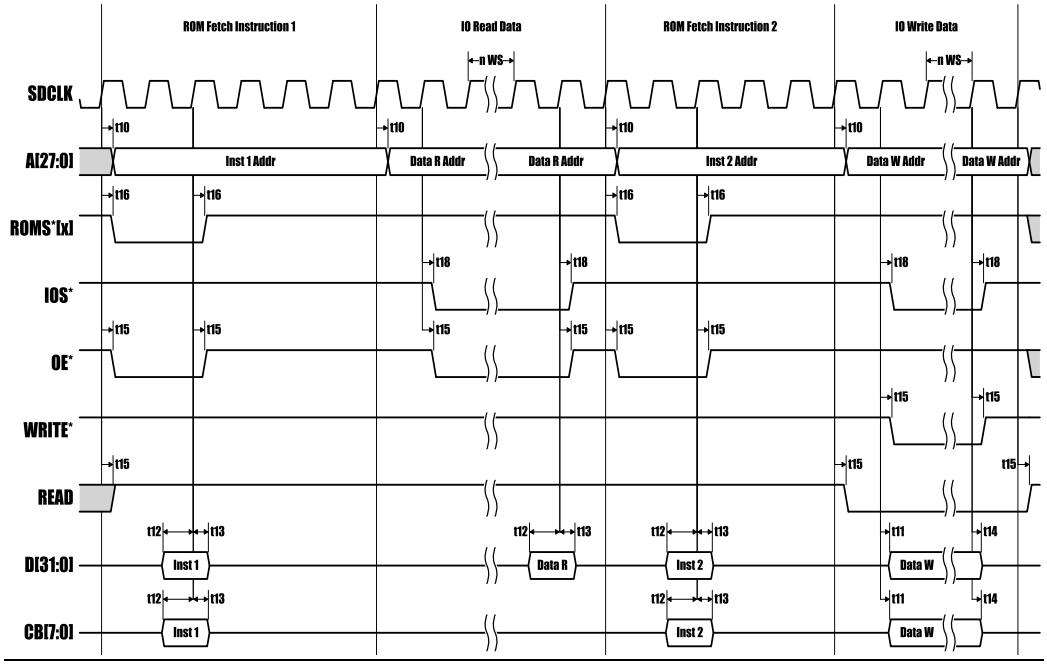


FIGURE 5. Timing waveforms – continued.

Processor: Fetch from ROM, Read and Write from/to 32-bit I/O n wait-states + sync. BRDY*

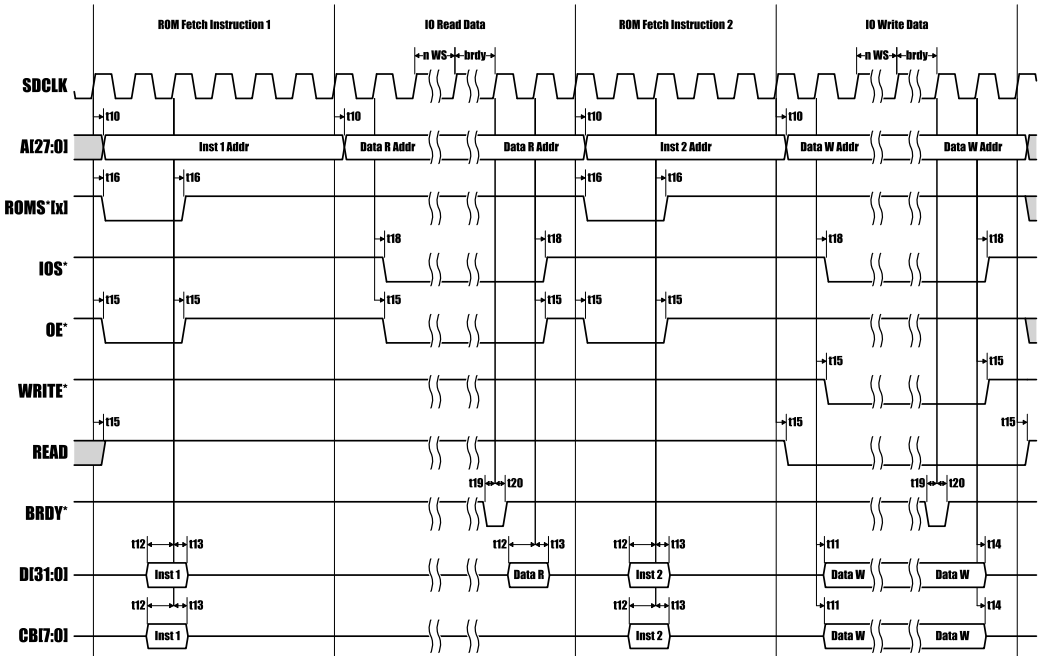
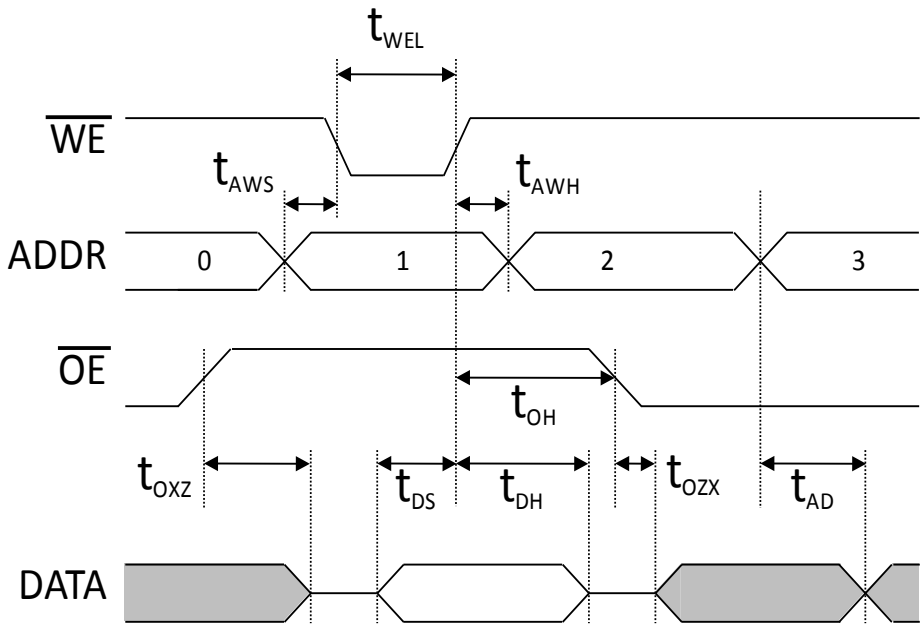


FIGURE 5. Timing waveforms – continued.

Reconfigurable unit: Single port Write/Read



Reconfigurable unit: Dual-port Write with Read

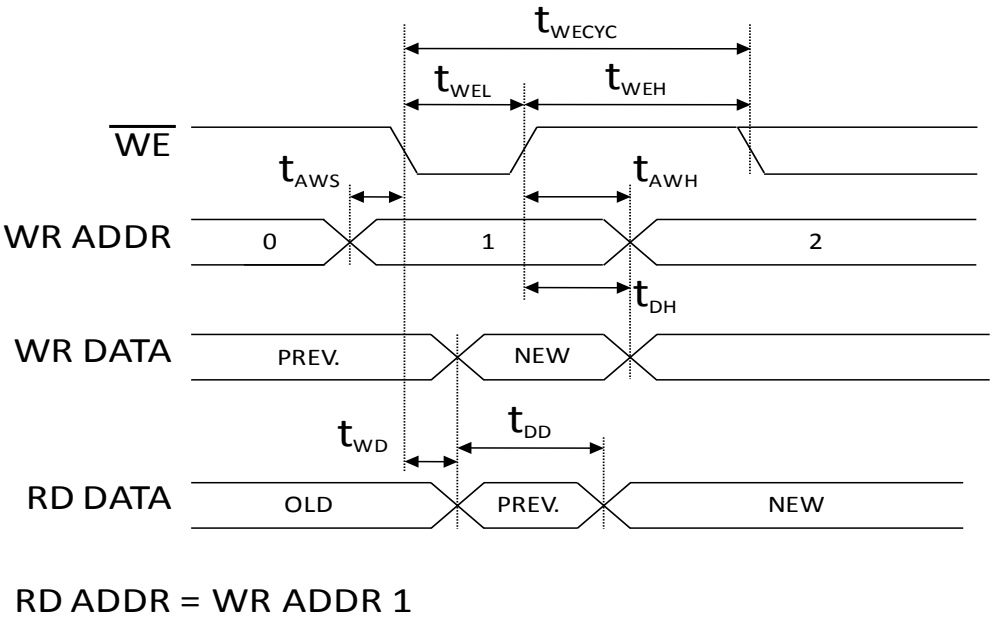
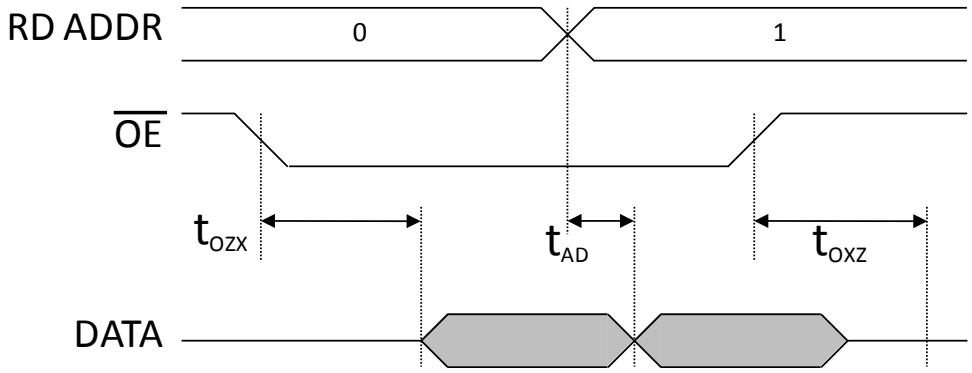


FIGURE 5. Timing waveforms – continued.

Reconfigurable unit: Dual-port Read



Reconfigurable unit: Single-port Write/ Read

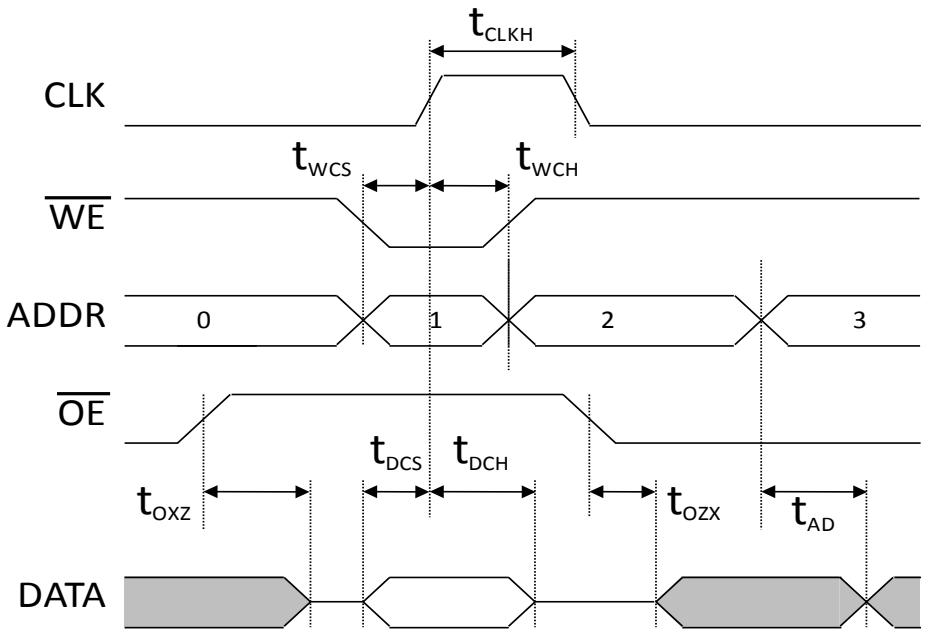
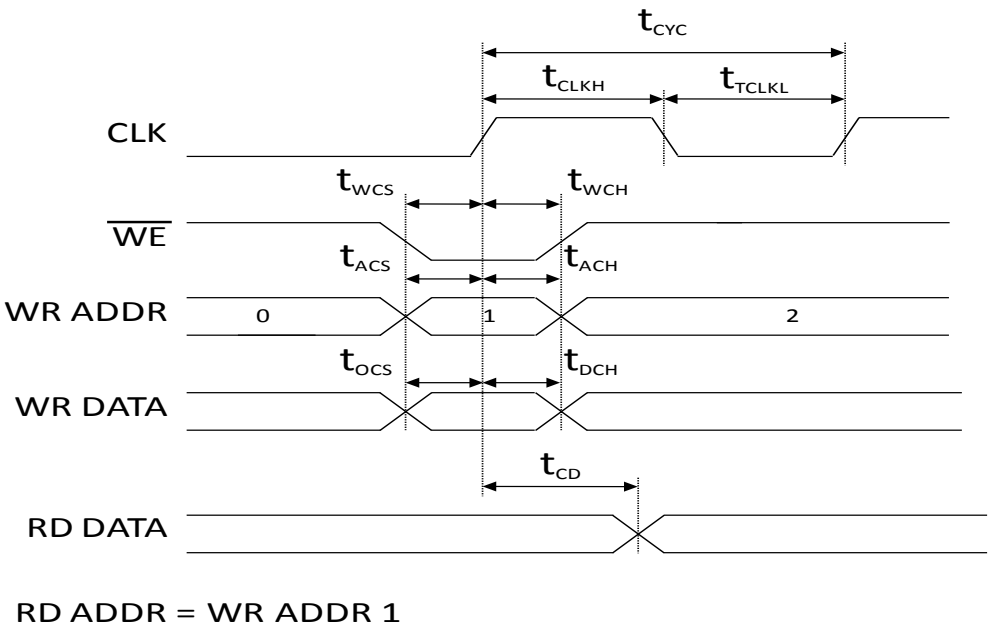


FIGURE 5. Timing waveforms – continued.

Reconfigurable unit: Dual-port Write with Read



Reconfigurable unit: Dual-port Read

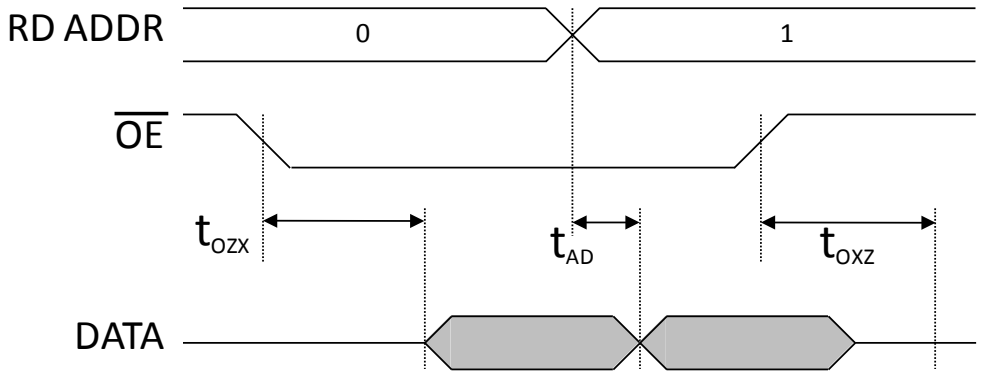


FIGURE 5. Timing waveforms – continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein..

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is on a minimum of three devices with no failures on a minimum of five worst case pins from each device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9 1/ 2/
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11 3/	1, 2, 3, 4, 7, 8, 9, 10, 11, 1/ 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11 3/	1, 2, 3, 4, 7, 8, 9, 10, 11 3/
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11 3/	1, 2, 3, 7, 8, 9, 10, 11 1/ 2/ 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9 3/	1, 7, 9 3/
Group E end-point electrical parameters (see 4.4)	1, 7, 9 3/	1, 7, 9 3/

1/ PDA applies to subgroup 1 and 7.

2/ Δ delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.

3/ Subgroups 9,10, and 11 switching parameters, if not provided in table I, shall be designated by device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be maintained under document revision level control, and shall be made available to the acquiring or preparing activity upon request.

TABLE IIB. Burn-in and operating life test delta limits (+25°C).

Parameter 1/	**Limit**	**Unit**
V_{OL}/V_{OH}	+/- 0.1	V
I_{IL}/I_{IH}	+/- 0.1	µA
I_{OZL}/I_{OZH}	+/- 0.1	µA
I_{CCSB}	5	mA
I_{CCSB1}	5	mA

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

TABLE III. Pin descriptions.

Pin	Function 1/
PROC_RESET* Processor reset (input)	[SI] When asserted, this asynchronous active low input immediately halts and resets the processor and all on-chip peripherals. The processor restarts execution after the 5th rising edge of the clock after PROC_RESET* was de-asserted.
FPGA_RESET* reconfigurable unit reset (input)	[SI] [CFG] FPGA_RESET* is the manual reset of the FPGA. This function reset the configuration download logic. FPGA_RESET* is internally pulled up to VCC and is active at a low level. Each time FPGA_RESET* is activated, the FPGA enters Manual Reset lifephase.
ERROR* Processor error (open-drain output with pull-up)	[SI] This active low output is asserted when the processor is halted in error mode.
WDOG* Watchdog timeout (open-drain output with pull-up)	[SI] This active low output is asserted when the watchdog timer has expired and remains asserted until the watchdog timer is reloaded with a non-null value.
BEXC* Bus exception (input)	[SI]This active low input is sampled simultaneously with the data during an access to the external memory. If asserted, a memory error is generated.
M0, M1, M2 reconfigurable unit configuration mode (Input)	[SI] [CFG] The configuration mode pins are used to define the configuration settings of the ATF697FF reconfiguration unit. ATF697FF reconfiguration unit samples the configuration mode pins each time a configuration clear cycle is ended. **Caution**: the mode pins should not be changed during power-on-reset or manual reset

See notes at the end of the table.

TABLE III. Pin descriptions - Continued.

Pin	Function 1/
CCLK Reconfigurable unit configuration clock (bi-directional)	[SI] [CFG] CCLK function provides the clock signal used by the configuration logic. Depending on the mode used for configuration download procedure, CCLK function is configured as input or output. For slave mode, the CCLK is configured as an input whereas for master mode, it is configured as an output. When configured in input mode, CCLK is pulled up to VCC with an internal resistor
IO713_D0 Multiplexed General Purpose IO Configuration Data	[SI] [CFG] D0 is used to transfer configuration data from or to the FPGA onfiguration SRAM. D0 is used for serial mode configuration and can be used together with D1 to D15 for parallel mode configuration. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO303_INIT Multiplexed General Purpose IO Configuration Error Indicator	[SI] [CFG] INIT is used as an error indicator regarding configuration logic. INIT is a bidirectional open drain I/O pulled up to VCC with an internal resistor. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
CON Configuration Status Indicator	[SI] [CFG] CON is the FPGA configuration start and status pin. It is a bidirectional open drain I/O pulled up to VCC with an internal resistor.
IO265_HDC Multiplexed General Purpose IO Configuration Status Indicator	[SI] [CFG] HDC indicates that the configuration download is on-going. HDC is an output and is polarized to a high logic level during the configuration. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO259_LDC Configuration Status Indicator Multiplexed General Purpose IO	[SI] [CFG] LDC indicates that the configuration download is on-going. LDC is an output and is polarized to a low logic level during the configuration. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO547_CS0* Multiplexed General Purpose IO Serial Configuration Chip Select	[SI] [CFG] CS0 is an active low chip select used during configuration. It is only available configuration download slave serial mode 1. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO720_GCK6_CSOUT Multiplexed General Purpose IO Clock Configuration Select Output	[SI] [CFG] CSOUT is the configuration pin used to enable the downstream device in an FPGA cascade chain. [CLOCK] GCK6 function is used to provide clock signals over the entire surface of the FPGA. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO655_CHECK* Multiplexed General Purpose IO Configuration Check	[SI] [CFG] CHECK* pin is used to enable the CHECK function when combined with a configuration download start. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IO225_OTS Multiplexed General Purpose IO Tri-State Command	[SI] [CFG] OTS pin is used to tri-state all the FPGA pins configured as user I/Os. [GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
CLK Processor reference clock	[CLOCK] This input provides a reference to generate the internal clock used by the processor and the internal peripherals
BYPASS Processor PLL bypass	[PLL] This active high input is used to bypass the internal PLL. When asserted, the processor is directly clocked from the external reference clock. When de-asserted, the processor receives its clock from the internal PLL. This signal shall be kept static and free from glitches while the processor is operating, as it is not sampled internally. Changing the signal shall only be performed while the processor is under reset otherwise the processor's behavior is not predictable.

See notes at the end of the table.

TABLE III. Pin descriptions. – Continued

Pin	Function 1/
LOCK PLL lock (output)	[PLL]When asserted, this active high output indicates the PLL of the processor is locked at a frequency corresponding to four times the frequency of the external processor reference clock. Caution: this signal is de-asserted as soon as the PLL unlocks.
SKEW[1:0] Clock tree skew (input with pull-down)	[CFG]These input signals are used to programme the skew on the internal triplicated clock trees. These signals shall be kept static and free from glitches while the processor is operating, as they are not sampled internally. Changing these signals shall only be performed while the processor is under reset otherwise the processor's behavior is not predictable.
IOx_GCKy Multiplexed General Purpose IO Clock	[CLOCK] GCK function is used to provide clock signals over the entire surface of the FPGA. GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
IOx_FCKy Multiplexed General Purpose IO Clock	[CLOCK] 1 fast clock is available on the reconfigurable unit part. (The 2 pins (FCK3 & FCK4) are multiplexed all together). GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.
A[27:0] Address bus (output)	[MEM]The lower 28 bits of the 32 bit address bus carry instruction or data addresses during a fetch or a load/store operation to the external memory. The address of the last external memory access remains on the address bus whenever the current access can be made out of the internal cache.
D[31:0] Data bus (bi-directional)	[MEM]The 32-bit bi-directional data bus serves as the interface between the processor and the external memory. The data bus is only driven by the processor during the execution of integer & floating-point store instructions and the store cycle of atomic-load-store instructions. It is kept in high impedance otherwise. However: only D[31:24] are used during an access to an 8-bit area D[15:0] are used as part of the general-purpose I/O interface whenever all the memory areas (ROM, SRAM & I/O) are 8-bit wide and the SDRAM interface is not enabled
CB[7:0] Check bits (bi-directional)	[MEM]These signals carry the EDAC check bits (*) during a write access to the external memory and are kept in high impedance otherwise. This applies whatever the EDAC activation or not. Note(*) : While only 7 bits are useful for EDAC protection, CB[7] is implemented to enable programming of FLASH memories and takes the value of MCFG3.tcb[7]
OE* Output enable (output)	[MEM] This active low output is asserted during a read access to the external memory. It can be used as an output enable signal when accessing PROM & I/O devices
READ Read enable (output)	[MEM] This active high output is asserted during a read access to the external memory. It can be used as a read enable signal when accessing PROM & I/O devices.
WRITE* Write enable (output)	[MEM] This active low output is asserted during a write-access to the external memory. It can be used as a write enable signal when accessing PROM & I/O devices.
RWE*[3:0] PROM & SRAM byte write-enable (output)	[MEM] These active low outputs provide individual write strobes for each byte-lane on the data bus: RWE*[0] controls D[31:24], RWE*[1] controls D[23:16], RWE*[2] controls D[15:8] and RWE*[3] controls D[7:0], and they are set according to the transaction width (word/half-word/byte) and the bus width set for the respective area.
BRDY* Bus ready (input)	[MEM] When driven low, this input indicates to the processor that the current memory access can be terminated on the next rising clock edge. When driven high, this input indicates to the processor that it must wait and not end the current access.

See notes at the end of the table.

TABLE III. Pin descriptions. – Continued

Pin	Function 1/
ROMS*[1:0] PROM chip-select (output)	[PROM] These active low outputs provide the chip-select signals for decoding the PROM area. ROMS*[0] is asserted when the lower half of the PROM area is accessed (0x00000000 - 0x0FFFFFFF), while ROMS* [1] is asserted when the upper half is accessed (0x10000000 - 0x1FFFFFFF).
RAMS*[4:0] SRAM chip-select (output)	[SRAM] These active low outputs provide the chip-select signals for decoding five SRAM banks.
RAMOE*[4:0] SRAM output enable (output)	[SRAM] These active low signals provide an output enable signal for each SRAM bank.
IOS* I/O select (output)	[IO] This active low output provides the chip-select signal for decoding the memory mapped I/O area.
SDCLK SDRAM clock (output)	[SDRAM] This signal provides a reference clock for SDRAM memories. It is a copy of the processor internal clock.
SDCS*[1:0] SDRAM chip select (output)	[SDRAM] These active low outputs provide the chip select signals for decoding two SDRAM banks.
SDRAS* SDRAM row address strobe (output)	[SDRAM] This active low output provides the RAS signal (Row Access Strobe) for SDRAM devices.
SDCAS* SDRAM column address strobe (output)	[SDRAM] This active low output provides the CAS signal (Column Access Strobe) for SDRAM devices.
SDWE* SDRAM write strobe (output)	[SDRAM] This active low output provides the write strobe for SDRAM devices.
SDDQM[3:0] SDRAM data mask (output)	[SDRAM] These active high outputs provide the DQM strobe (Data Mask) for SDRAM devices.
GPIO[15:0] General Purpose Input Output (bi-directional)	[GPIO] These bi-directional signals can be used as general-purpose inputs or outputs to control external devices. Some of these signals have an alternate function and also serve as inputs or outputs for internal peripherals. Half of them are used as an internal mean of communication.
IOx Reconfigurable unit : General Purpose IO	[GPIO] The programmable IOs are dedicated to user's application. Each programmable IO can independently be configured as input, output or bidirectional IO.
ILVDSx / ILVDSNx LVDS Receiver Differential Pair (Input)	[LVDS] ILDVSx/ILVDSNx receiver is a pair of differential signals that comply with the LVDS standard where 'x' is the LVDS channel: A1, A2, B1 or B2.
OLVDSx / OLVDSNx LVDS Driver Differential Pair (Output)	[LVDS] OLDVSx/OLVDSNx transmitter is a pair of differential signals that comply with the LVDS standard where 'x' is the LVDS channel: A1, A2, B1 or B2.
VREF LVDS reference voltage	[LVDS] VREF is the reference voltage for LVDS transmission operations. Each LVDS cluster has dedicated VREF source. It shall be accurately power supplied to 1.25V to comply with the LVDS standard.
DSUEN DSU enable (input)	[DSU] When asserted, this synchronous active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode. This signal is meant for debug purpose and shall be driven low in the final application.
DSURX DSU receiver (input)	[DSU] This input provides the serial data stream to the DSU communication link receiver.This signal is meant for debug purpose and shall be driven low in the final application.
DSUTX DSU transmitter (output)	[DSU] This output provides the serial data stream from the DSU communication link transmitter.

See notes at the end of the table.

TABLE III. Pin descriptions. – Continued

Pin	Function 1/
DSUACT DSU active (output)	[DSU] This active high output is asserted when the processor is in debug mode and controlled by the DSU.
DSUBRE DSU break enable (input)	[DSU] A low-to-high transition on this synchronous input signals a break condition and is used to set the processor into debug mode (see "Debug Support Unit" later in this document for specific use). This signal is meant for debug purpose and shall be driven low in the final application.
PROC_VCC33 Processor I/O power (supply)	[PWR] Power supply for the I/O pins of the processor.
FPGA_VCC33 Reconfiguarble unit I/O power (supply)	[PWR] Power supply for the I/O pins of the reconfigurable unit.
PROC_VDD18 Processor Core power (supply)	[PWR] Power supply for the core of processor.
FPGA_VDD18 Reconfigurable unit Core power (supply)	[PWR] Power supply for the core of reconfigurable unit.
VSS I/O ground (supply)	Ground supply.
PROC_VDD_PLL processor PLL power supply	[PWR] Power supply for the PLL.
PROC_VSS_PLL processor PLL ground supply	Ground supply for the PLL.

1/ In the above section, a complete description of the functions available for each pin is given. The family to which each function belongs to is precised. The various functions families available for the device are presented here after:

- [SI] : System interface functions,
- [CFG] : Configuration management functions,
- [GPIO]: General Purpose Input/Output functions,
- [CLOCK]: Clock management functions,
- [PLL]: PLL functions,
- [MEM]: Memory interface functions,
- [PROM]: PROM management functions,
- [SRAM]: SRAM management functions,
- [SDRAM] : SDRAM management functions,
- [IO]: IO functions,
- [LVDS]: LVDS I/O functions,
- [DSU]: Debugger System Unit functions,
- [PWR]: Power Supply functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-02-09

Approved sources of supply for SMD 5962-14229 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1422901QXC	F7400	ATF697FF-ZA-MQ
5962-1422901VXC	F7400	ATF697FF-ZA-SV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes, La Chantrerie BP 70602 44306 Nantes Cedex 3 France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.