# MCP1725

## 500 mA, Low Voltage, Low Quiescent Current LDO Regulator

### Features

- 500 mA Output Current Capability
- Input Operating Voltage Range: 2.3V to 6.0V
- Adjustable Output Voltage Range: 0.8V to 5.0V
- Standard Fixed Output Voltages:
  - 0.8V, 1.2V, 1.8V, 2.5V, 3.0V, 3.3V, 5.0V
- Other Fixed Output Voltage Options Available Upon Request
- Low Dropout Voltage: 210 mV typical at 500 mA
- Typical Output Voltage Tolerance: 0.5%
- Stable with 1.0 µF Ceramic Output Capacitor
- Fast response to Load Transients
- Low Supply Current: 120 µA (typical)
- Low Shutdown Supply Current: 0.1 µA (typical)
- Adjustable Delay on Power Good Output
- Short Circuit Current Limiting and Overtemperature Protection
- 2x3 DFN-8 and SOIC-8 Package Options

### Applications

- High-Speed Driver Chipset Power
- Networking Backplane Cards
- Notebook Computers
- Network Interface Cards
- Palmtop Computers
- Video Graphics Adapters
- 2.5V to 1.XV Regulators

### Description

The MCP1725 is a 500 mA Low Dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. The MCP1725 comes in a fixed (or adjustable) output voltage version, with an output voltage range of 0.8V to 5.0V. The 500 mA output current capability, combined with the low output voltage capability, make the MCP1725 a good choice for new sub-1.8V output voltage LDO applications that have high current demands.

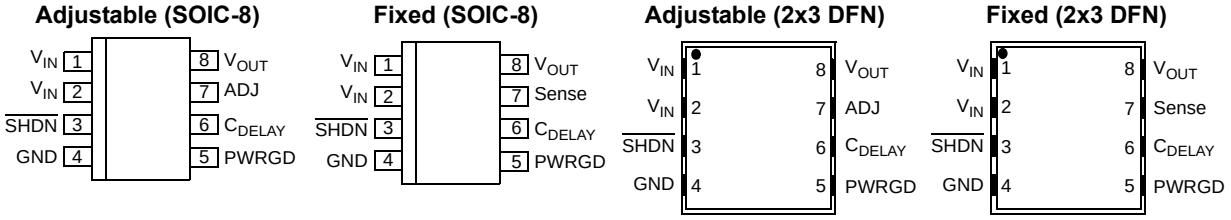
The MCP1725 is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 µF of output capacitance is needed to stabilize the LDO.

Using CMOS construction, the quiescent current consumed by the MCP1725 is typically less than 120 µA over the entire input voltage range, making it attractive for portable computing applications that demand high output current. When shut down, the quiescent current is reduced to less than 0.1 µA.

The scaled-down output voltage is internally monitored and a power good (PWRGD) output is provided when the output is within 92% of regulation (typical). An external capacitor can be used on the $C_{DELAY}$ pin to adjust the delay from 200 µs to 300 ms.

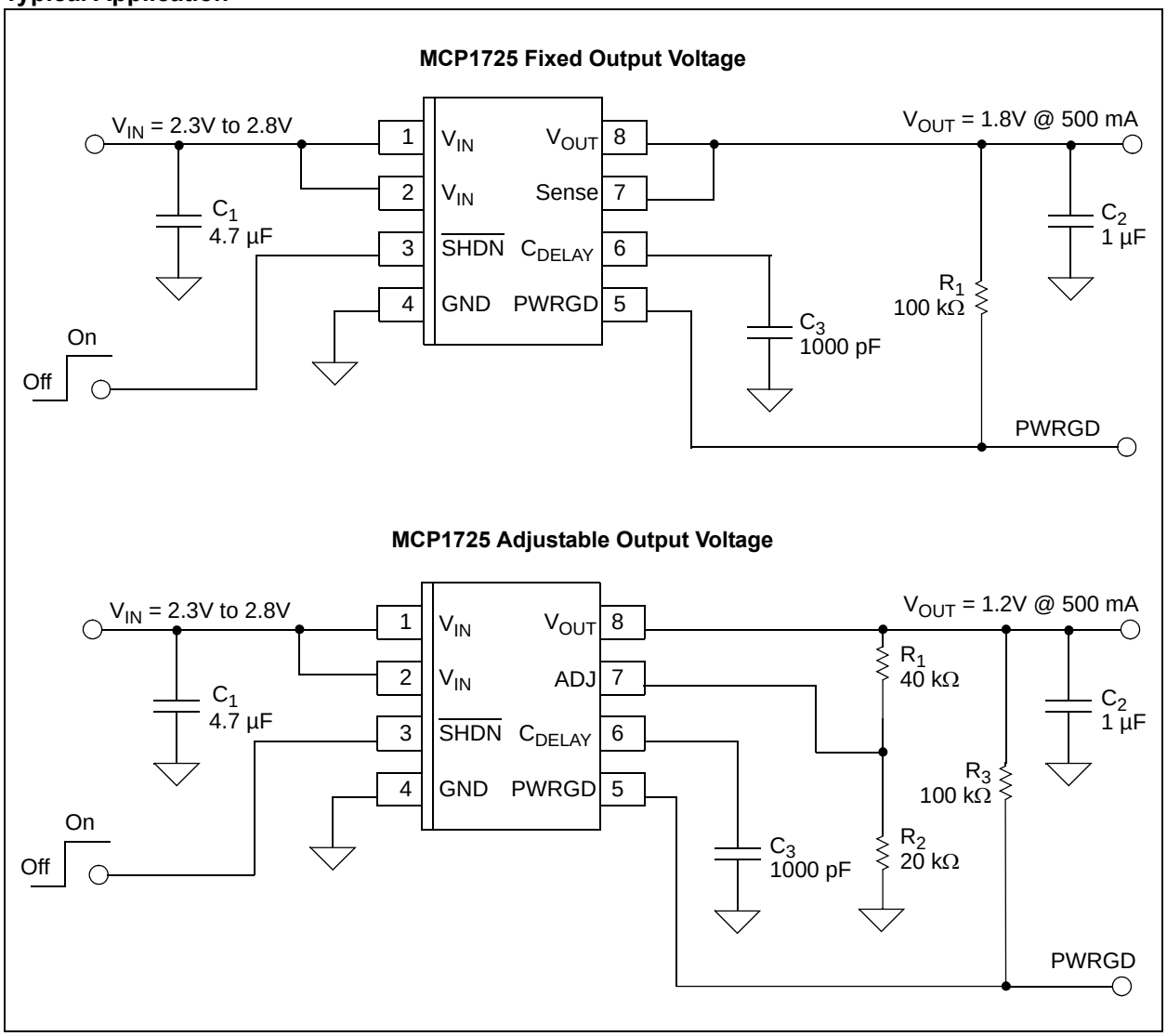
The overtemperature and short circuit current-limiting provide additional protection for the LDO during system fault conditions.

### Package Types

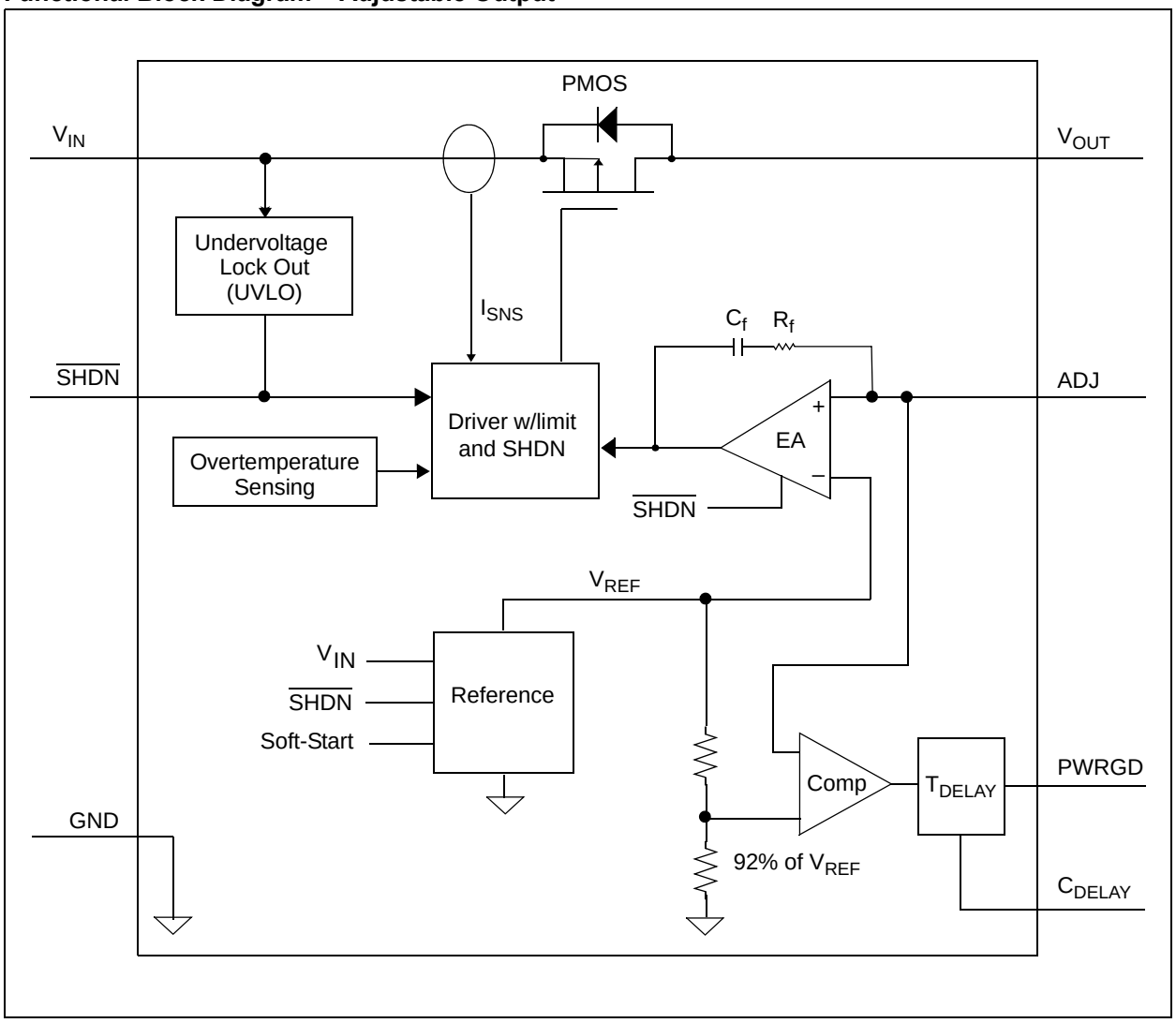



**Note:** DFN tab is at ground potential.

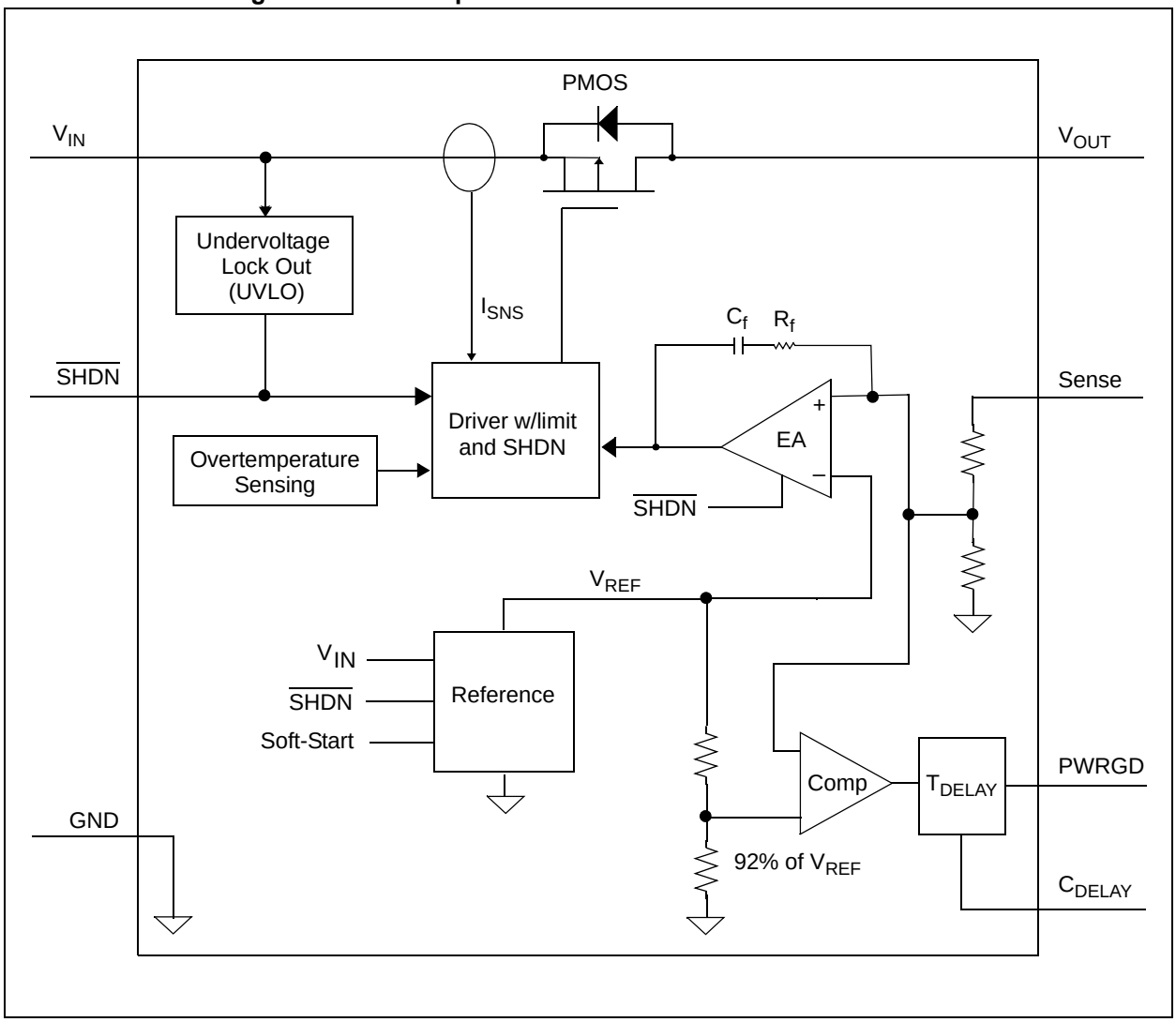
## Typical Application



**Functional Block Diagram - Adjustable Output**



**Functional Block Diagram - Fixed Output**



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{IN}$ ..... 6.5V
Maximum Voltage on Any Pin
.....(GND – 0.3V) to ($V_{IN}$ + 0.3)V
Maximum Power Dissipation..... Internally-Limited
(**Note 6**)
Output Short Circuit Duration..... Continuous
Storage temperature ..... -65°C to +150°C
Maximum Junction Temperature, $T_J$ ..... +150°C
ESD protection on all pins (HBM/MM).. ≥ 2 kV; ≥ 200V

**† Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## AC/DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ **(Note 1)**, $V_R$ = 1.8V for Adjustable Output, $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), $T_A$ = +25°C.
**Boldface** type applies for junction temperatures, $T_J$ (**Note 7**) of **-40°C to +125°C**

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Operating Voltage | $V_{IN}$ | **2.3** | | **6.0** | V | **Note 1** |
| Input Quiescent Current | $I_q$ | — | 120 | **220** | µA | $I_L$ = 0 mA, $V_{IN}$ = **Note 1**, $V_{OUT}$ = 0.8V to 5.0V |
| Input Quiescent Current for $\overline{SHDN}$ Mode | $I_{\overline{SHDN}}$ | — | 0.1 | **3** | µA | $\overline{SHDN}$ = GND |
| Maximum Output Current | $I_{OUT}$ | **500** | — | — | mA | $V_{IN}$ = 2.3V to 6.0V<br>$V_R$ = 0.8V to 5.0V, **Note 1** |
| Line Regulation | $\Delta V_{OUT}$/ ($V_{OUT}$ x $\Delta V_{IN}$) | — | ±0.05 | **±0.16** | %/V | **(Note 1)** ≤ $V_{IN}$ ≤ 6V |
| Load Regulation | $\Delta V_{OUT}/V_{OUT}$ | **-1.0** | ±0.5 | **1.0** | % | $I_{OUT}$ = 1 mA to 500 mA, (**Note 4**) |
| Output Short Circuit Current | $I_{OUT\_SC}$ | — | 1.2 | — | A | $R_{LOAD}$ < 0.1Ω, Peak Current |
| **Adjust Pin Characteristics (Adjustable Output Only)** | | | | | | |
| Adjust Pin Reference Voltage | $V_{ADJ}$ | **0.402** | 0.410 | **0.418** | V | $V_{IN}$ = 2.3V to $V_{IN}$ = 6.0V, $I_{OUT}$ = 1 mA |
| Adjust Pin Leakage Current | $I_{ADJ}$ | -10 | ±0.01 | +10 | nA | $V_{IN}$ = 6.0V, $V_{ADJ}$ = 0V to 6V |
| Adjust Temperature Coefficient | $TCV_{OUT}$ | — | 40 | — | ppm/°C | **Note 3** |
| **Fixed-Output Characteristics (Fixed Output Only)** | | | | | | |
| Voltage Regulation | $V_{OUT}$ | **$V_R$ - 2.5%** | $V_R$ ±0.5% | **$V_R$ + 2.5%** | V | **Note 2** |

**Note 1:** The minimum $V_{IN}$ must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

**2:** $V_R$ is the nominal regulator output voltage for the fixed cases. $V_R$ = 1.2V, 1.8V, etc. $V_R$ is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

**3:** $TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

**5:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{OUT} = V_R + V_{DROPOUT(MAX)}$.

**6:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact device reliability.

**7:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

## AC/DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ **(Note 1)**, $V_R$ = 1.8V for Adjustable Output, $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), $T_A$ = +25°C.
**Boldface** type applies for junction temperatures, $T_J$ (**Note 7**) of **-40°C to +125°C**

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Dropout Characteristics** | | | | | | |
| Dropout Voltage | $V_{IN}$-$V_{OUT}$ | — | 210 | **350** | mV | $I_{OUT}$ = 500 mA, **(Note 5)** $V_{IN(MIN)}$ = 2.3V |
| **Power Good Characteristics** | | | | | | |
| PWRGD Input Voltage Operating Range | $V_{PWRGD\_VIN}$ | 1.0 | — | 6.0 | V | $T_A$ = +25°C |
| | | **1.2** | — | **6.0** | | $T_A$ = -40°C to +125°C |
| | | | | | | For $V_{IN}$ < 2.3V, $I_{SINK}$ = 100 µA |
| PWRGD Threshold Voltage (Referenced to $V_{OUT}$) | $V_{PWRGD\_TH}$ | — | — | — | $\%V_{OUT}$ | Falling Edge |
| | | **89** | 92 | **95** | | $V_{OUT}$ < 2.5V Fixed, $V_{OUT}$ = Adj. |
| | | **90** | 92 | **94** | | $V_{OUT}$ >= 2.5V Fixed |
| PWRGD Threshold Hysteresis | $V_{PWRGD\_HYS}$ | **1.0** | 2.0 | **3.0** | $\%V_{OUT}$ | |
| PWRGD Output Voltage Low | $V_{PWRGD\_L}$ | — | 0.2 | **0.4** | V | $I_{PWRGD\ SINK}$ = 1.2 mA, ADJ = 0V, SENSE = 0V |
| PWRGD Leakage | $P_{WRGD\_LK}$ | — | 1 | — | nA | $V_{PWRGD} = V_{IN}$ = 6.0V |
| PWRGD Time Delay | $T_{PG}$ | | | | | Rising Edge<br>$R_{PULLUP}$ = 10 kΩ<br>$I_{CDELAY}$ = 140 nA (Typ) |
| | | — | 200 | — | µs | $C_{DELAY}$ = OPEN |
| | | **10** | 30 | **55** | ms | $C_{DELAY}$ = 0.01 µF |
| | | — | 300 | — | ms | $C_{DELAY}$ = 0.1 µF |
| Detect Threshold to PWRGD Active Time Delay | $T_{VDET-PWRGD}$ | — | 200 | — | µs | $V_{ADJ}$ or $V_{SENSE}$ = $V_{PWRGD\_TH}$ + 20 mV to $V_{PWRGD\_TH}$ - 20 mV |
| **Shutdown Input** | | | | | | |
| Logic High Input | $V_{SHDN-HIGH}$ | **45** | — | — | $\%V_{IN}$ | $V_{IN}$ = 2.3V to 6.0V |
| Logic Low Input | $V_{SHDN-LOW}$ | — | — | **15** | $\%V_{IN}$ | $V_{IN}$ = 2.3V to 6.0V |
| $\overline{SHDN}$ Input Leakage Current | $\overline{SHDN}_{ILK}$ | **-0.1** | ±0.001 | **+0.1** | µA | $V_{IN}$ = 6V, $\overline{SHDN}$ =$V_{IN}$, $\overline{SHDN}$ = GND |

**Note 1:** The minimum $V_{IN}$ must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

**2:** $V_R$ is the nominal regulator output voltage for the fixed cases. $V_R$ = 1.2V, 1.8V, etc. $V_R$ is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

**3:** $TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

**5:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{OUT} = V_R + V_{DROPOUT(MAX)}$.

**6:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact device reliability.

**7:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

## AC/DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ **(Note 1)**, $V_R$ = 1.8V for Adjustable Output, $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), $T_A$ = +25°C.
**Boldface** type applies for junction temperatures, $T_J$ (**Note 7**) of **-40°C to +125°C**

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **AC Performance** | | | | | | |
| Output Delay From $\overline{SHDN}$ | $T_{OR}$ | — | 100 | — | µs | $\overline{SHDN}$ = GND to $V_{IN}$<br>$V_{OUT}$ = GND to 95% $V_R$ |
| Output Noise | $e_N$ | — | 2.0 | — | µV/√Hz | $I_{OUT}$ = 200 mA, f = 1 kHz,<br>$C_{OUT}$ = 10 µF (X7R Ceramic),<br>$V_{OUT}$ = 2.5V |
| Power Supply Ripple Rejection Ratio | PSRR | — | 60 | — | dB | f = 100 Hz, $C_{OUT}$ = 10 µF,<br>$I_{OUT}$ = 10 mA,<br>$V_{INAC}$ = 30 mV pk-pk,<br>$C_{IN}$ = 0 µF |
| Thermal Shutdown Temperature | $T_{SD}$ | — | 150 | — | °C | $I_{OUT}$ = 100 µA, $V_{OUT}$ = 1.8V,<br>$V_{IN}$ = 2.8V |
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | — | 10 | — | °C | $I_{OUT}$ = 100 µA, $V_{OUT}$ = 1.8V,<br>$V_{IN}$ = 2.8V |

**Note 1:** The minimum $V_{IN}$ must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

**2:** $V_R$ is the nominal regulator output voltage for the fixed cases. $V_R$ = 1.2V, 1.8V, etc. $V_R$ is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

**3:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

**5:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{OUT} = V_R + V_{DROPOUT(MAX)}$.

**6:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact device reliability.

**7:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

## TEMPERATURE SPECIFICATIONS

**Electrical Specifications:** Unless otherwise indicated, all limits apply for $V_{IN}$ = 2.3V to 6.0V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Junction Temperature Range | $T_J$ | -40 | — | +125 | °C | Steady State |
| Maximum Junction Temperature | $T_J$ | — | — | +150 | °C | Transient |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 8LD 2x3 DFN | $\theta_{JA}$ | — | 76 | — | °C/W | 4-Layer JC51-7 Standard Board with vias |
| | $\theta_{JC}$ | — | 26 | — | °C/W | |
| Thermal Resistance, 8LD SOIC | $\theta_{JA}$ | — | 163 | — | °C/W | 4-Layer JC51-7 Standard Board |
| | $\theta_{JC}$ | — | 38.8 | — | °C/W | |

## 2.0 TYPICAL PERFORMANCE CURVES

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$ or $V_{IN} = 2.3V$ (whichever is greater), $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ µF Ceramic (X7R), $\overline{SHDN} = V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A = +25°C$.

**Note:** Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction Temperature over the Ambient temperature is not significant.

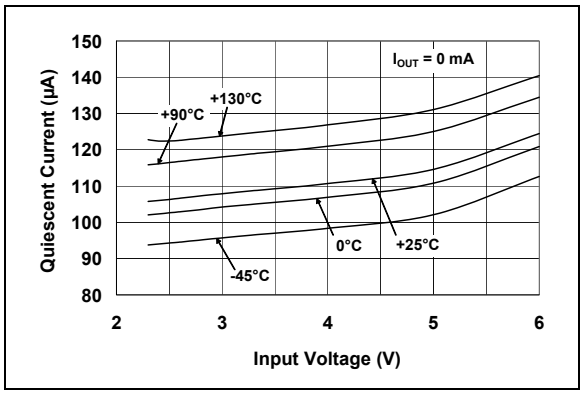



***FIGURE 2-1:*** *Quiescent Current vs. Input Voltage (1.8V Adjustable).*

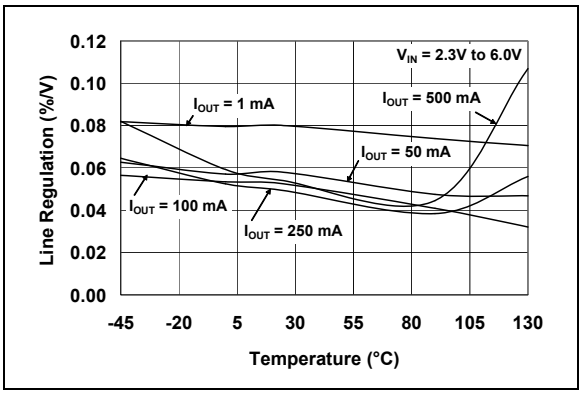



***FIGURE 2-4:*** *Line Regulation vs. Temperature (1.8V Adjustable).*

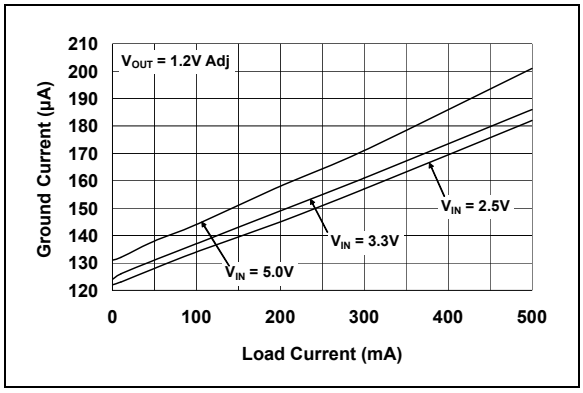



***FIGURE 2-2:*** *Ground Current vs. Load Current (1.2V Adjustable).*

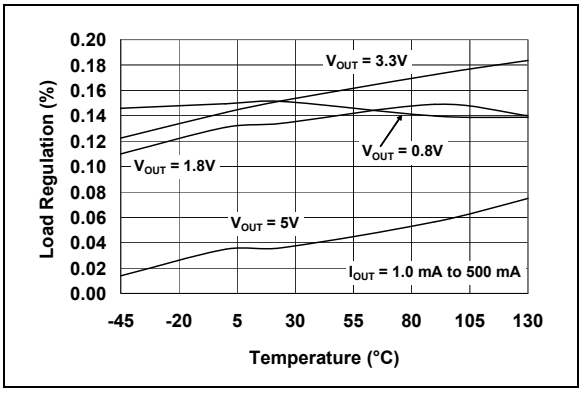



***FIGURE 2-5:*** *Load Regulation vs. Temperature (Adjustable Version).*

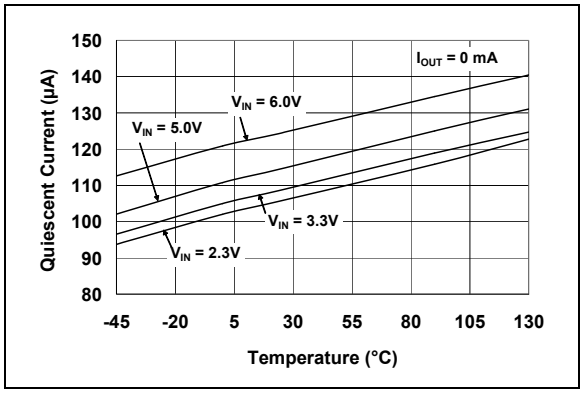



***FIGURE 2-3:*** *Quiescent Current vs. Junction Temperature (1.8V Adjustable).*

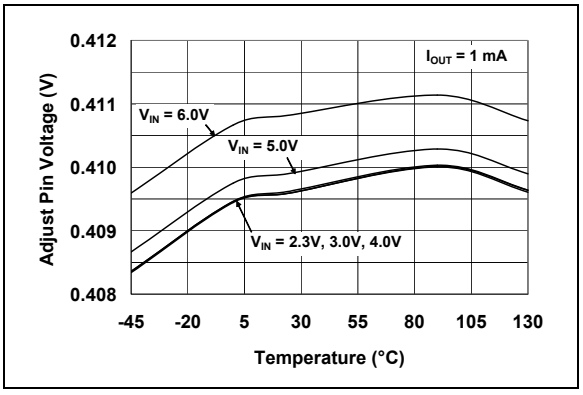



***FIGURE 2-6:*** *Adjust Pin Voltage vs. Temperature.*

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$ or $V_{IN} = 2.3V$ (whichever is greater), $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ µF Ceramic (X7R), SHDN = $V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A = +25°C$.

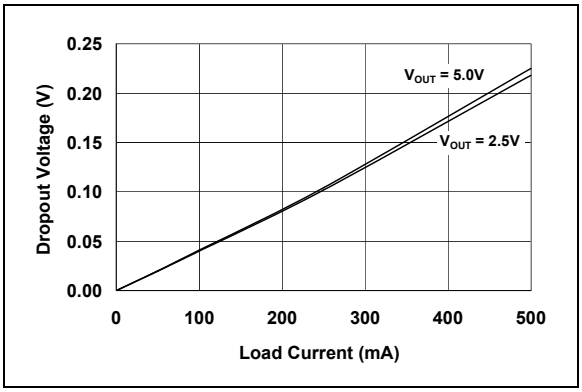



***FIGURE 2-7:*** *Dropout Voltage vs. Load Current (Adjustable Version).*

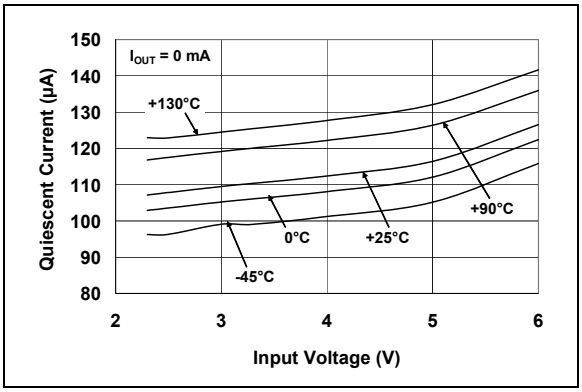



***FIGURE 2-10:*** *Quiescent Current vs. Input Voltage (0.8V Fixed).*

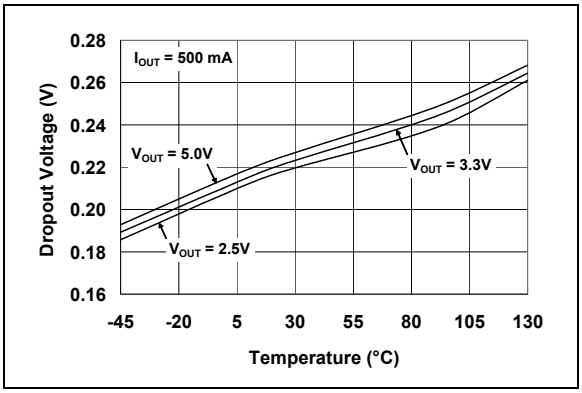



***FIGURE 2-8:*** *Dropout Voltage vs. Temperature (Adjustable Version).*

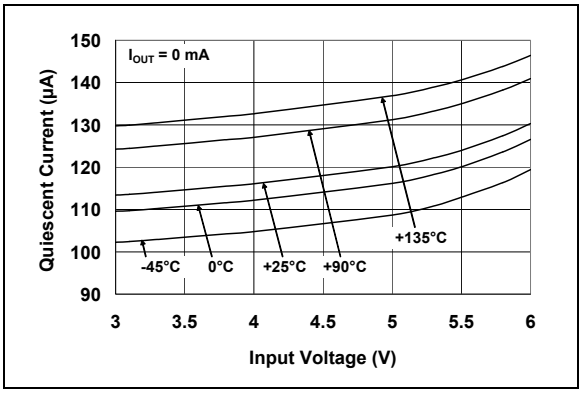



***FIGURE 2-11:*** *Quiescent Current vs. Input Voltage (2.5V Fixed).*

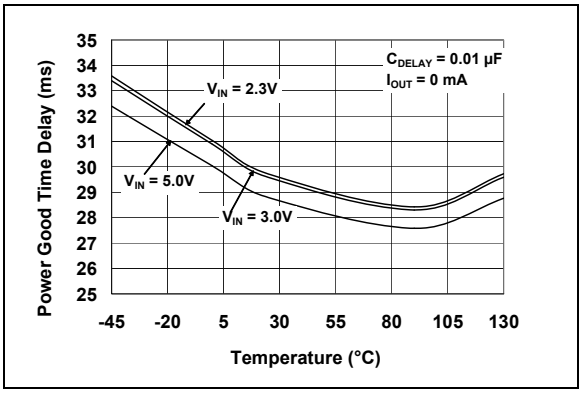



***FIGURE 2-9:*** *Power Good (PWRGD) Time Delay vs. Temperature (Adjustable Version).*

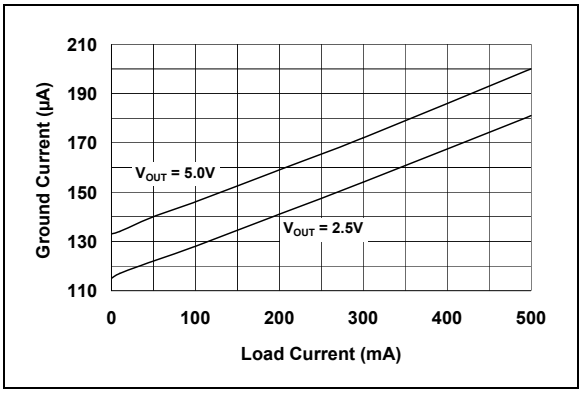



***FIGURE 2-12:*** *Ground Current vs. Load Current.*

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$ or $V_{IN} = 2.3V$ (whichever is greater), $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ µF Ceramic (X7R), $\overline{SHDN} = V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A = +25°C$.

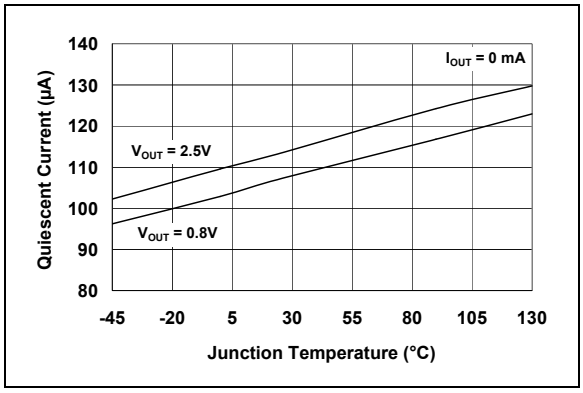



***FIGURE 2-13:*** *Quiescent Current vs. Junction Temperature.*

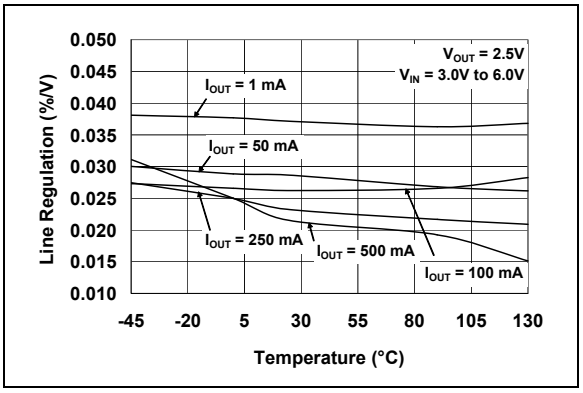



***FIGURE 2-16:*** *Line Regulation vs. Temperature (2.5V Fixed).*

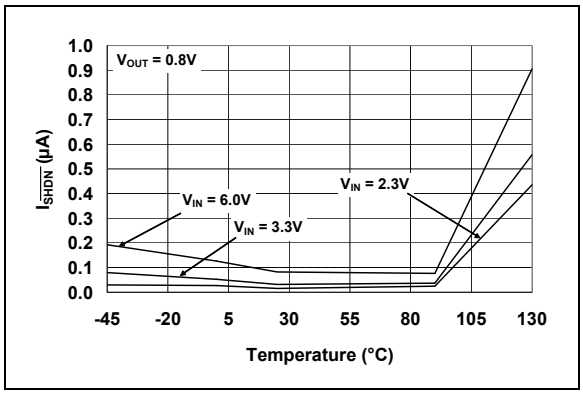



***FIGURE 2-14:*** *$I_{\overline{SHDN}}$ vs. Temperature.*

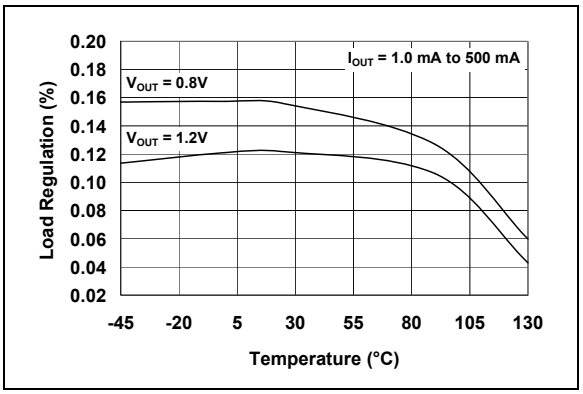



***FIGURE 2-17:*** *Load Regulation vs. Temperature ($V_{OUT} < 2.5V$ Fixed).*

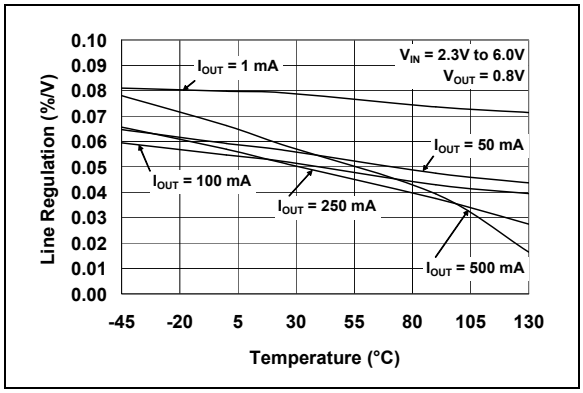



***FIGURE 2-15:*** *Line Regulation vs. Temperature (0.8V Fixed).*

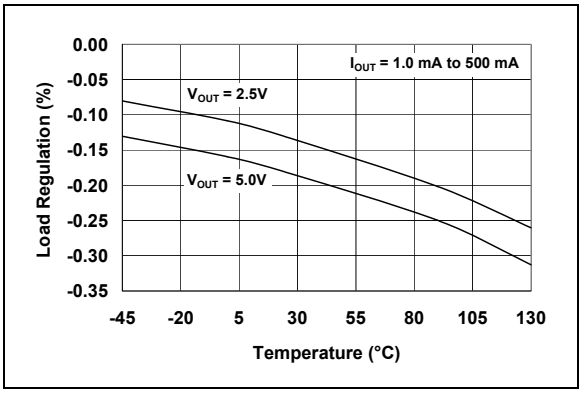



***FIGURE 2-18:*** *Load Regulation vs. Temperature ($V_{OUT} \geq 2.5V$ Fixed).*

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$ or $V_{IN} = 2.3V$ (whichever is greater), $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ µF Ceramic (X7R), SHDN = $V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A = +25°C$.

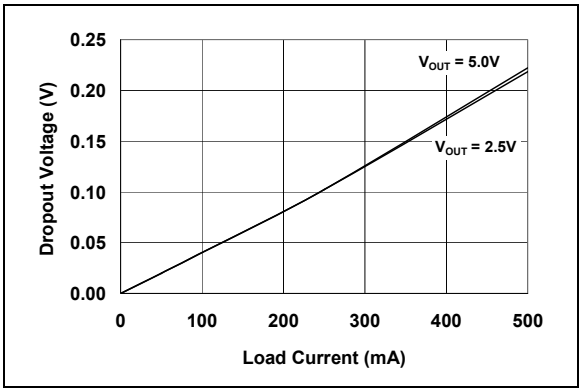



***FIGURE 2-19:*** *Dropout Voltage vs. Load Current.*

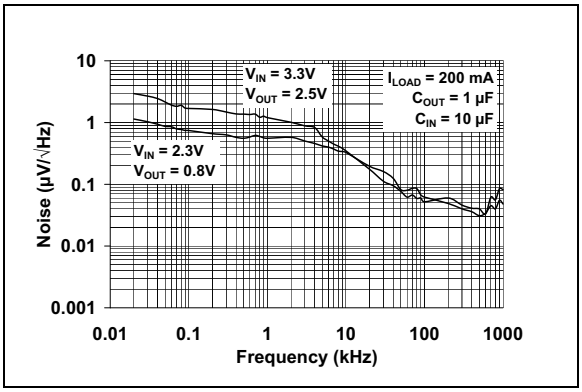



***FIGURE 2-22:*** *Output Noise Voltage Density vs. Frequency.*

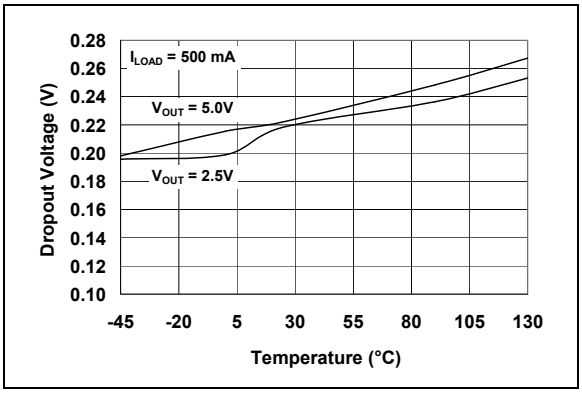



***FIGURE 2-20:*** *Dropout Voltage vs. Temperature.*

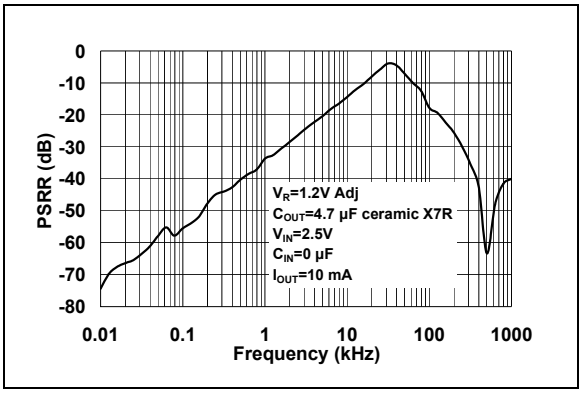



***FIGURE 2-23:*** *Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT}$ = 1.2V Adj.).*

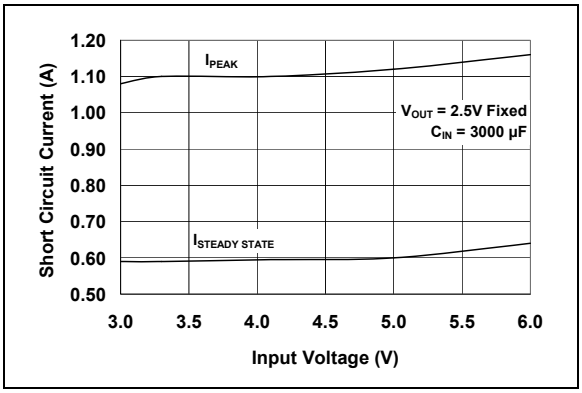



***FIGURE 2-21:*** *Short Circuit Current vs. Input Voltage.*

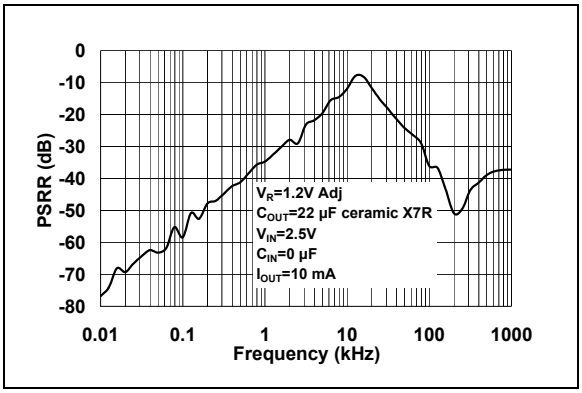



***FIGURE 2-24:*** *Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT}$ = 1.2V Adj.).*

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT}$ + 0.5V or $V_{IN}$ = 2.3V (whichever is greater), $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF Ceramic (X7R), SHDN = $V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A$ = +25°C.

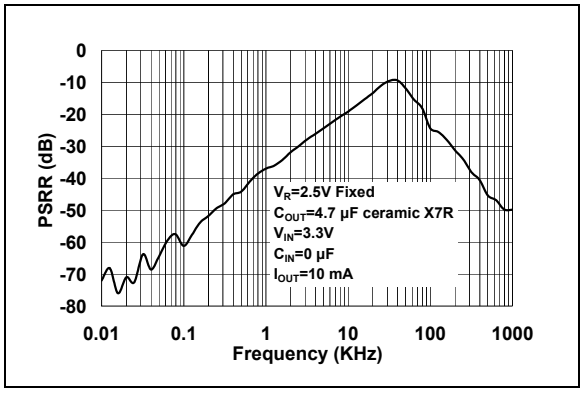



***FIGURE 2-25:*** *Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT}$ = 2.5V Fixed).*

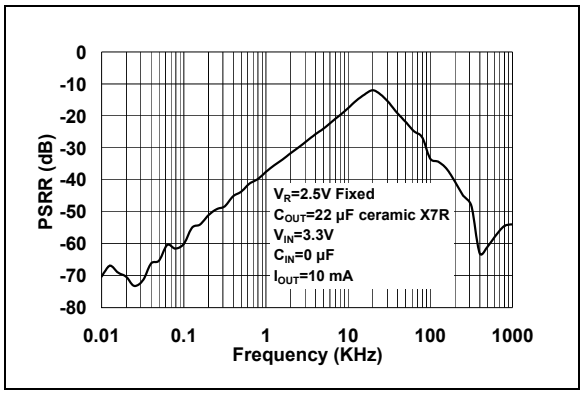



***FIGURE 2-26:*** *Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT}$ = 2.5V Fixed).*

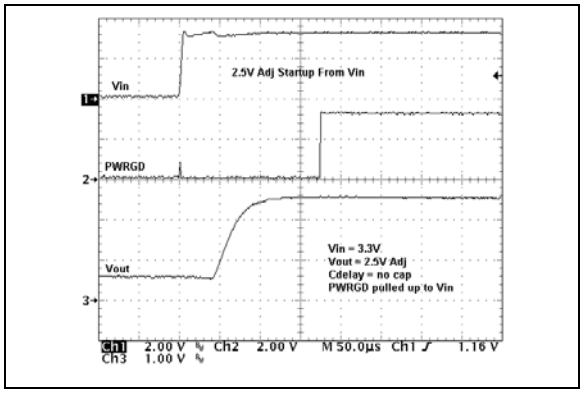



***FIGURE 2-27:*** *2.5V (Adj.) Startup from $V_{IN}$.*

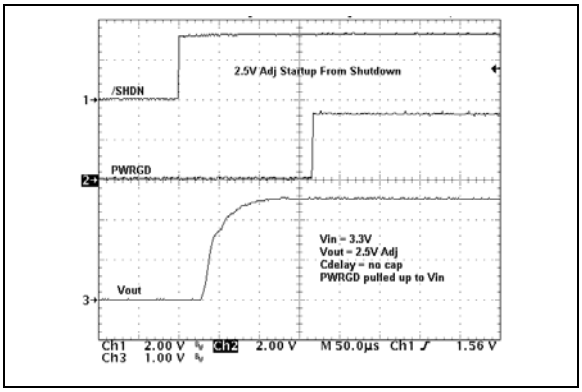



***FIGURE 2-28:*** *2.5V (Adj.) Startup from Shutdown.*

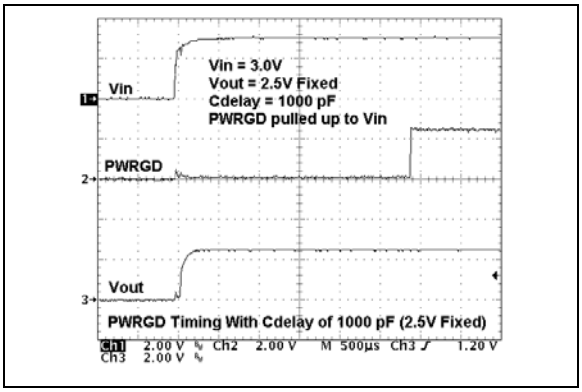



***FIGURE 2-29:*** *Power Good (PWRGD) Timing with Cdelay of 1000 pF (2.5V Fixed).*

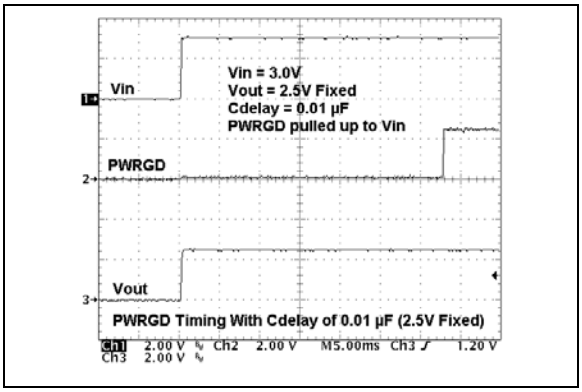



***FIGURE 2-30:*** *Power Good (PWRGD) Timing with $C_{DELAY}$ of 0.01 µF (2.5V Fixed).*

**Note:** Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$ or $V_{IN} = 2.3V$ (whichever is greater), $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ µF Ceramic (X7R), SHDN = $V_{IN}$, $C_{DELAY}$ = Open, Fixed Output Version, and $T_A = +25°C$.

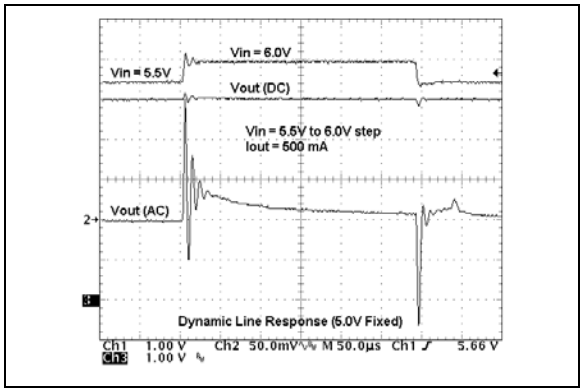



***FIGURE 2-31:*** *Dynamic Line Response (5.0V Fixed).*

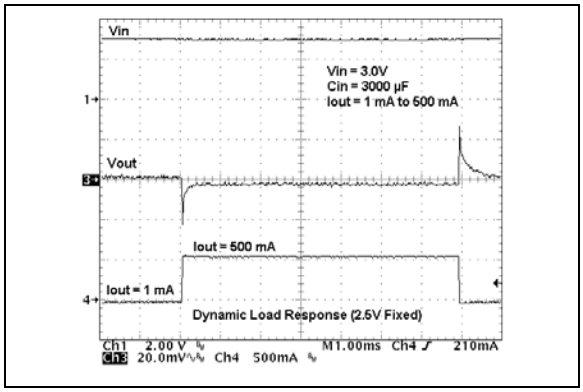



***FIGURE 2-33:*** *Dynamic Load Response (2.5V Fixed, 1 mA to 500 mA).*

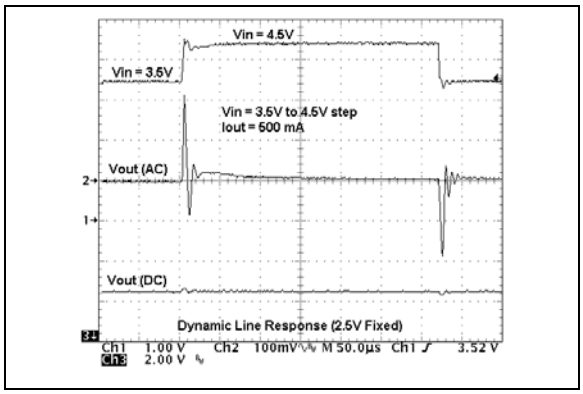



***FIGURE 2-32:*** *Dynamic Line Response (2.5V Fixed).*

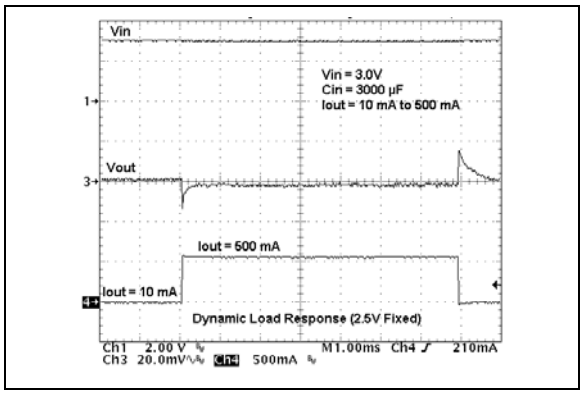



***FIGURE 2-34:*** *Dynamic Load Response (2.5V Fixed, 10 mA to 500 mA).*

## 3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Fixed Output | Adjustable Output | Name | Description |
|---|---|---|---|
| 1 | 1 | $V_{IN}$ | Input Voltage Supply |
| 2 | 2 | $V_{IN}$ | Input Voltage Supply |
| 3 | 3 | $\overline{SHDN}$ | Shutdown Control Input (active-low) |
| 4 | 4 | GND | Ground |
| 5 | 5 | PWRGD | Power Good Output (open-drain) |
| 6 | 6 | $C_{DELAY}$ | Power Good Delay Set-Point Input |
| — | 7 | ADJ | Voltage Sense Input (adjustable version) |
| 7 | — | Sense | Voltage Sense Input (fixed voltage version) |
| 8 | 8 | $V_{OUT}$ | Regulated Output Voltage |
| Exposed Pad | Exposed Pad | EP | Exposed Pad of the DFN Package (ground potential) |

### 3.1 Input Voltage Supply ($V_{IN}$)

Connect the unregulated or regulated input voltage source to $V_{IN}$. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications.

### 3.2 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.1 µA.

### 3.3 Ground (GND)

Connect the GND pin of the LDO to a quiet circuit ground. This will help the LDO power supply rejection ratio and noise performance. The ground pin of the LDO only conducts the quiescent current of the LDO (typically 120 µA), so a heavy trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

### 3.4 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The PWRGD output is typically delayed by 200 µs (typical, no capacitance on $C_{DELAY}$ pin) from the time the LDO output is within 92% + 3% (max hysteresis) of the regulated output value on power-up. This delay time is controlled by the $C_{DELAY}$ pin.

### 3.5 Power Good Delay Set-Point Input ($C_{DELAY}$)

The $C_{DELAY}$ input sets the power-up delay time for the PWRGD output. By connecting an external capacitor from the $C_{DELAY}$ pin to ground, the typical delay times for the PWRGD output can be adjusted from 200 µs (no capacitance) to 300 ms (0.1 µF capacitor). This allows for the optimal setting of the system reset time.

## 3.6 Output Voltage Sense/Adjust Input (ADJ/Sense)

### 3.6.1 ADJ

For adjustable applications, the output voltage is connected to the ADJ input through a resistor divider that sets the output voltage regulation value. This provides the user the capability to set the output voltage to any value they desire within the 0.8V to 5.0V range of the device.

### 3.6.2 Sense

For fixed output voltage versions of the device, the SENSE input is used to provide output voltage feedback to the internal circuitry of the MCP1725. The SENSE pin typically improves load regulation by allowing the device to compensate for voltage drops due to packaging and circuit board layout.

## 3.7 Regulated Output Voltage ($V_{OUT}$)

The $V_{OUT}$ pin(s) is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 µF is required for LDO stability. The MCP1725 is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See **Section 4.3 "Output Capacitor"** for output capacitor selection guidance.

## 3.8 Exposed Pad (EP)

The 2x3 DFN package has an exposed pad on the bottom of the package. This pad should be soldered to the Printed Circuit Board (PCB) to aid in the removal of heat from the package during operation. The exposed pad is at the ground potential of the LDO.

## 4.0 DEVICE OVERVIEW

The MCP1725 is a high output current, Low Dropout (LDO) voltage regulator with an adjustable delay power-good output and shutdown control input. The low dropout voltage of 210 mV typical at 0.5A of current makes it ideal for battery-powered applications. Unlike other high output current LDOs, the MCP1725 only draws a maximum of 220 µA of quiescent current.

## 4.1 LDO Output Voltage

The MCP1725 LDO is available with either a fixed output voltage or an adjustable output voltage. The output voltage range is 0.8V to 5.0V for both versions.

### 4.1.1 ADJUST INPUT

The adjustable version of the MCP1725 uses the ADJ pin (pin 7) to get the output voltage feedback for output voltage regulation. This allows the user to set the output voltage of the device with two external resistors. The nominal voltage for ADJ is 0.41V.

Figure 4-1 shows the adjustable version of the MCP1725. Resistors $R_1$ and $R_2$ form the resistor divider network necessary to set the output voltage. With this configuration, the equation for setting $V_{OUT}$ is:

**EQUATION 4-1:**

$$V_{OUT} = V_{ADJ}\left(\frac{R_1 + R_2}{R_2}\right)$$

Where:

| | | |
|---|---|---|
| $V_{OUT}$ | = | LDO Output Voltage |
| $V_{ADJ}$ | = | ADJ Pin Voltage (typically 0.41V) |

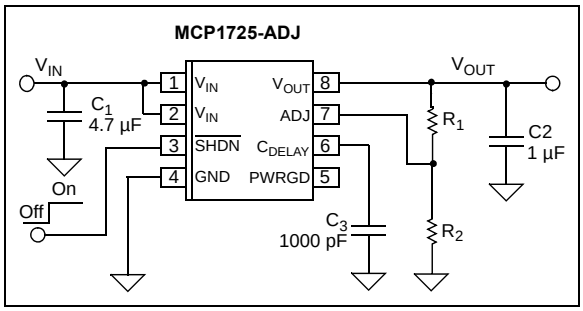



***FIGURE 4-1:*** *Typical Adjustable Output Voltage Application Circuit.*

The allowable resistance value range for resistor $R_2$ is from 10 kΩ to 200 kΩ. Solving the equation for $R_1$ yields the following equation:

**EQUATION 4-2:**

$$R_1 = R_2\left(\frac{V_{OUT} - V_{ADJ}}{V_{ADJ}}\right)$$

Where:

| | | |
|---|---|---|
| $V_{OUT}$ | = | LDO Output Voltage |
| $V_{ADJ}$ | = | ADJ Pin Voltage (typically 0.41V) |

## 4.2 Output Current and Current Limiting

The MCP1725 LDO is tested and ensured to supply a minimum of 0.5A of output current. The MCP1725 has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1725 also incorporates an output current limit. If the output voltage falls below 0.7V due to an overload condition (usually represents a shorted load condition), the output current is limited to 1.2A (typical). If the overload condition is a soft overload, the MCP1725 will supply higher load currents of up to 1A. The MCP1725 should not be operated in this condition continuously as it may result in failure of the device. However, this does allow for device usage in applications that have higher pulsed load currents having an average output current value of 0.5A or less.

Output overload conditions may also result in an overtemperature shutdown of the device. If the junction temperature rises above 150°C, the LDO will shut down the output voltage. See **Section 4.9 "Overtemperature Protection"** for more information on overtemperature shutdown.

## 4.3 Output Capacitor

The MCP1725 requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor must be no greater than 1 ohm. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 milli-ohms.

Larger LDO output capacitors can be used with the MCP1725 to improve dynamic performance and power supply ripple rejection performance. A maximum of 22 µF is recommended. Aluminum-electrolytic capacitors are not recommended for low-temperature applications of < -25°C.

## 4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent (or higher) value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

## 4.5 Power Good Output (PWRGD)

The PWRGD output is used to indicate when the output voltage of the LDO is within 92% (typical value, see **Section 1.0 "Electrical Characteristics"** for Minimum and Maximum specifications) of its nominal regulation value.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as $T_{PG}$ in **Section 1.0 "Electrical Characteristics"**). The power good time delay is adjustable via the $C_{DELAY}$ pin of the LDO (see **Section 4.6 "$C_{DELAY}$ Input"**). By placing a capacitor from the $C_{DELAY}$ pin to ground, the power good time delay can be adjusted from 200 µs (no capacitance) to 300 ms (0.1 µF capacitor). After the time delay period, the PWRGD output will go high, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 170 µs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-2 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{SHDN}$ input, the power good output is pulled low immediately, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-3.

The power good output is an open-drain output that can be pulled up to any voltage that is equal to or less than the LDO input voltage. This output is capable of sinking 1.2 mA ($V_{PWRGD}$ < 0.4V maximum).

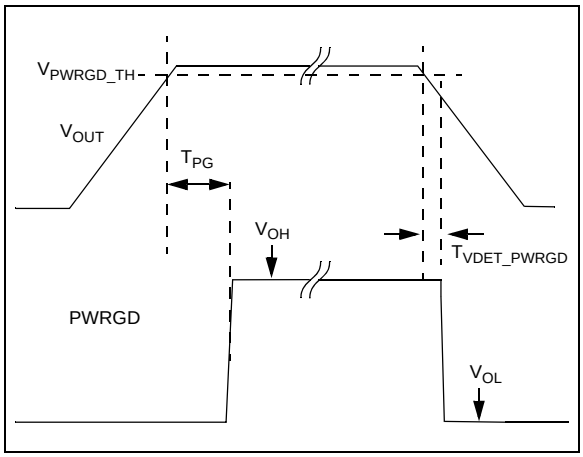



***FIGURE 4-2:*** *Power Good Timing.*

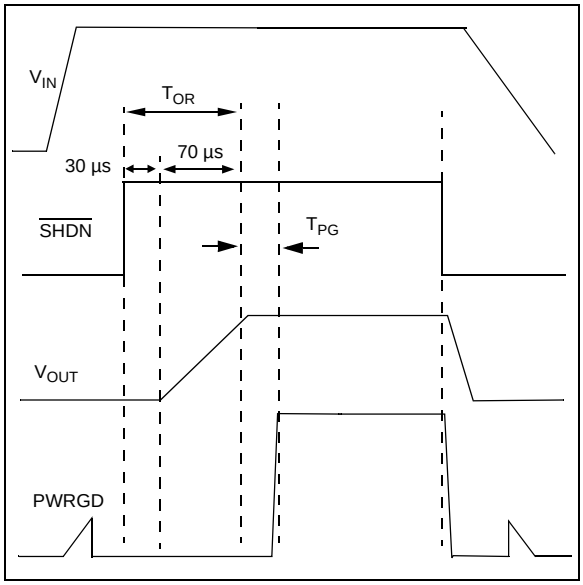



***FIGURE 4-3:*** *Power Good Timing from Shutdown.*

## 4.6 $C_{DELAY}$ Input

The $C_{DELAY}$ input is used to provide the power-up delay timing for the power good output, as discussed in the previous section. By adding a capacitor from the $C_{DELAY}$ pin to ground, the PWRGD power-up time delay can be adjusted from 200 µs (no capacitance on $C_{DELAY}$) to 300 ms (0.1 µF of capacitance on $C_{DELAY}$). See **Section 1.0 "Electrical Characteristics"** for $C_{DELAY}$ timing tolerances.

Once the power good threshold (rising) has been reached, the $C_{DELAY}$ pin charges the external capacitor to $V_{IN}$. The charging current is 140 nA (typical). The PWRGD output will transition high when the $C_{DELAY}$ pin voltage has charged to 0.42V. If the output falls below the power good threshold limit during the charging time between 0.0V and 0.42V on the $C_{DELAY}$ pin, the $C_{DELAY}$ pin voltage will be pulled to ground, thus resetting the timer. The $C_{DELAY}$ pin will be held low until the output voltage of the LDO has once again risen above the power good rising threshold. A timing diagram showing $C_{DELAY}$, PWRGD and $V_{OUT}$ is shown in Figure 4-4.

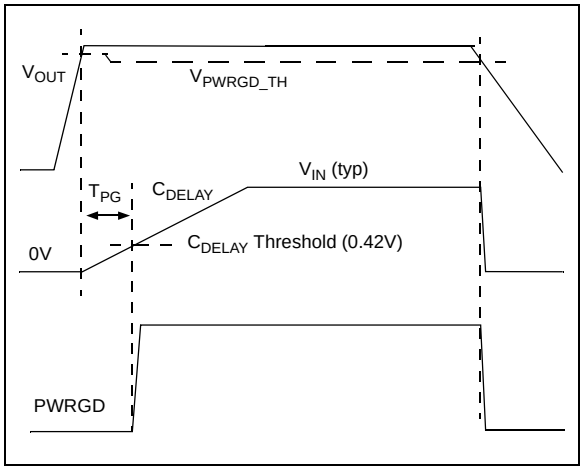



***FIGURE 4-4:*** *$C_{DELAY}$ and PWRGD Timing Diagram.*

## 4.7 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The typical value of this shutdown threshold is 30% of $V_{IN}$, with minimum and maximum limits over the entire operating temperature range of 45% and 15%, respectively.

The $\overline{SHDN}$ input will ignore low-going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO will enter Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the shutdown input signal.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 30 µs delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the 30 µs delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 30 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the LDO output being in regulation is typically 100 µs. See Figure 4-5 for a timing diagram of the $\overline{SHDN}$ input.

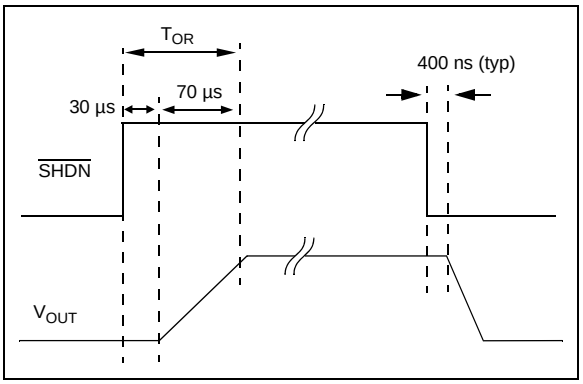



***FIGURE 4-5:*** *Shutdown Input Timing Diagram.*

## 4.8 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a $V_R$ + 0.6V differential applied. The MCP1725 LDO has a very low dropout voltage specification of 210 mV (typical) at 0.5A of output current. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

The MCP1725 LDO operates across an input voltage range of 2.3V to 6.0V and incorporates input Undervoltage Lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 2.18V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output will remain on until the input voltage level reaches 2.04V (typical).

Since the MCP1725 LDO undervoltage lockout activates at 2.04V as the input voltage is falling, the dropout voltage specification does not apply for output voltages that are less than 1.9V.

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 2.3V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

## 4.9 Overtemperature Protection

The MCP1725 LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately 150°C. If the LDO junction temperature does reach 150°C, the LDO output will be turned off until the junction temperature cools to approximately 140°C, at which point the LDO output will automatically resume normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See **Section 5.0 "Application Circuits/Issues"** for more information on LDO power dissipation and junction temperature.

## 5.0 APPLICATION CIRCUITS/ ISSUES

### 5.1 Typical Application

The MCP1725 is used for applications that require high LDO output current and a power good output.

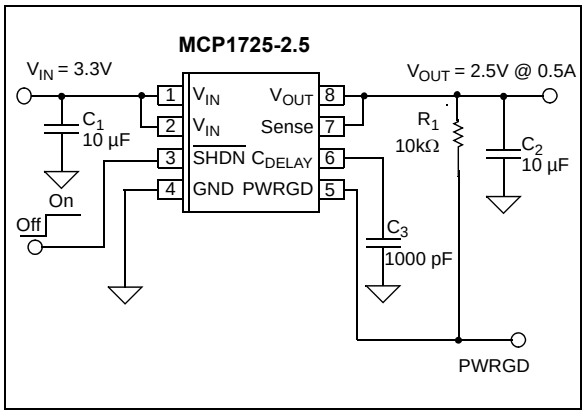



***FIGURE 5-1:*** *Typical Application Circuit.*

#### 5.1.1 APPLICATION CONDITIONS

| | | |
|---|---|---|
| Package Type | = | 2x3 DFN8 |
| Input Voltage Range | = | 3.3V ± 5% |
| $V_{IN}$ maximum | = | 3.465V |
| $V_{IN}$ minimum | = | 3.135V |
| $V_{DROPOUT\ (max)}$ | = | 0.350V |
| $V_{OUT}$ (typical) | = | 2.5V |
| $I_{OUT}$ | = | 0.5A maximum |
| $P_{DISS}$ (typical) | = | 0.4W |
| Temperature Rise | = | 30.4°C |

### 5.2 Power Calculations

#### 5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1725 is a function of input voltage, output voltage, output current, and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

**EQUATION 5-1:**

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

Where:

| | | |
|---|---|---|
| $P_{LDO}$ | = | LDO Pass device internal power dissipation |
| $V_{IN(MAX)}$ | = | Maximum input voltage |
| $V_{OUT(MIN)}$ | = | LDO minimum output voltage |

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1725 as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation:

**EQUATION 5-2:**

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

Where:

| | | |
|---|---|---|
| $P_{I(GND}$ | = | Power dissipation due to the quiescent current of the LDO |
| $V_{IN(MAX)}$ | = | Maximum input voltage |
| $I_{VIN}$ | = | Current flowing in the $V_{IN}$ pin with no LDO output current (LDO quiescent current) |

The total power dissipated within the MCP1725 is the sum of the power dissipated in the LDO pass device and the $P(I_{GND})$ term. Because of the CMOS construction, the typical $I_{GND}$ for the MCP1725 is 120 µA. Operating at 3.465V results in a power dissipation of 0.42 milli-Watts. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1725 is +125°C. To estimate the internal junction temperature of the MCP1725, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction to ambient for the 2x3 DFN package is estimated at 76° C/W.

**EQUATION 5-3:**

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

| | | |
|---|---|---|
| $T_{J(MAX)}$ | = | Maximum continuous junction temperature |
| $P_{TOTAL}$ | = | Total device power dissipation |
| $R\theta_{JA}$ | = | Thermal resistance from junction to ambient |
| $T_{AMAX}$ | = | Maximum ambient temperature |

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

**EQUATION 5-4:**

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = maximum continuous junction temperature
$T_{A(MAX)}$ = maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

**EQUATION 5-5:**

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$ = Maximum device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient

**EQUATION 5-6:**

$$T_J = T_{J(RISE)} + T_A$$

$T_J$ = Junction temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$T_A$ = Ambient temperature

## 5.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation is calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

**EXAMPLE 5-1: POWER DISSIPATION EXAMPLE**

**Package**

Package Type = 2x3 DFN

**Input Voltage**

$V_{IN}$ = 3.3V ± 5%

**LDO Output Voltage and Current**

$V_{OUT}$ = 2.5V

$I_{OUT}$ = 0.5A

**Maximum Ambient Temperature**

$T_{A(MAX)}$ = 60°C

**Internal Power Dissipation**

$P_{LDO(MAX)}$ = $(V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

$P_{LDO}$ = ((3.3V x 1.05) – (2.5V x 0.975)) x 0.5A

$P_{LDO}$ = 0.51 Watts

### 5.3.1 DEVICE JUNCTION TEMPERATURE RISE

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction-to-ambient for the application. The thermal resistance from junction-to-ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7 *"High Effective Thermal Conductivity Test Board for Leaded Surface-Mount Packages"*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

$T_{J(RISE)}$ = $P_{TOTAL}$ x $R\theta_{JA}$

$T_{JRISE}$ = 0.51 W x 76.0° C/W

$T_{JRISE}$ = 38.8°C

### 5.3.2 JUNCTION TEMPERATURE ESTIMATE

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

$T_J = T_{JRISE} + T_{A(MAX)}$
$T_J = 38.8°C + 60.0°C$
$T_J = 98.8°C$

As you can see from the result, this application will be operating near around a junction temperature of 100°C. The PCB layout for this application is very important as it has a significant impact on the junction-to-ambient thermal resistance ($R\theta_{JA}$) of the 2x3 DFN package, which is very important in this application.

### 5.3.3 MAXIMUM PACKAGE POWER DISSIPATION AT 60°C AMBIENT TEMPERATURE

**2x3 DFN (76°C/W $R\theta_{JA}$):**

$P_{D(MAX)} = (125°C – 60°C) / 76°C/W$
$P_{D(MAX)} = 0.855W$

**SOIC8 (163°C/Watt $R\theta_{JA}$):**

$P_{D(MAX)} = (125°C – 60°C)/ 163°C/W$
$P_{D(MAX)} = 0.399W$

From this table, you can see the difference in maximum allowable power dissipation between the 2x3 DFN package and the 8-pin SOIC package. This difference is due to the exposed metal tab on the bottom of the DFN package. The exposed tab of the DFN package provides a very good thermal path from the die of the LDO to the PCB. The PCB then acts like a heatsink, providing more area to distribute the heat generated by the LDO.

## 5.4 $C_{DELAY}$ Calculations (typical)

$$C = I \bullet \frac{\Delta T}{\Delta V}$$

Where:

| | | |
|---|---|---|
| C | = | $C_{DELAY}$ Capacitor |
| I | = | $C_{DELAY}$ charging current, 140 nA typical. |
| $\Delta$T | = | time delay |
| $\Delta$V | = | $C_{DELAY}$ threshold voltage, 0.42V typical |

$$C = I \bullet \frac{\Delta T}{\Delta V} = \frac{(140nA \bullet \Delta T)}{0.42V} = 333.3 \times 10^{-09} \bullet \Delta T$$

For a delay of 300ms,

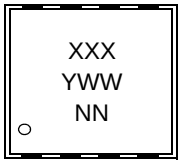
C = 333.3E-09 *.300

C = 100E-09 µF (0.1 µF)

## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

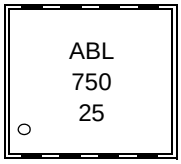
8-Lead DFN (2x3)



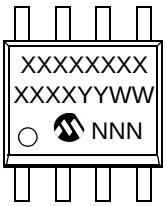

| Standard / Extended Temp | | | |
|---|---|---|---|
| **Code** | **Voltage Options *** | **Code** | **Voltage Options *** |
| ABL | 0.8 | ABR | 3.0 |
| ABM | 1.2 | ABS | 3.3 |
| ABP | 1.8 | ABT | 5.0 |
| ABQ | 2.5 | ABU | ADJ |

* Custom output voltages available upon request. Contact your local Microchip sales office for more information.

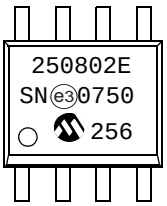
Example:




8-Lead SOIC (150 mil)




Example:

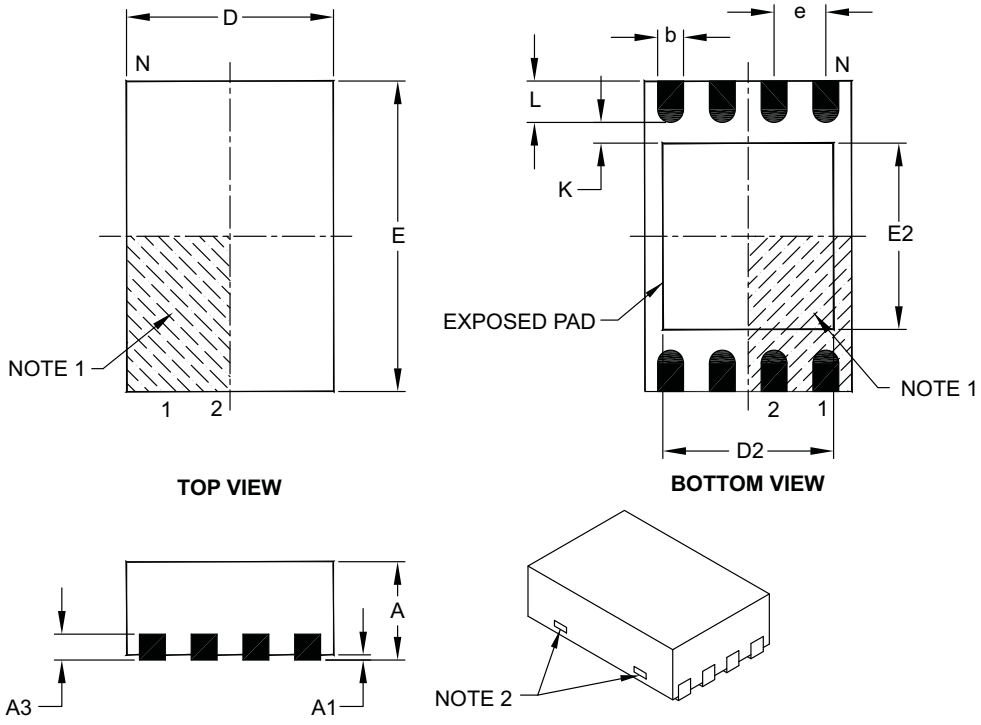



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | – | 1.75 |
| Exposed Pad Width | E2 | 1.50 | – | 1.90 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

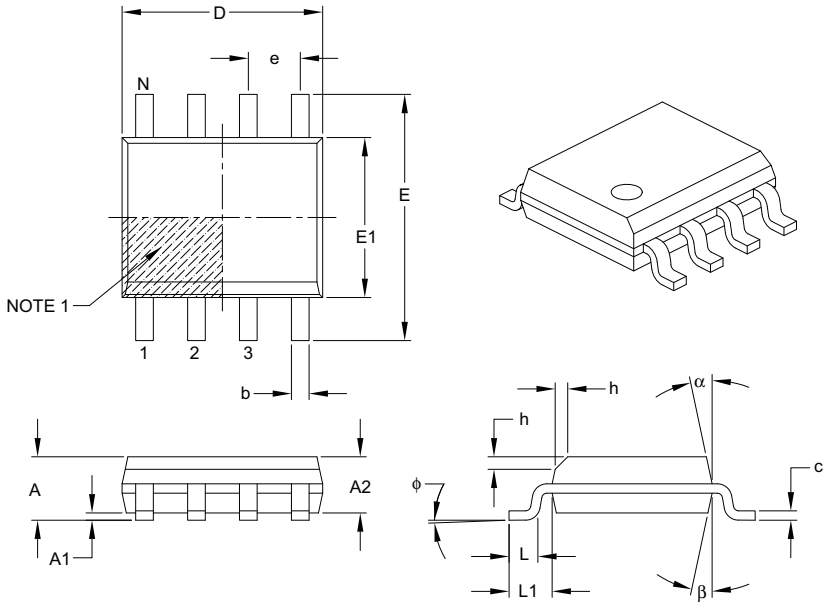
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision B (December 2007)

- Updated Temperature Specifications in **Section 1.0 “Electrical Characteristics”**.
- Updated **Section 6.0 “Packaging Information”**.
- Updated Templates.

## Revision A (December 2006)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | XX | X | X | X/ | XX |
|---|---|---|---|---|---|
| Device | Output Voltage | Feature Code | Tolerance | Temp. | Package |

| | | |
|---|---|---|
| Device: | MCP1725: | 500 mA Low Dropout Regulator |
| | MCP1725T: | 500 mA Low Dropout Regulator, Tape and Reel |
| Output Voltage *: | 08 = | 0.8V “Standard” |
| | 12 = | 1.2V “Standard” |
| | 18 = | 1.8V “Standard” |
| | 25 = | 2.5V “Standard” |
| | 30 = | 3.0V “Standard” |
| | 33 = | 3.3V “Standard” |
| | 50 = | 5.0V “Standard” |
| | *Contact factory for other output voltage options | |
| Extra Feature Code: | 0 = | Fixed |
| Tolerance: | 2 = | 2.0% (Standard) |
| Temperature: | E = | -40°C to +125°C |
| Package Type: | MC = | Plastic Dual Flat No Lead (DFN) (2x3 Body), 8-lead |
| | SN = | Plastic Small Outline (150 mil Body), 8-lead |

**Examples:**

a) MCP1725-0802E/MC: 0.8V Low Dropout Regulator, 8LD DFN pkg.

b) MCP1725T-1202E/MC: Tape and Reel, 1.2V Low Dropout Regulator, 8LD DFN pkg.

c) MCP1725-1802E/MC: 1.8V Low Dropout Voltage Regulator, 8LD DFN pkg.

d) MCP1725T-2502E/MC: Tape and Reel, 2.5V Low Dropout Voltage Regulator, 8LD DFN pkg.

e) MCP1725-3002E/MC: 3.0V Low Dropout Voltage Regulator, 8LD DFN pkg.

f) MCP1725-3302E/MC: 3.3V Low Dropout Voltage Regulator, 8LD DFN pkg.

g) MCP1725T-5002E/MC: Tape and Reel, 5.0V Low Dropout Voltage Regulator, 8LD DFN pkg.

h) MCP1725-ADJE/MC: ADJ Low Dropout Voltage Regulator, 8LD DFN pkg.

i) MCP1725T-0802E/SN: Tape and Reel, 0.8V Low Dropout Voltage Regulator, 8LD SOIC pkg.

j) MCP1725-1202E/SN: 1.2V Low Dropout Voltage Regulator, 8LD SOIC pkg.

k) MCP1725T-1802E/SN: Tape and Reel, 1.8V Low Dropout Voltage Regulator, 8LD SOIC pkg.

l) MCP1725-2502E/SN: 2.5V Low Dropout Voltage Regulator, 8LD SOIC pkg.

m) MCP1725-3002E/SN: 3.0V Low Dropout Voltage Regulator, 8LD SOIC pkg.

n) MCP1725-3302E/SN: 3.3V Low Dropout Voltage Regulator, 8LD SOIC pkg.

o) MCP1725T-5002E/SN: Tape and Reel, 5.0V Low Dropout Voltage Regulator, 8LD SOIC pkg.

p) MCP1725T-ADJE/SN: Tape and Reel, ADJ Low Dropout Voltage Regulator, 8LD SOIC pkg.

**NOTES:**

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